Open NAND Flash Interface Specification

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Revision History

Revision Number	Description	Author	Revision Date
5.1 Draft 0.7	• Created based on Revision 5.0 incorporated ONFI 5.0 ECN-001/002/003/004/005 • Incorporated new timing modes for NV-DDR3 & NV-LPDDR4 • Added New Features/Training Sequences • Added Note for not supporting ODT Pin in ONFI	Kai-Uwe Schmidt & Sriram Balasubrahmanyam	November 23, 2021
5.1 Draft 0.8	• Incorporated TWG feedback on Draft 0.7 upto 03/01/2022 • Incorporated ONFI 5.0 ECN-006/008 • Parameter Page updates for new features • Added ESD specs • Updated tDQSRE/tAC spec min from 2ns to 1.5ns for TM20-22	Sriram Balasubrahmanyam	March 2, 2022
5.1 Draft 1.0	• Updated tREH/tRP/tDQSH/tDQSL, tJITper/tJITcc for DQS/RE specs for TM20-22 • Removed tWPRE/tRPRE for NV-DDR2/DDR3 mode • Changed tDQSRH(min) from 5ns to 3ns; Added tDQSRH (max) spec = 5ns • Updated Max data rate for same Package Electricals from 2400MT/s to 3600MT/s • Removed Section “Calcualting Pin Capacitance” since Parameter Page removed Byte 128 on ONFI5.0 • Few editorials, typos	Sriram Balasubrahmanyam	April 8, 2022
5.1 Final 1.0	• Removed tCCS/tADL, array timing parameters that were referencing (removed) parameter page definitions • Made Parameter Page Byte 143, bit 1 as reserved since pincap specs were removed • Updated Feature Address 24h (WDCA) ‘tFEAT’ time as vendor specific • Added clarification note for per-pin vrefq absolute method • Updated ICC4R/ICC4W/ICCQ4R/ICCQ4W for >2400MT/s & ≤3600MT/s	Sriram Balasubrahmanyam	May 3, 2022

Table of Contents

1. Introduction

1.1. Goals and Objectives

This specification defines a standardized NAND Flash device interface that provides the means for a system to be designed that supports a range of NAND Flash devices without direct design pre-association. The solution also provides the means for a system to seamlessly make use of new NAND devices that may not have existed at the time that the system was designed.

Some of the goals and requirements for the specification include:

- Support range of device capabilities and new unforeseen innovation
- Consistent with existing NAND Flash designs providing orderly transition to ONFI
- Capabilities and features are self-described in a parameter page such that hard-coded chip ID tables in the host are not necessary
- Flash devices are interoperable and do not require host changes to support a new Flash device
- Define a higher speed NAND interface that is compatible with existing NAND Flash interface
- Allow for separate core (Vcc) and I/O (VccQ) power rails

1.2. References

The specification makes reference to the following specifications and standards:

- JEDEC SSTL_18 standard. Standard is available at http://www.jedec.org.

1.3. Definitions, abbreviations, and conventions

1.3.1. Definitions and Abbreviations

The terminology used in this specification is intended to be self-sufficient and does not rely on overloaded meanings defined in other specifications. Terms with specific meaning not directly clear from the context are clarified in the following sections.

1.3.1.1. address

The address is comprised of a row address and a column address. The row address identifies the page, block, and LUN to be accessed. The column address identifies the byte or word within a page to access. The least significant bit of the column address shall always be zero in the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interfaces.

1.3.1.2. asynchronous

Asynchronous is when data is latched with the WE_n signal for writes and RE_n signal for reads.

1.3.1.3. block

Consists of multiple pages and is the smallest addressable unit for erase operations.

1.3.1.4. column

The byte (x8 devices) or word (x16 devices) location within the page register.

1.3.1.1. CTT

Acronym for Center Tapped Termination

1.3.1.2. data burst

A data burst is a continuous set of data input or data output cycles without a pause. Specifically, there is not more than a data cycle time of pause within the data sequence.

1.3.1.2.1. data burst end

The host issues a new command after exiting the data burst. This exits NAND read mode and ends the data burst.

1.3.1.2.2. data burst exit

The host brings CE_n, ALE or CLE high during the data burst. ODT is off (if enabled) when in exit state and warmup cycles are re-issued (if enabled) if the data burst is continued after exit.

1.3.1.2.3. data burst pause

The host stops DQS (input burst) or RE (output burst) during data burst. ODT (if enabled) stays enabled the entire pause time and warmup cycles (if enabled) are not re-issued when continuing the data burst from pause.

1.3.1.1. DBI

Acronym for Data Bus Inversion.

1.3.1.2. DDR

Acronym for double data rate.

1.3.1.3. defect area

The defect area is where factory defects are marked by the manufacturer. Refer to section 3.3.

1.3.1.4. Deselected (ODT state)

When on-die termination is used, the LUN may be in a Deselected, Selected, or Sniff state with associated actions for each. Refer to section 4.17.

1.3.1.5. device

The packaged NAND unit. A device consists of one or more NAND Targets.

1.3.1.6. differential signaling

Differential signaling is a method of transmitting information by means of two complementary signals. The opposite technique is called single-ended signaling. The RE_n and DQS signals may each have complementary signals enabled to improve noise immunity, refer to section 4.11.2.

1.3.1.7. Dword

A Dword is thirty-two (32) bits of data. A Dword may be represented as 32 bits, as two adjacent words, or as four adjacent bytes. When shown as bits the least significant bit is bit 0 and most significant bit is bit 31. The most significant bit is shown on the left. When shown as words the least significant word (lower) is word 0 and the most significant (upper) word is word 1. When shown as bytes the least significant byte is byte 0 and the most significant byte is byte 3. See Figure 1 for a description of the relationship between bytes, words, and Dwords.

1.3.1.8. Host Target

A set of NAND Targets that share the same host CE_n signal. If CE_n reduction is not used, then a Host Target is equivalent to a NAND Target.

1.3.1.9. latching edge

The latching edge describes the edge of the CLK, RE_n, WE_n, or DQS signal that the contents of the data bus are latched on.

For NV-DDR, the latching edge for data cycles is both the rising and falling edges of the DQS signal. For command and address cycles the latching edge is the rising edge of the CLK signal.

For NV-DDR2 and NV_DDR3, the latching edge for data cycles is both the rising and falling edges of the DQS signal. For command and address cycles the latching edge is the rising edge of the WE_n signal.

1.3.1.1. LTT

Acronym for Low Tapped Termination

1.3.1.2. LUN (logical unit number)

The minimum unit that can independently execute commands and report status. There are one or more LUNs per NAND Target.

1.3.1.3. na

na stands for “not applicable”. Fields marked as “na” are not used.

1.3.1.4. NAND Target

A set of LUNs that share one CE_n signal within one NAND package.

1.3.1.5. O/M

O/M stands for Optional/Mandatory requirement. When the entry is set to “M”, the item is mandatory. When the entry is set to “O”, the item is optional.

1.3.1.6. on-die termination (ODT)

On-die termination is a type of electrical termination where the termination is provided by the NAND device. On-die termination is commonly referred to by its acronym, ODT. Refer to section 4.17.

1.3.1.7. page

The smallest addressable unit for read and program operations.

1.3.1.8. page register

Register used to read data from that was transferred from the Flash array. For program operations, the data is placed in this register prior to transferring the data to the Flash array.

1.3.1.9. partial page (obsolete)

A portion of the page, referred to as a partial page, may be programmed if the NAND Target supports more than one program per page as indicated in the parameter page. The host may choose to read only a portion of the data from the page register in a read operation; this portion may also be referred to as a partial page.

1.3.1.10. read request

A read request is a data output cycle request from the host that results in a data transfer from the device to the host. Refer to section 4.3 for information on data output cycles.

1.3.1.11. row

Refers to the block and page to be accessed.

1.3.1.12. Selected (ODT state)

When on-die termination is used, the LUN may be in a Deselected, Selected, or Sniff state with associated actions for each. Refer to section 4.17.

1.3.1.13. single-ended signaling

Single-ended signaling is when a one signal is used to transmit information. The opposite technique is differential signaling.

1.3.1.14. Sniff (ODT state)

When on-die termination is used, the LUN may be in a Deselected, Selected, or Sniff state with associated actions for each. Refer to section 4.17.

1.3.1.15. source synchronous

Source synchronous is when the strobe (DQS) is forwarded with the data to indicate when the data should be latched. The strobe signal, DQS, can be thought of as an additional data bus bit.

1.3.1.16. SR[ ]

SR refers to the status register contained within a particular LUN. SR[x] refers to bit x in the status register for the associated LUN. Refer to section 5.13 for the definition of bit meanings within the status register.

1.3.1.17. target

This term is equivalent to a NAND Target. When there is no potential confusion between NAND Target and Host Target, the shorter term of “target” is used.

1.3.1.18. Uncorrectable Bit Error Rate, or ratio (UBER)

A metric for the rate of occurrence of data errors, equal to the number of data errors per bits read. Mathematically, it may be represented as:

UBER = cumulative number of data errors / cumulative number of bits read

Note: The cumulative number of bits read is the sum of all bits of data read back from the device, with multiple reads of the same memory bit as multiple bits read. For example, if a 100GB device is read ten times then there would be about 1TB ($8x10^{12}$ bits) read. The cumulative number of data errors is the count of the physical pages for which the device fails to return correct data.

1.3.1.19. Volume

A Volume is an appointed address to a NAND Target. Volumes are used as part of Volume addressing, refer to section 2.20.

1.3.1.20. VREFQ

Input reference voltage.

1.3.1.21. Vtt

Termination voltage.

1.3.1.22. word

A word is sixteen (16) bits of data. A word may be represented as 16 bits or as two adjacent bytes. When shown as bits the least significant bit is bit 0 and most significant bit is bit 15. The most significant bit is shown on the left. When shown as bytes the least significant byte (lower) is byte 0 and the most significant byte (upper) is byte 1. See Figure 1 for a description of the relationship between bytes, words and Dwords.

1.3.2. Conventions

The names of abbreviations and acronyms used as signal names are in all uppercase (e.g., CE_n). “_n” is used indicate an active low signal (i.e., an inverted logic sense). It is acceptable to use the overbar, trailing slash (\), or # symbol rather than “_n” to indicate an active low signal. “_t” is used to indicate the true signal and “_c” is used to indicate the complementary signal when using differential signaling for a signal pair (e.g., RE_n or DQS).

Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field. Numerical fields are unsigned unless otherwise indicated.

1.3.2.1. Precedence

If there is a conflict between text, figures, state machines, timing diagrams, and tables, the precedence shall be state machines, timing diagrams, tables, figures, and then text.

1.3.2.2. Keywords

Several keywords are used to differentiate between different levels of requirements.

1.3.2.2.1. mandatory

A keyword indicating items to be implemented as defined by this specification.

1.3.2.2.2. may

A keyword that indicates flexibility of choice with no implied preference.

1.3.2.2.3. optional

A keyword that describes features that are not required by this specification. However, if any optional feature defined by the specification is implemented, the feature shall be implemented in the way defined by the specification.

1.3.2.2.4. reserved

A keyword indicating reserved bits, bytes, words, fields, and opcode values that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this or other specifications. A reserved bit, byte, word, or field shall be cleared to zero, or in accordance with a future extension to this specification. The recipient shall not check reserved bits, bytes, words, or fields.

1.3.2.2.5. shall

A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to the specification.

1.3.2.2.6. should

A keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “it is recommended”.

1.3.2.3. Byte, word and Dword Relationships

Figure 1-1 illustrates the relationship between bytes, words and Dwords.

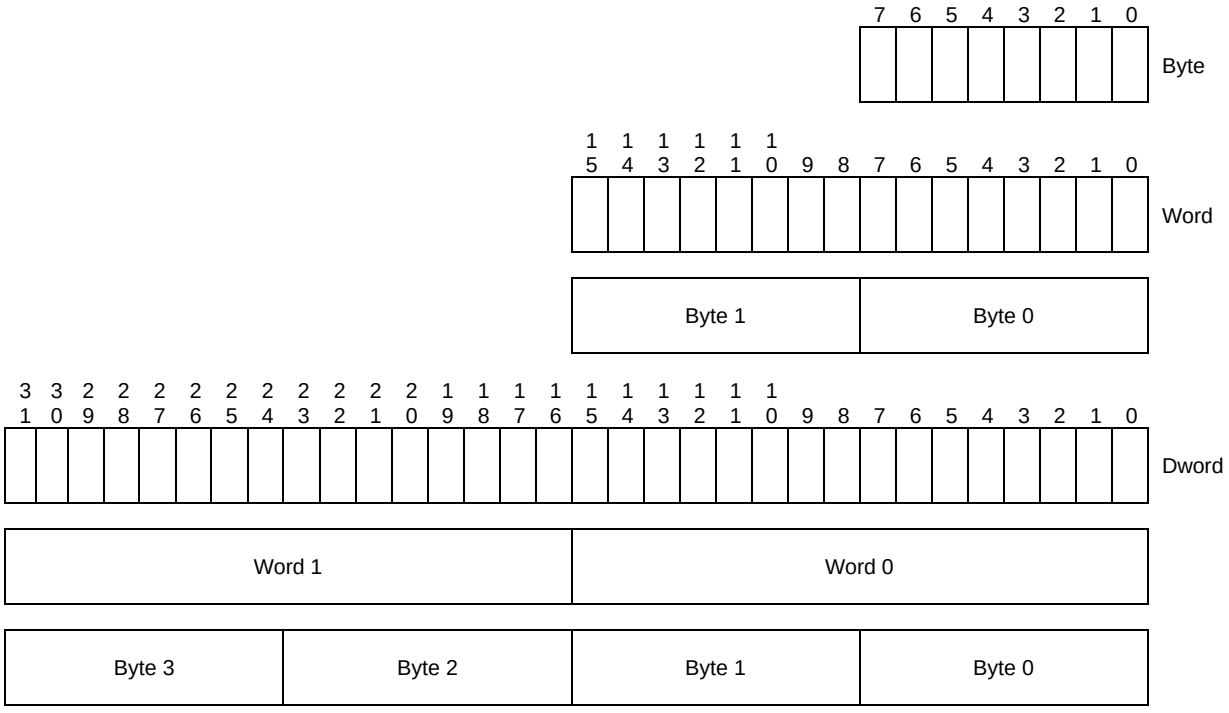


Figure 1-1 Byte, word and Dword relationships

1.3.2.4. Behavioral Flow Diagrams

For each function to be completed a state machine approach is used to describe the sequence and externally visible behavior requirements. Each function is composed of several states to accomplish a set goal. Each state of the set is described by an individual state table. Table 1-1

below shows the general layout for each of the state tables that comprise the set of states for the function.

State name	Action list		
	Transition condition 0	→	**Next state 0**
	Transition condition 1	→	**Next state 1**

Table 1-1 State Table Cell Description

Each state is identified by a unique state name. The state name is a brief description of the primary action taken during the state. Actions to take while in the state are described in the action list.

Each transition is identified by a transition label and a transition condition. The transition label consists of the state designator of the state from which the transition is being made followed by the state designator of the state to which the transition is being made. The transition condition is a brief description of the event or condition that causes the transition to occur and may include a transition action that is taken when the transition occurs. This action is described fully in the transition description text. Transition conditions are listed in priority order and are not required to be mutually exclusive. The first transition condition that evaluates to be true shall be taken.

Upon entry to a state, all actions to be executed in that state are executed. If a state is re-entered from itself, all actions to be executed in the state are executed again.

It is assumed that all actions are executed within a state and that transitions from state to state are instantaneous.

2. Physical Interface

2.1. TSOP-48 and WSOP-48 Pin Assignments

Figure 2-1 defines the pin assignments for devices using 48-pin TSOP or 48-pin WSOP packaging for 8-bit data access. Figure 2-2 defines the pin assignments for devices using 48-pin TSOP or 48-pin WSOP packaging for 16-bit data access. The package with 16-bit data access does not support the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interfaces. The physical dimensions of the TSOP package is defined in the JEDEC document MO-142 variation DD. The physical dimensions of the WSOP package is defined in the JEDEC document MO-259. The physical dimensions of the BGA-100, BGA-132, and BGA-152 packages are defined in the JEDEC document MO-304. The physical dimensions of the BGA-316 and BGA-272 packages are defined in the JEDEC document MO-210.

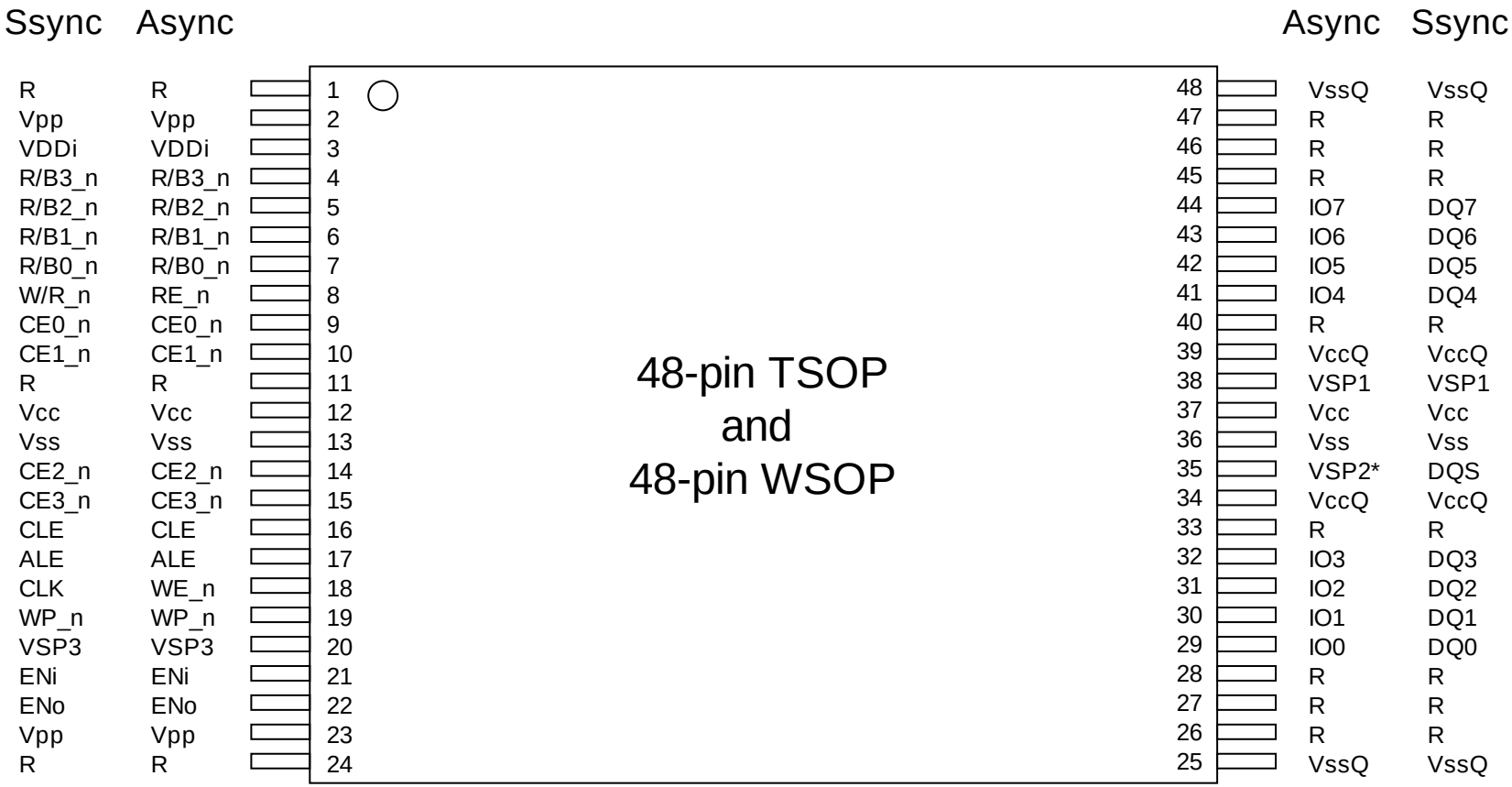


Figure 2-1 48-pin TSOP/WSOP pinout for 8-bit data access

NOTE: For a NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 capable part, pin 35 is not used when configured in the asynchronous data interface. Specifically, VSP2 is present for SDR only parts.

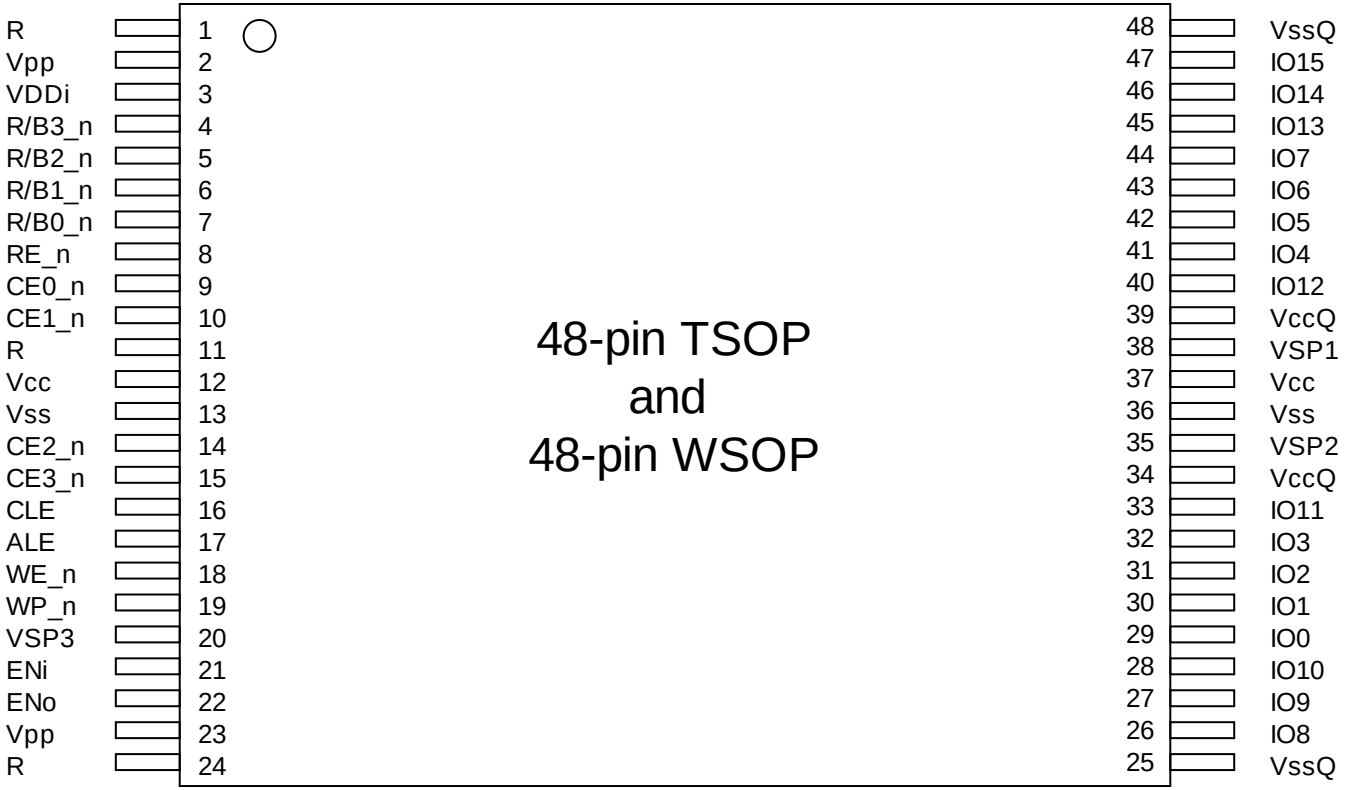


Figure 2-2 48-pin TSOP/WSOP pinout for 16-bit data access

2.2. LGA-52 Pad Assignments

Figure 2-3 defines the pad assignments for devices using 52-pad LGA packaging with 8-bit data access. An option is specified for two independent 8-bit data buses. Figure 2-4 defines the pad assignments for devices using 52-pad LGA packaging with 16-bit data access. The physical dimensions of the package are 12mmx17mm or 14mmx18mm. Figure 2-5 defines the pad spacing requirements for the 52-pad LGA package for both package dimensions. These LGA packages do not support the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface.

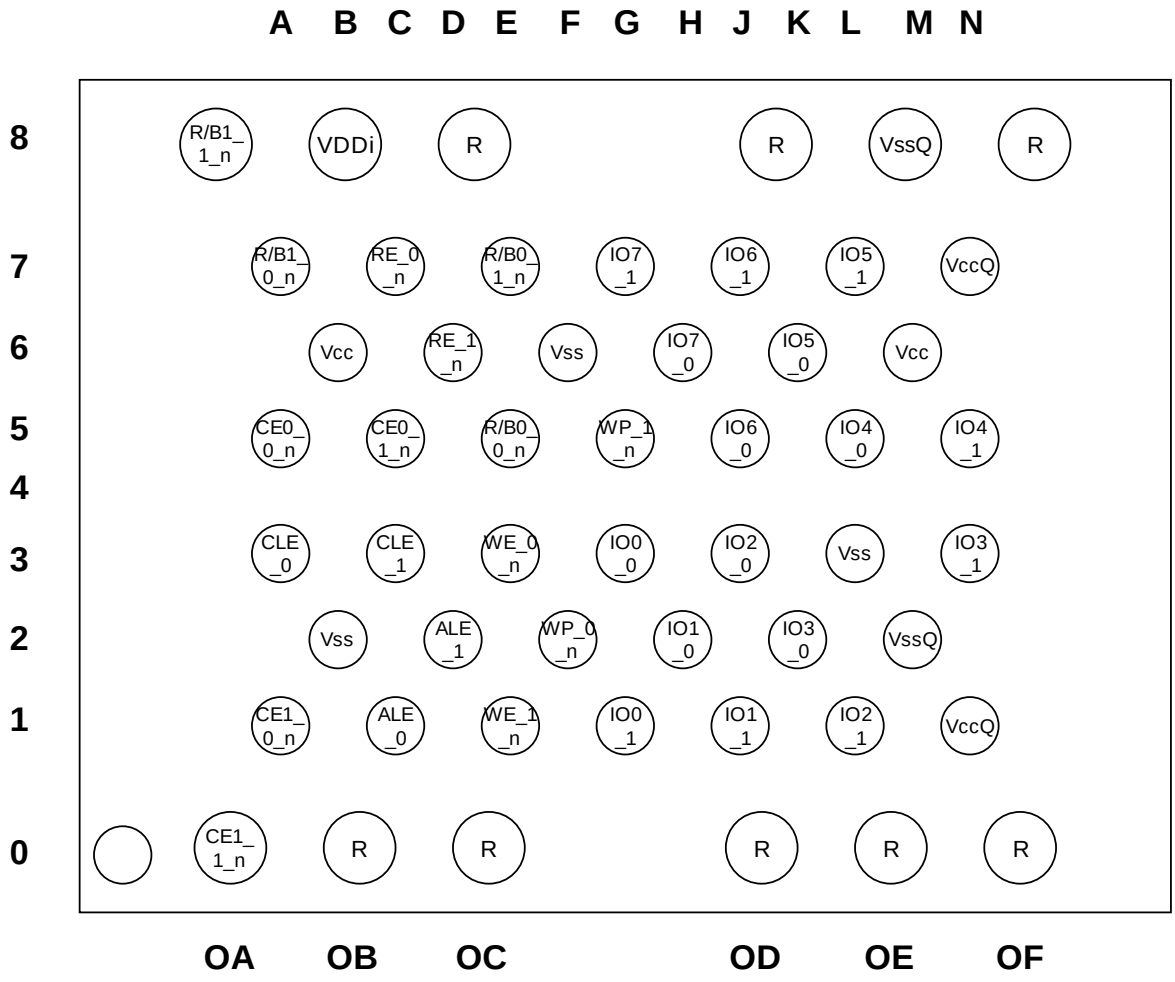


Figure 2-3 LGA pinout for 8-bit data access

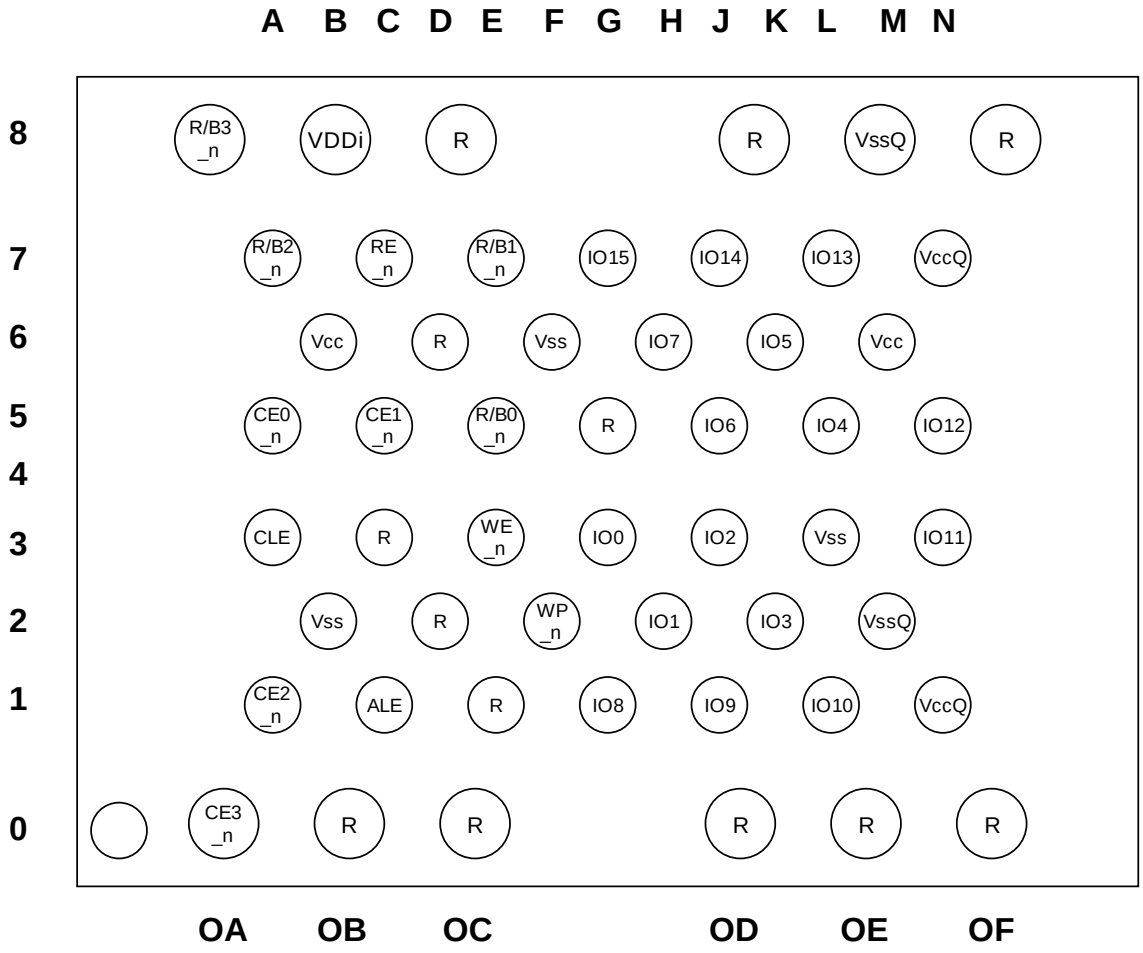


Figure 2-4 LGA pinout for 16-bit data access

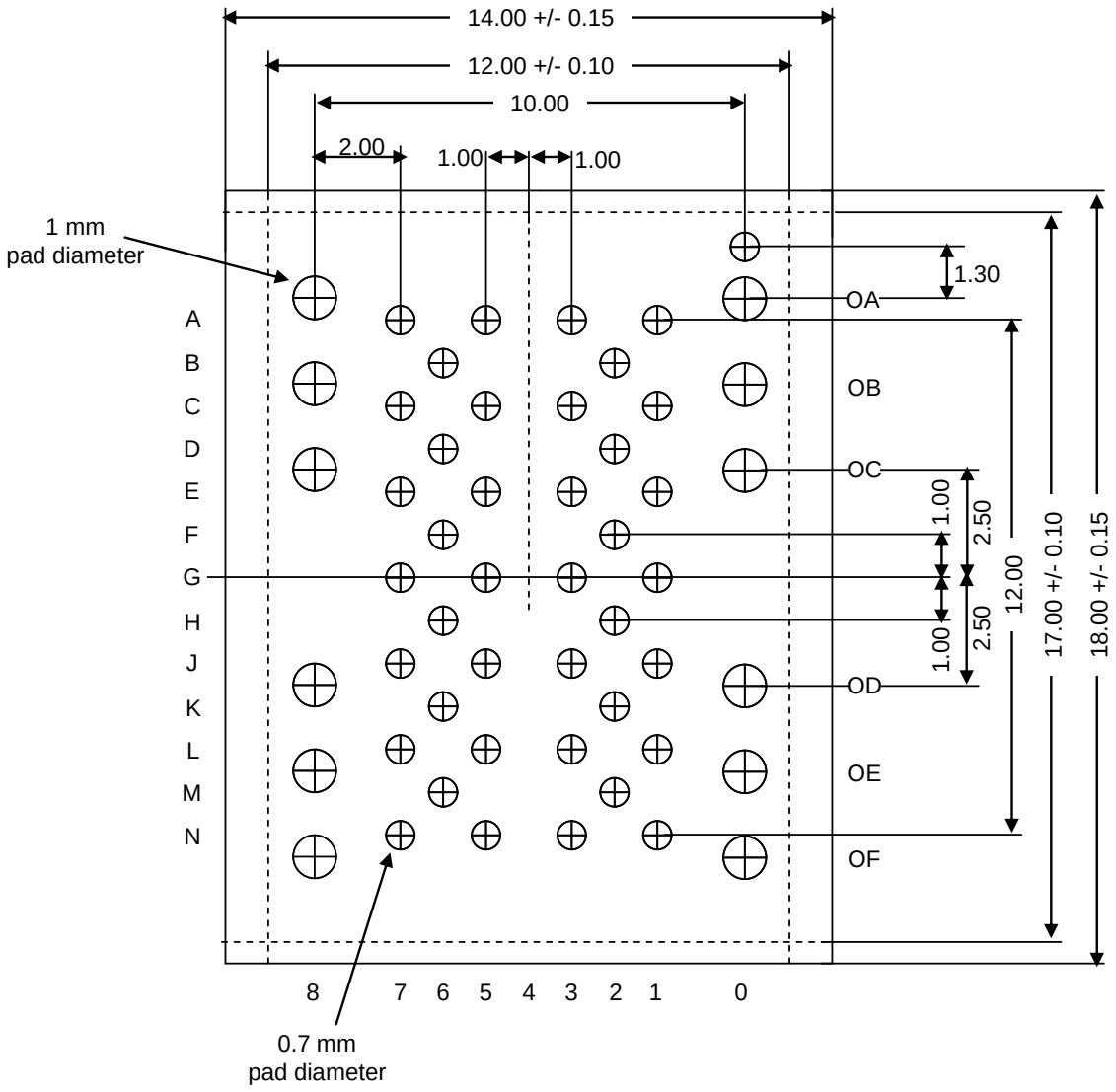
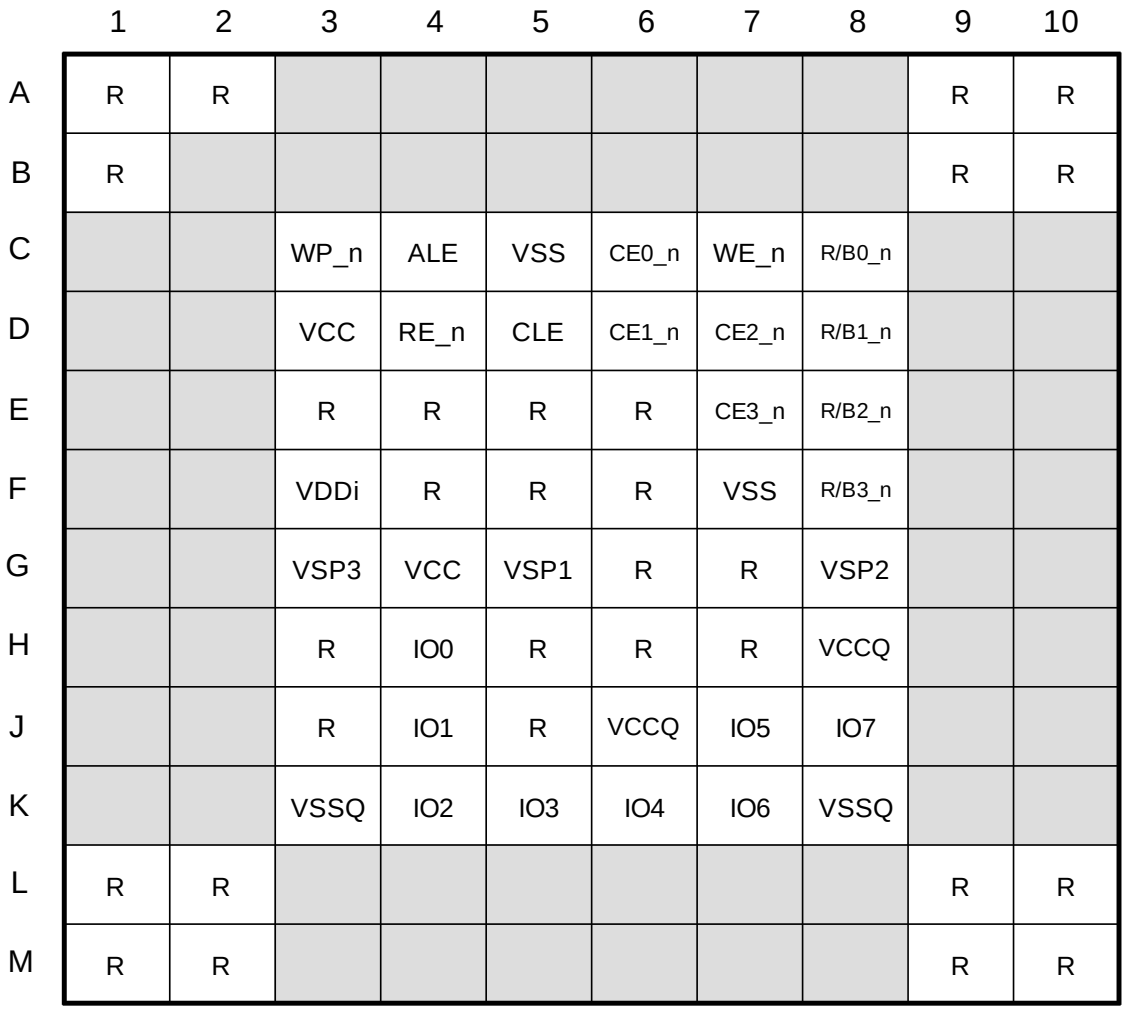


Figure 2-5 LGA-52 pad spacing requirements (bottom view, dimensions in millimeters)

2.3. BGA-63 Ball Assignments

Figure 2-6 defines the ball assignments for devices using 63-ball BGA packaging with 8-bit data access for the SDR data interface. Figure 2-7 defines the ball assignments for devices using 63-ball BGA packaging with 8-bit data access for the NV-DDR data interface. Figure 2-8 defines the ball assignments for devices using 63-ball BGA packaging with 16-bit data access for the SDR data interface. The 63-ball BGA package with 16-bit data access does not support the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface. Figure 2-9 defines the ball spacing requirements for the 63-ball BGA package. The 63-ball BGA package has two solder ball diameter sizes: 0.45±0.05mm and 0.55±0.05mm post reflow.



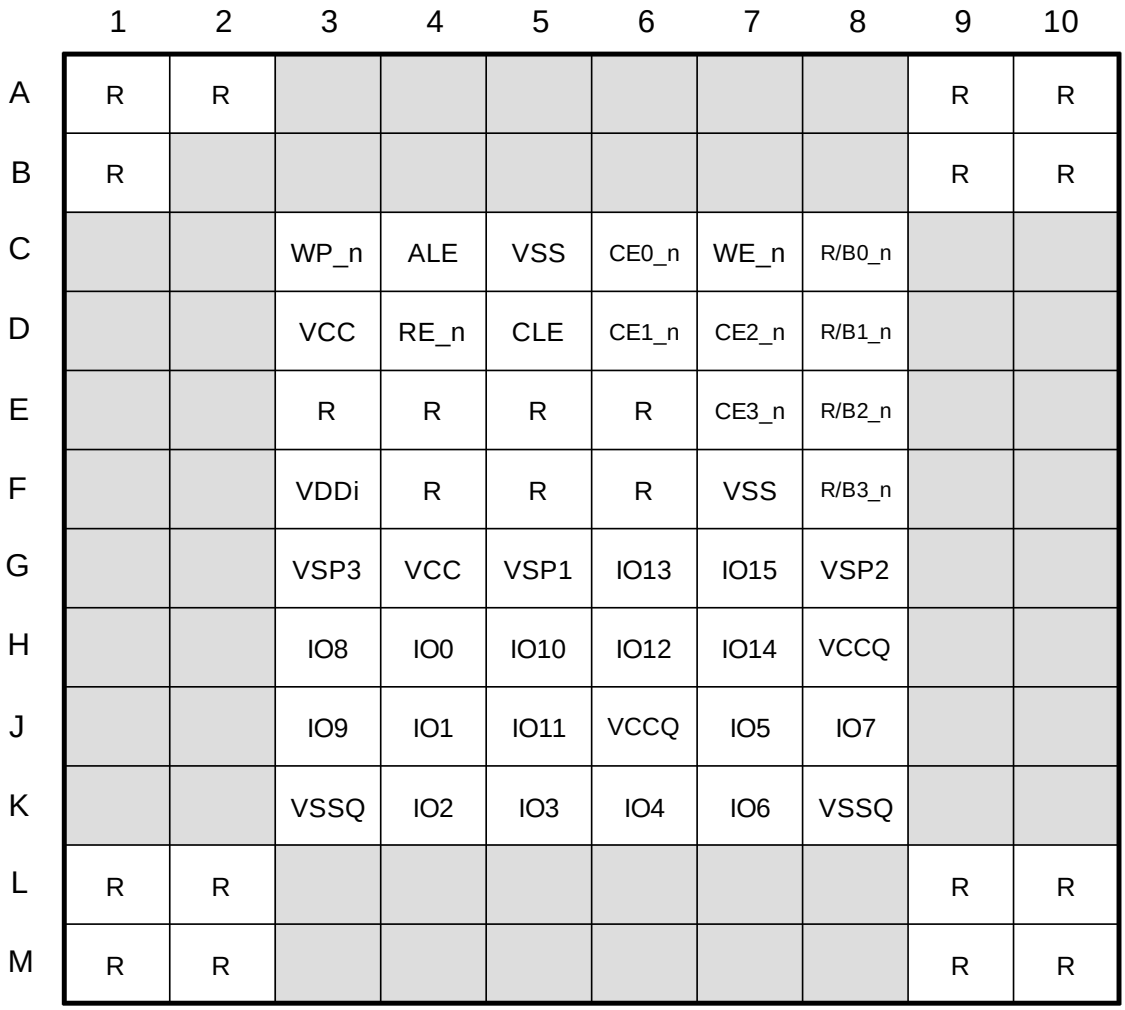
	1	2	3	4	5	6	7	8	9	10
A	R	R							R	R
B	R								R	R
C			WP_n	ALE	VSS	CE0_n	WE_n	R/B0_n		
D			VCC	RE_n	CLE	CE1_n	CE2_n	R/B1_n		
E			R	R	R	R	CE3_n	R/B2_n		
F			VDDi	R	R	R	VSS	R/B3_n		
G			VSP3	VCC	VSP1	R	R	VSP2		
H			R	IO0	R	R	R	VCCQ		
J			R	IO1	R	VCCQ	IO5	IO7		
K			VSSQ	IO2	IO3	IO4	IO6	VSSQ		
L	R	R							R	R
M	R	R							R	R

Figure 2-6 BGA-63 ball assignments for 8-bit data access, SDR only data interface

Note that WE_n is located at ball H7 when a NV-DDR capable part is used in SDR mode.

	1	2	3	4	5	6	7	8	9	10
A	R	R							R	R
B	R								R	R
C			WP_n	ALE	VSS	CE0_n	R	R/B0_n		
D			VCC	W/R_n	CLE	CE1_n	CE2_n	R/B1_n		
E			R	R	R	R	CE3_n	R/B2_n		
F			VDDi	R	VREFQ	R	VSS	R/B3_n		
G			VSP3	VCC	VSP1	R	R	VSP2		
H			R	DQ0	DQS_c	CLK_c	CLK_t	VCCQ		
J			R	DQ1	DQS_t	VCCQ	DQ5	DQ7		
K			VSSQ	DQ2	DQ3	DQ4	DQ6	VSSQ		
L	R	R							R	R
M	R	R							R	R

Figure 2-7 BGA-63 ball assignments for 8-bit data access, NV-DDR data interface



	1	2	3	4	5	6	7	8	9	10
A	R	R							R	R
B	R								R	R
C			WP_n	ALE	VSS	CE0_n	WE_n	R/B0_n		
D			VCC	RE_n	CLE	CE1_n	CE2_n	R/B1_n		
E			R	R	R	R	CE3_n	R/B2_n		
F			VDDi	R	R	R	VSS	R/B3_n		
G			VSP3	VCC	VSP1	IO13	IO15	VSP2		
H			IO8	IO0	IO10	IO12	IO14	VCCQ		
J			IO9	IO1	IO11	VCCQ	IO5	IO7		
K			VSSQ	IO2	IO3	IO4	IO6	VSSQ		
L	R	R							R	R
M	R	R							R	R

Figure 2-8 BGA-63 ball assignments for 16-bit, SDR only data interface

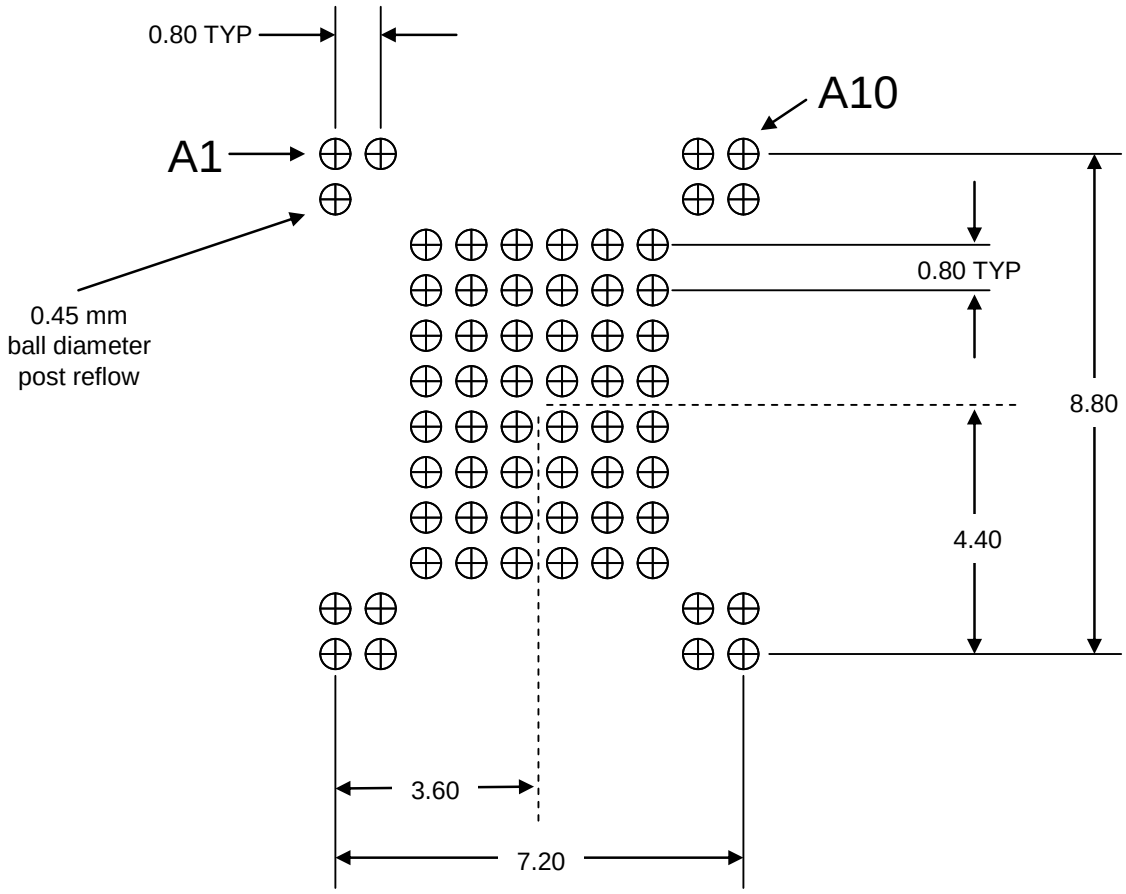


Figure 2-9 BGA-63 ball spacing requirements (top view, dimensions in millimeters)

2.4. BGA-100 Ball Assignments

Figure 2-10 defines the ball assignments for devices using 100-ball BGA packaging with dual 8-bit data access for the SDR data interface. Figure 2-11 defines the ball assignments for devices using 100-ball BGA packaging with dual 8-bit data access for the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface. Figure 2-12 defines the ball spacing requirements for the 100-ball BGA package. The 100-ball BGA has two package sizes: 12mm x 18mm and 14mm x 18mm and two solder ball diameter sizes: 0.45±0.05mm and 0.55±0.05mm post reflow for both package sizes.

The functionality of balls H7 and K5 is overloaded. If CE_n pin reduction is supported, then these balls have the functionality of ENo and ENi. If CE_n pin reduction is not supported, then these balls are used as R/B1_1_n and CE1_0_n. In the case of CE_n pin reduction, only two CE_n balls are used for the package and thus re-purposing the functionality of these balls does not cause an issue.

	1	2	3	4	5	6	7	8	9	10
A	R	R							R	R
B	R									R
C										
D		R	RFT	VSP3_1	WP_1_n	VSP2_1	VSP1_1	RFT	R	
E		R	RFT	VSP3_0	WP_0_n	VSP2_0	VSP1_0	RFT	VDDi	
F		VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	
G		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	
H		VSSQ	VCCQ	R	R	R/B0_1_n	R/B1_1_n ENo	VCCQ	VSSQ	
J		IO0_1	IO2_1	ALE_1	CE1_1_n	R/B0_0_n	R/B1_0_n	IO5_1	IO7_1	
K		IO0_0	IO2_0	ALE_0	CE1_0_n ENi	CE0_1_n	CE0_0_n	IO5_0	IO7_0	
L		VCCQ	VSSQ	VCCQ	CLE_1	RE_1_n	VCCQ	VSSQ	VCCQ	
M		IO1_1	IO3_1	VSSQ	CLE_0	RE_0_n	VSSQ	IO4_1	IO6_1	
N		IO1_0	IO3_0	NC	NC	NC	WE_1_n	IO4_0	IO6_0	
P		VSSQ	VCCQ	NC	NC	NC	WE_0_n	VCCQ	VSSQ	
R										
T	R									R
U	R	R							R	R

Figure 2-10 BGA-100 ball assignments for dual 8-bit data access, SDR data interface

	1	2	3	4	5	6	7	8	9	10
A	R	R							R	R
B	R									R
C										
D		ZQ_0	RFT	VSP3_1	WP_1_n	VSP2_1	VSP1_1	RFT	ZQ_1	
E		R	RFT	VSP3_0	WP_0_n	VSP2_0	VSP1_0	RFT	VDDi	
F		VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	
G		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	
H		VSSQ	VCCQ	VREFQ_1	VREFQ_0	R/B0_1_n	R/B1_1_n ENo	VCCQ	VSSQ	
J		DQ0_1	DQ2_1	ALE_1	CE1_1_n	R/B0_0_n	R/B1_0_n	DQ5_1	DQ7_1	
K		DQ0_0	DQ2_0	ALE_0	CE1_0_n ENi	CE0_1_n	CE0_0_n	DQ5_0	DQ7_0	
L		VCCQ	VSSQ	VCCQ	CLE_1	W/R_1_n RE_1_t	VCCQ	VSSQ	VCCQ	
M		DQ1_1	DQ3_1	VSSQ	CLE_0	W/R_0_n RE_0_t	VSSQ	DQ4_1	DQ6_1	
N		DQ1_0	DQ3_0	DQS_1_c	DQS_1_t	RE_1_c	CLK_1 WE_1	DQ4_0	DQ6_0	
P		VSSQ	VCCQ	DQS_0_c	DQS_0_t	RE_0_c	CLK_0 WE_0	VCCQ	VSSQ	
R										
T	R									R
U	R	R							R	R

Figure 2-11 BGA-100 ball assignments for dual 8-bit data access, NV-DDR, NV-DDR2 or NV-DDR3 data interface

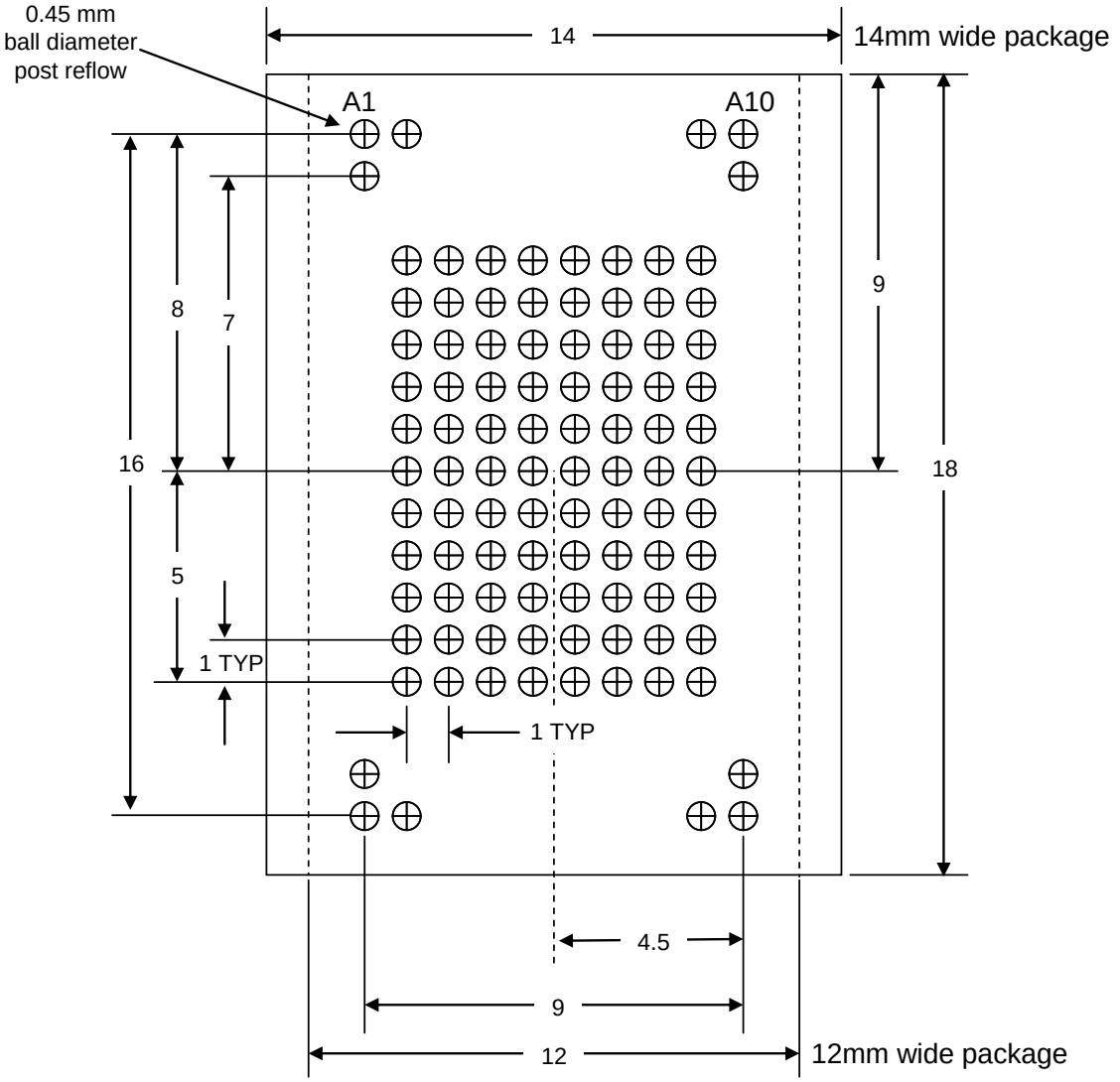


Figure 2-12 BGA-100 ball spacing requirements (top view, dimensions in millimeters)

2.5. BGA-152 and BGA-132 Ball Assignments

Figure 2-13 defines the ball assignments for devices using 152-ball BGA packaging with dual 8-bit data access. Figure 2-14 defines the ball assignments for devices using 132-ball BGA packaging with dual 8-bit data access. Figure 2-15 defines the ball spacing requirements for the 152-ball and 132-ball BGA package. There are two package sizes: 12mm x 18mm (132-ball) and 14mm x 18mm (152-ball) and two solder ball diameter sizes: 0.45±0.05mm and 0.55±0.05mm post reflow for both package sizes. Note: If the 12mm x 18mm package size is used, then outer columns are not present, and the package is a 132-ball BGA. For the 132-ball BGA, the columns are re-enumerated to begin at column 1 (i.e. BGA-152 column 2 becomes BGA-132 column 1). Depending on the data interface selected, balls may have different usages and/or meanings. Refer to for the specific use for each ball in each data interface. ONFI does not support ODT pin. Ball-map showing ODT_*_n/WP_*_n muxing is just as a reference to JEDEC

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC	NC						NC	NC	NC	NC
B	NC	NC	NC	NC						NC	NC	NC	NC
C	NU	NU	NU	NU						NU	NU	NU	NU
D	NU	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU	NU
E	NU	NU	VSSQ	DQ2_1	VSSQ	DQS_1 (DQS_1_t)		RE_1_n (RE_1_t) or W/R_1_n	VSSQ	DQ5_1	VSSQ	NU	NU
F			DQ0_1	DQ1_1	DQS_1_c	RE_1_c		WE_1_n or CK_1	VREFQ_ 1	DQ6_1	DQ7_1		
G			VSSQ	VCCQ	ALE_1	CLE_1		DBI_1 or NU	VSSQ or NU	VCCQ	VSSQ		
H			ENo or NU or CE2_0_n	ENi or NU or CE3_0_n	WP_1_n or ODT_1_n	NU		CE1_1_n	CE0_1_n	RZQ_1	NU		
J			VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS		
K			NU	RZQ_0	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_n or ODT_0_n	NU or CE3_1_n	VDDi or NU or CE2_1_n		
L			VSSQ	VCCQ	VSSQ or NU	DBI_0 or NU		CLE_0	ALE_0	VCCQ	VSSQ		
M			DQ7_0	DQ6_0	VREFQ_0	WE_0_n or CK_0		RE_0_c	DQS_0_c	DQ1_0	DQ0_0		
N	NU	NU	VSSQ	DQ5_0	VSSQ	RE_0_n (RE_0_t) or W/R_0_n		DQS_0 or (DQS_0_t)	VSSQ	DQ2_0	VSSQ	NU	NU
P	NU	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU	NU
R	NU	NU	NU	NU						NU	NU	NU	NU
T	NC	NC	NC	NC						NC	NC	NC	NC
U	NC	NC	NC	NC						NC	NC	NC	NC

Figure 2-13 BGA-152 ball assignments for dual 8-bit data access

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	NC						NC	NC	NC
B	NC	NC	NC						NC	NC	NC
C	NU	NU	NU						NU	NU	NU
D	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU
E	NU	VSSQ	DQ2_1	VSSQ	DQS_1 (DQS_1_t)		RE_1_n (RE_1_t) or W/R_1_n	VSSQ	DQ5_1	VSSQ	NU
F		DQ0_1	DQ1_1	DQS_1_c	RE_1_c		WE_1_n or CK_1	VREFQ_ 1	DQ6_1	DQ7_1	
G		VSSQ	VCCQ	ALE_1	CLE_1		DBI_1 or NU	VSSQ or NU	VCCQ	VSSQ	
H		ENo or NU or CE2_0_n	ENi or NU or CE3_0_n	WP_1_n or ODT_1_n	NU		CE1_1_n	CE0_1_n	RZQ_1	NU	
J		VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS	
K		NU	RZQ_0	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_n or ODT_0_n	NU or CE3_1_n	VDDi or NU or CE2_1_n	
L		VSSQ	VCCQ	VSSQ or NU	DBI_0 or NU		CLE_0	ALE_0	VCCQ	VSSQ	
M		DQ7_0	DQ6_0	VREFQ_0	WE_0_n or CK_0		RE_0_c	DQS_0_c	DQ1_0	DQ0_0	
N	NU	VSSQ	DQ5_0	VSSQ	RE_0_n (RE_0_t) or W/R_0_n		DQS_0 or (DQS_0_t)	VSSQ	DQ2_0	VSSQ	NU
P	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU
R	NU	NU	NU						NU	NU	NU
T	NC	NC	NC						NC	NC	NC
U	NC	NC	NC						NC	NC	NC

Figure 2-14 BGA-132 ball assignments for dual 8-bit data access

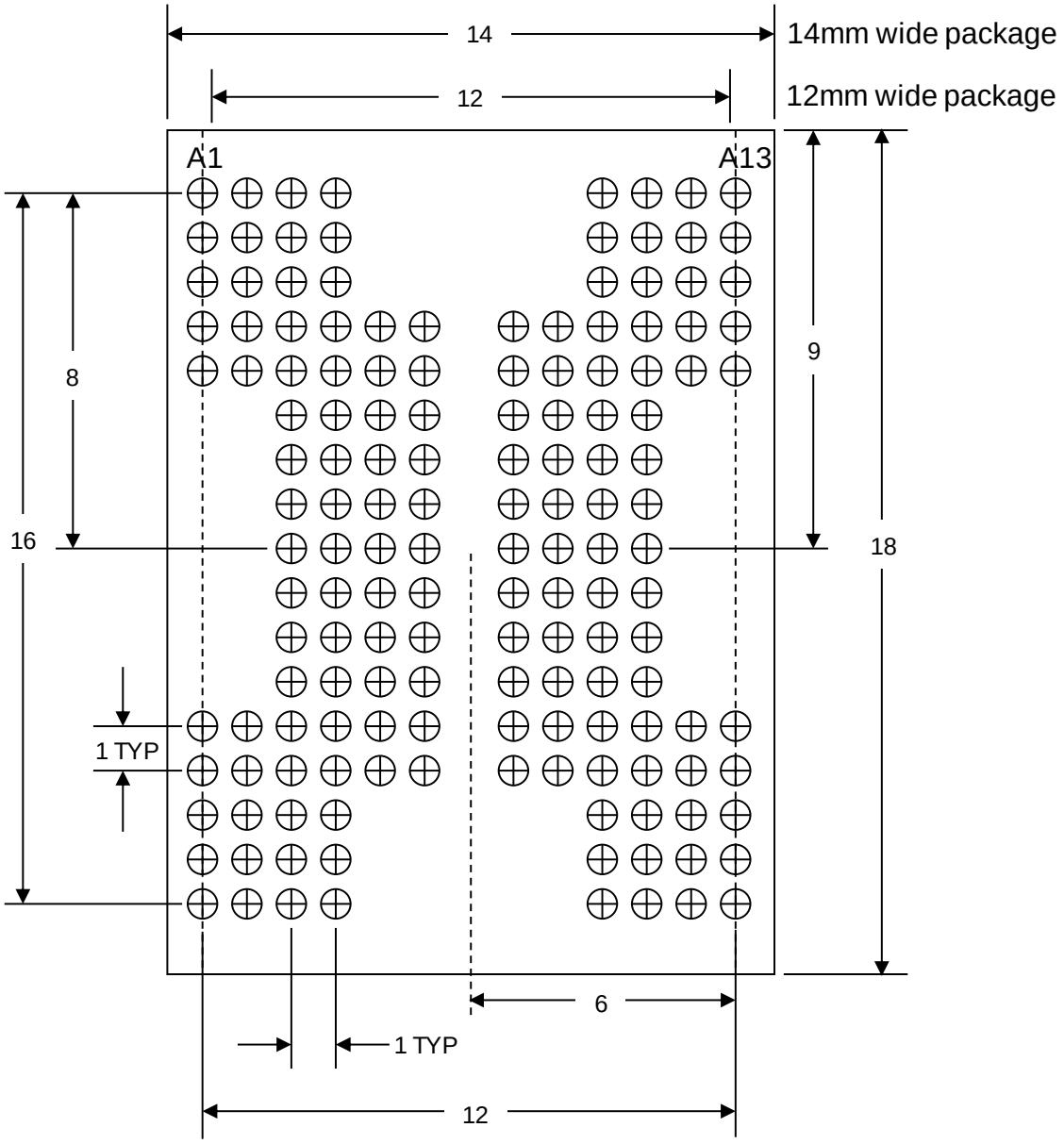


Figure 2-15 BGA-152 and BGA-132 ball spacing requirements (top view, dimensions in millimeters)

2.6. BGA-272, BGA-252, and BGA-316 Ball Assignments

Figure 2-16 defines the ball assignments for devices using 272-ball BGA packaging with quad 8-bit data access. Figure 2-17 defines the ball assignments for devices using 252-ball BGA packaging with quad 8-bit data access. Figure 2-18 defines the ball assignments for devices using 316-ball 16 CE_n BGA packaging with quad 8-bit data access. Figure 2-19 defines the ball assignments for devices using 316-ball 32 CE_n BGA packaging with quad 8-bit data access. Figure 2-20 defines the ball spacing requirements for the 272-ball and 252-ball BGA packages. Figure 2-21 defines the ball spacing requirements for the 316-ball BGA package. The package size for the 272-ball and 316-ball packages is 14mm x 18mm while the package size for the 252-

ball package is 12mm x 18mm. The 252-ball package removes the outer columns from the 272-ball package resulting in a smaller package size. The 252-ball ball assignment is also re-enumerated to begin at column 1 (ie. BGA-272 column 2 becomes BGA-252 column 1). Depending on the data interface selected, balls may have different usages and/or meanings. Refer to for the specific use for each ball in each data interface. ONFI does not support ODT pin. Ball-map showing ODT_*_n/WP_*_n muxing is just as a reference to JEDEC

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	NU									NU	NC	NC	NC
B	NC	NC	NU	VCCQ	VSS	VSS	VSS			VCC	VCCQ	VSS	VCCQ	NU	NC	NC
C	NC	NU	VCCQ	VSS	VSS	DQ0_2	DQ0_0			VSS	VSS	VSS	VSS	VCC	NU	NC
D	NU	VCC	VSS	VSS	VSS	DQ1_2	DQ1_0			DQ4_2	DQ4_0	VSS	VSS	VSS	VCC	NU
E	NU	VCC	VSS	VSS	VSS	DQ2_2	DQ2_0			DQ5_2	DQ5_0	VSS	VSS	VSS	VSS	NU
F		VSS	VSS	VSS	DQ3_0	DQS_2 (DQS_2_t)	DQS_0 (DQS_0_t)			DQ6_2	DQ6_0	VSS	VSS	VSS	VCCQ	
G		VCCQ	VSS	VSS	DQ3_2	DQS_2_c	DQS_0_c			VCCQ	DQ7_2	DQ7_0	RZQ_2	RZQ_0	VCCQ	
H		VCCQ	VSS	VSS	VSP0 R	VSP2 R	VSS			WE_0_n or CK_0	CE1_0_n	CE3_0_n	R/B0_0_n	R/B1_0_n	VSS	
J		ENi or NU	ENo or NU	VSS	VSS	DBI_2 or NU	DBI_0 or NU			WE_2_n or CK_2	CE1_2_n	CE3_2_n	R/B0_2_n	R/B1_2_n	VSP6 R	
K		VCC	WP_0_n or ODT_0_n	ALE_0	CLE_0	RE_0_n (RE_0_t) or W/R_0_n	RE_0_c			CE0_2_n	CE0_0_n	CE2_2_n	CE2_0_n	VSP4 or VDDi	VPP	
L		NU	WP_2_n or ODT_2_n	ALE_2	CLE_2	RE_2_n (RE_2_t) or W/R_2_n	RE_2_c			VREFQ	VREFQ	VSS	VSS	VSS	VSS	
M		VSS	VSS	VSS	VSS	VREFQ	VREFQ			RE_3_c	RE_3_n (RE_3_t) or W/R_3_n	CLE_3	ALE_3	WP_3_n or ODT_3_n	NU	
N		VPP	VSP5 or VDDi	CE2_1_n	CE2_3_n	CE0_1_n	CE0_3_n			RE_1_c	RE_1_n (RE_1_t) or W/R_1_n	CLE_1	ALE_1	WP_1_n ODT_1_n	VCC	
P		VSP7 R	R/B1_3_n	R/B0_3_n	CE3_3_n	CE1_3_n	WE_3_n or CK_3			DBI_1 or NU	DBI_3 or NU	VSS	VSS	NU	NU	
R		VSS	R/B1_1_n	R/B0_1_n	CE3_1_n	CE1_1_n	WE_1_n or CK_1			VSS	VSP3 R	VSP1 R	VSS	VSS	VCCQ	
T		VCCQ	RZQ_1	RZQ_3	DQ7_1	DQ7_3	VCCQ			DQS_1_c	DQS_3_c	DQ3_3	VSS	VSS	VCCQ	
U		VCCQ	VSS	VSS	VSS	DQ6_1	DQ6_3			DQS_1 (DQS_1_t)	DQS_3 (DQS_3_t)	DQ3_1	VSS	VSS	VSS	
V	NU	VSS	VSS	VSS	VSS	DQ5_1	DQ5_3			DQ2_1	DQ2_3	VSS	VSS	VSS	VCC	NU
W	NU	VCC	VSS	VSS	VSS	DQ4_1	DQ4_3			DQ1_1	DQ1_3	VSS	VSS	VSS	VCC	NU
Y	NC	NU	VCC	VSS	VSS	VSS	VSS			DQ0_1	DQ0_3	VSS	VSS	VCCQ	NU	NC
AA	NC	NC	NU	VCCQ	VSS	VCCQ	VCC			VSS	VSS	VSS	VCCQ	NU	NC	NC
AB	NC	NC	NC	NU									NU	NC	NC	NC

Figure 2-16 BGA-272 ball assignments for quad 8-bit data access

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	NU									NU	NC	NC
B	NC	NU	VCCQ	VSS	VSS	VSS			VCC	VCCQ	VSS	VCCQ	NU	NC
C	NU	VCCQ	VSS	VSS	DQ0_2	DQ0_0			VSS	VSS	VSS	VSS	VCC	NU
D	VCC	VSS	VSS	VSS	DQ1_2	DQ1_0			DQ4_2	DQ4_0	VSS	VSS	VSS	VCC
E	VCC	VSS	VSS	VSS	DQ2_2	DQ2_0			DQ5_2	DQ5_0	VSS	VSS	VSS	VSS
F	VSS	VSS	VSS	DQ3_0	DQS_2 (DQS_2_t)	DQS_0 (DQS_0_t)			DQ6_2	DQ6_0	VSS	VSS	VSS	VCCQ
G	VCCQ	VSS	VSS	DQ3_2	DQS_2_c	DQS_0_c			VCCQ	DQ7_2	DQ7_0	RZQ_2	RZQ_0	VCCQ
H	VCCQ	VSS	VSS	VSP0 R	VSP2 R	VSS			WE_0_n or CK_0	CE1_0_n	CE3_0_n	R/B0_0_n	R/B1_0_n	VSS
J	ENi or NU	ENo or NU	VSS	VSS	DBI_2 or NU	DBI_0 or NU			WE_2_n or CK_2	CE1_2_n	CE3_2_n	R/B0_2_n	R/B1_2_n	VSP6 R
K	VCC	WP_0_n or ODT_0_n	ALE_0	CLE_0	RE_0_n (RE_0_t) or W/R_0_n	RE_0_c			CE0_2_n	CE0_0_n	CE2_2_n	CE2_0_n	VSP4 or VDDi	VPP
L	NU	WP_2_n or ODT_2_n	ALE_2	CLE_2	RE_2_n (RE_2_t) or W/R_2_n	RE_2_c			VREFQ	VREFQ	VSS	VSS	VSS	VSS
M	VSS	VSS	VSS	VSS	VREFQ	VREFQ			RE_3_c	RE_3_n (RE_3_t) or W/R_3_n	CLE_3	ALE_3	WP_3_n or ODT_3_n	NU
N	VPP	VSP5 or VDDi	CE2_1_n	CE2_3_n	CE0_1_n	CE0_3_n			RE_1_c	RE_1_n (RE_1_t) or W/R_1_n	CLE_1	ALE_1	WP_1_n ODT_1_n	VCC
P	VSP7 R	R/B1_3_n	R/B0_3_n	CE3_3_n	CE1_3_n	WE_3_n or CK_3			DBI_1 or NU	DBI_3 or NU	VSS	VSS	NU	NU
R	VSS	R/B1_1_n	R/B0_1_n	CE3_1_n	CE1_1_n	WE_1_n or CK_1			VSS	VSP3 R	VSP1 R	VSS	VSS	VCCQ
T	VCCQ	RZQ_1	RZQ_3	DQ7_1	DQ7_3	VCCQ			DQS_1_c	DQS_3_c	DQ3_3	VSS	VSS	VCCQ
U	VCCQ	VSS	VSS	VSS	DQ6_1	DQ6_3			DQS_1 (DQS_1_t)	DQS_3 (DQS_3_t)	DQ3_1	VSS	VSS	VSS
V	VSS	VSS	VSS	VSS	DQ5_1	DQ5_3			DQ2_1	DQ2_3	VSS	VSS	VSS	VCC
W	VCC	VSS	VSS	VSS	DQ4_1	DQ4_3			DQ1_1	DQ1_3	VSS	VSS	VSS	VCC
Y	NU	VCC	VSS	VSS	VSS	VSS			DQ0_1	DQ0_3	VSS	VSS	VCCQ	NU
AA	NC	NU	VCCQ	VSS	VCCQ	VCC			VSS	VSS	VSS	VCCQ	NU	NC
AB	NC	NC	NU									NU	NC	NC

Figure 2-17 BGA-252 ball assignments for quad 8-bit data access

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
B	NC	NC	NC	VCCQ	VSS	VCCQ	VSS	VREFQ	VCC	VSS	VCC	VSS	VCC	NC	NC	NC
C	NC	NC	VSS	VCC	VSS	DQ7_2	DQ7_0			VCCQ	VSS	ENi or NU	ENo or NU	VPP	NC	NC
D	NC	VCC	VSS	VSP	VSP	DQ6_2	DQ6_0			VSS	VSS	VSS	VSS	VSS	VCC	NC
E	NC	VCCQ	VSS	VSP	VSP	DQ5_2	DQ5_0			DBI_2 or NU	R/B0_2	RZQ_2	VSS	VSS	RFU	NC
F	NC	VSS	VSS	VCCQ	VSS	DQ4_2	DQ4_0			DBI_0 or NU	R/B0_0	RZQ_0	VSS	VSS	VSS	NC
G	NC	VCCQ	VSS	VCC	VSS	DQS_2 (DQS_2_t)	DQS_0 (DQS_0_t)			WP_0_n or ODT_0_n	WP_2_n or ODT_2_n	CE1_2_n	CE3_2_n	VSS	VCC	NC
H	NC	VCC	VSS	VCCQ	VSS	DQS_2_c	DQS_0_c			CLE_0	CLE_2	CE1_0_n	CE3_0_n	VSS	RFU	NC
J	NC	VSP	VSP	VSS	DQ3_2	DQ3_0	RE_2_c			RE_0_c	ALE_2	CE0_2_n	CE2_2_n	VSS	VSS	NC
K	NC	VCCQ	VSS	VSS	DQ2_2	DQ2_0	RE_2_n (RE_2_t) or W/R_2_n			RE_0_n (RE_0_t) or W/R_0_n	ALE_0	CE0_0_n	CE2_0_n	VSS	VCC	NC
L	NC	VDDi	VREFQ	VSP	DQ1_2	DQ1_0	WE_2_n or CK_2			WE_0_n or CK_0	DQ0_1	DQ0_3	VSP	VSS	VCCQ	NC
M	NC	VCCQ	VSS	VSP	DQ0_2	DQ0_0	WE_1_n or CK_1			WE_3_n or CK_3	DQ1_1	DQ1_3	VSP	VREFQ	VDDi	NC
N	NC	VCC	VSS	CE2_1_n	CE0_1_n	ALE_1	RE_1_n (RE_1_t) or W/R_1_n			RE_3_n (RE_3_t) or W/R_3_n	DQ2_1	DQ2_3	VSS	VSS	VCCQ	NC
P	NC	VSS	VSS	CE2_3_n	CE0_3_n	ALE_3	RE_1_c			RE_3_c	DQ3_1	DQ3_3	VSS	VSP	VSP	NC
R	NC	RFU	VSS	CE3_1_n	CE1_1_n	CLE_3	CLE_1			DQS_1_c	DQS_3_c	VSS	VCCQ	VSS	VCC	NC
T	NC	VCC	VSS	CE3_3_n	CE1_3_n	WP_3_n or ODT_3_n	WP_1_n or ODT_1_n			DQS_1 (DQS_1_t)	DQS_3 (DQS_3_t)	VSS	VCC	VSS	VCCQ	NC
U	NC	VSS	VSS	VSS	RZQ_1	R/B0_1	DBI_1 or NU			DQ4_1	DQ4_3	VSS	VCCQ	VSS	VSS	NC
V	NC	RFU	VSS	VSS	RZQ_3	R/B0_3	DBI_3 or NU			DQ5_1	DQ5_3	VSP	VSP	VSS	VCCQ	NC
W	NC	VCC	VSS	VSS	VSS	VSS	VSS			DQ6_1	DQ6_3	VSP	VSP	VSS	VCC	NC
Y	NC	NC	VPP	RFU	RFU	VSS	VCCQ			DQ7_1	DQ7_3	VSS	VCC	VSS	NC	NC
AA	NC	NC	NC	VCC	VSS	VCC	VSS	VCC	VREFQ	VSS	VCCQ	VSS	VCCQ	NC	NC	NC
AB	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

Figure 2-18 BGA-316 ball 16 CE_n assignments for quad 8-bit data access

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
B	NC	NC	NC	VCCQ	VSS	VCCQ	VSS	VREFQ	VCC	VSS	VCC	VSS	VCC	NC	NC	NC
C	NC	NC	VSS	VCC	VSS	DQ7_2	DQ7_0			VCCQ	VSS	ENi or NU	ENo or NU	VPP	NC	NC
D	NC	VCC	VSS	VSP	VSP	DQ6_2	DQ6_0			VSS	VSS	VSS	VSS	VSS	VCC	NC
E	NC	VCCQ	VSS	VSP	VSP	DQ5_2	DQ5_0			DBI_2 or NU	R/B0_2	RZQ_2	CE6_2_n	CE7_2_n	RFU	NC
F	NC	VSS	VSS	VCCQ	VSS	DQ4_2	DQ4_0			DBI_0 or NU	R/B0_0	RZQ_0	CE6_0_n	CE7_0_n	VSS	NC
G	NC	VCCQ	VSS	VCC	VSS	DQS_2 (DQS_2_t)	DQS_0 (DQS_0_t)			WP_0_n or ODT_0_n	WP_2_n or ODT_2_n	CE1_2_n	CE3_2_n	CE5_2_n	VCC	NC
H	NC	VCC	VSS	VCCQ	VSS	DQS_2_c	DQS_0_c			CLE_0	CLE_2	CE1_0_n	CE3_0_n	CE5_0_n	RFU	NC
J	NC	VSP	VSP	VSS	DQ3_2	DQ3_0	RE_2_c			RE_0_c	ALE_2	CE0_2_n	CE2_2_n	CE4_2_n	VSS	NC
K	NC	VCCQ	VSS	VSS	DQ2_2	DQ2_0	RE_2_n (RE_2_t) or W/R_2_n			RE_0_n (RE_0_t) or W/R_0_n	ALE_0	CE0_0_n	CE2_0_n	CE4_0_n	VCC	NC
L	NC	VDDi	VREFQ	VSP	DQ1_2	DQ1_0	WE_2_n or CK_2			WE_0_n or CK_0	DQ0_1	DQ0_3	VSP	VSS	VCCQ	NC
M	NC	VCCQ	VSS	VSP	DQ0_2	DQ0_0	WE_1_n or CK_1			WE_3_n or CK_3	DQ1_1	DQ1_3	VSP	VREFQ	VDDi	NC
N	NC	VCC	CE4_1_n	CE2_1_n	CE0_1_n	ALE_1	RE_1_n (RE_1_t) or W/R_1_n			RE_3_n (RE_3_t) or W/R_3_n	DQ2_1	DQ2_3	VSS	VSS	VCCQ	NC
P	NC	VSS	CE4_3_n	CE2_3_n	CE0_3_n	ALE_3	RE_1_c			RE_3_c	DQ3_1	DQ3_3	VSS	VSP	VSP	NC
R	NC	RFU	CE5_1_n	CE3_1_n	CE1_1_n	CLE_3	CLE_1			DQS_1_c	DQS_3_c	VSS	VCCQ	VSS	VCC	NC
T	NC	VCC	CE5_3_n	CE3_3_n	CE1_3_n	WP_3_n or ODT_3_n	WP_1_n or ODT_1_n			DQS_1 (DQS_1_t)	DQS_3 (DQS_3_t)	VSS	VCC	VSS	VCCQ	NC
U	NC	VSS	CE7_1_n	CE6_1_n	RZQ_1	R/B0_1	DBI_1 or NU			DQ4_1	DQ4_3	VSS	VCCQ	VSS	VSS	NC
V	NC	RFU	CE7_1_n	CE6_3_n	RZQ_3	R/B0_3	DBI_3 or NU			DQ5_1	DQ5_3	VSP	VSP	VSS	VCCQ	NC
W	NC	VCC	VSS	VSS	VSS	VSS	VSS			DQ6_1	DQ6_3	VSP	VSP	VSS	VCC	NC
Y	NC	NC	VPP	RFU	RFU	VSS	VCCQ			DQ7_1	DQ7_3	VSS	VCC	VSS	NC	NC
AA	NC	NC	NC	VCC	VSS	VCC	VSS	VCC	VREFQ	VSS	VCCQ	VSS	VCCQ	NC	NC	NC
AB	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

Figure 2-19 BGA-316 ball 32 CE_n assignments for quad 8-bit data access

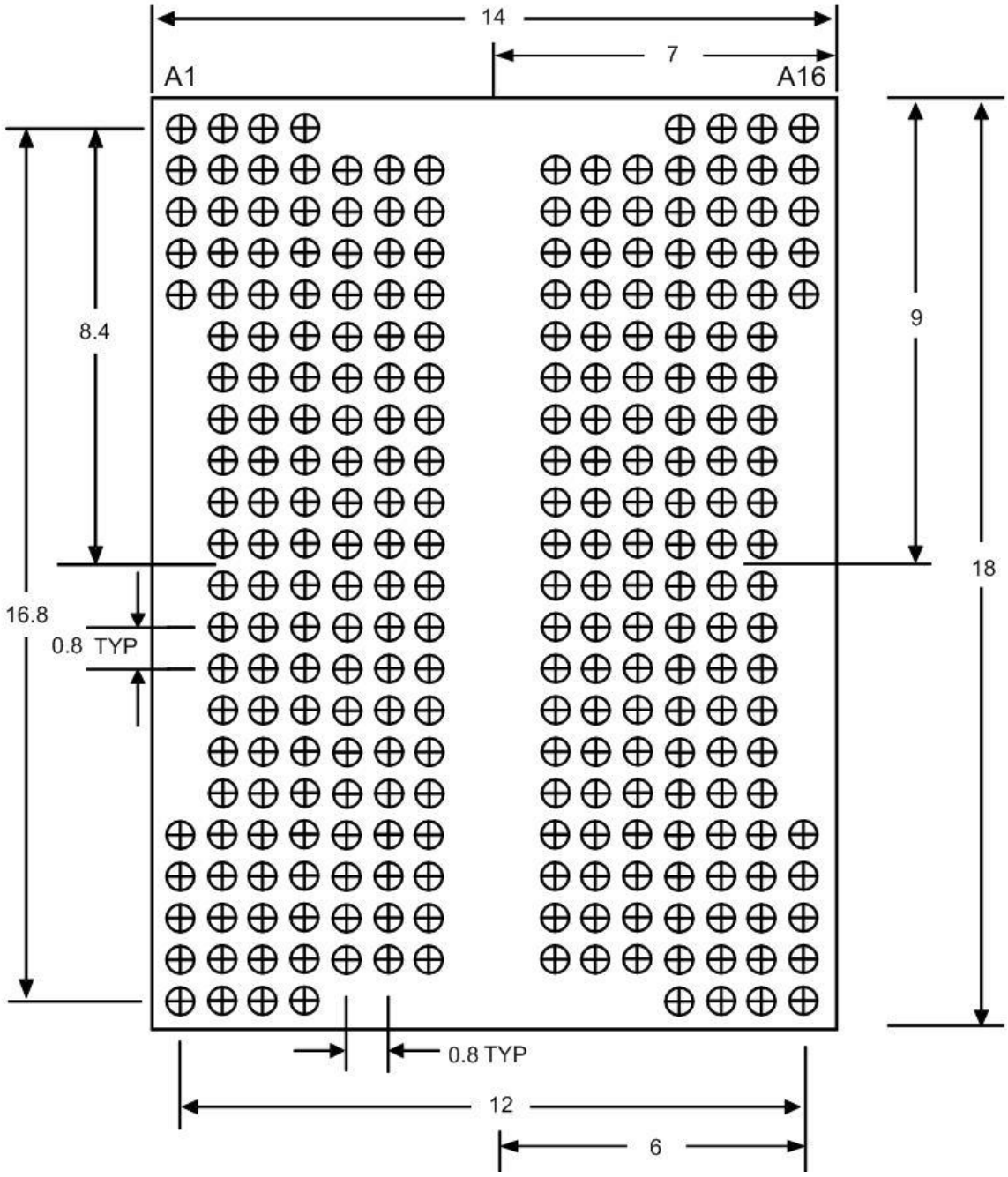


Figure 2-20 BGA-272 and BGA-252 ball spacing requirements (top view, dimensions in millimeters)

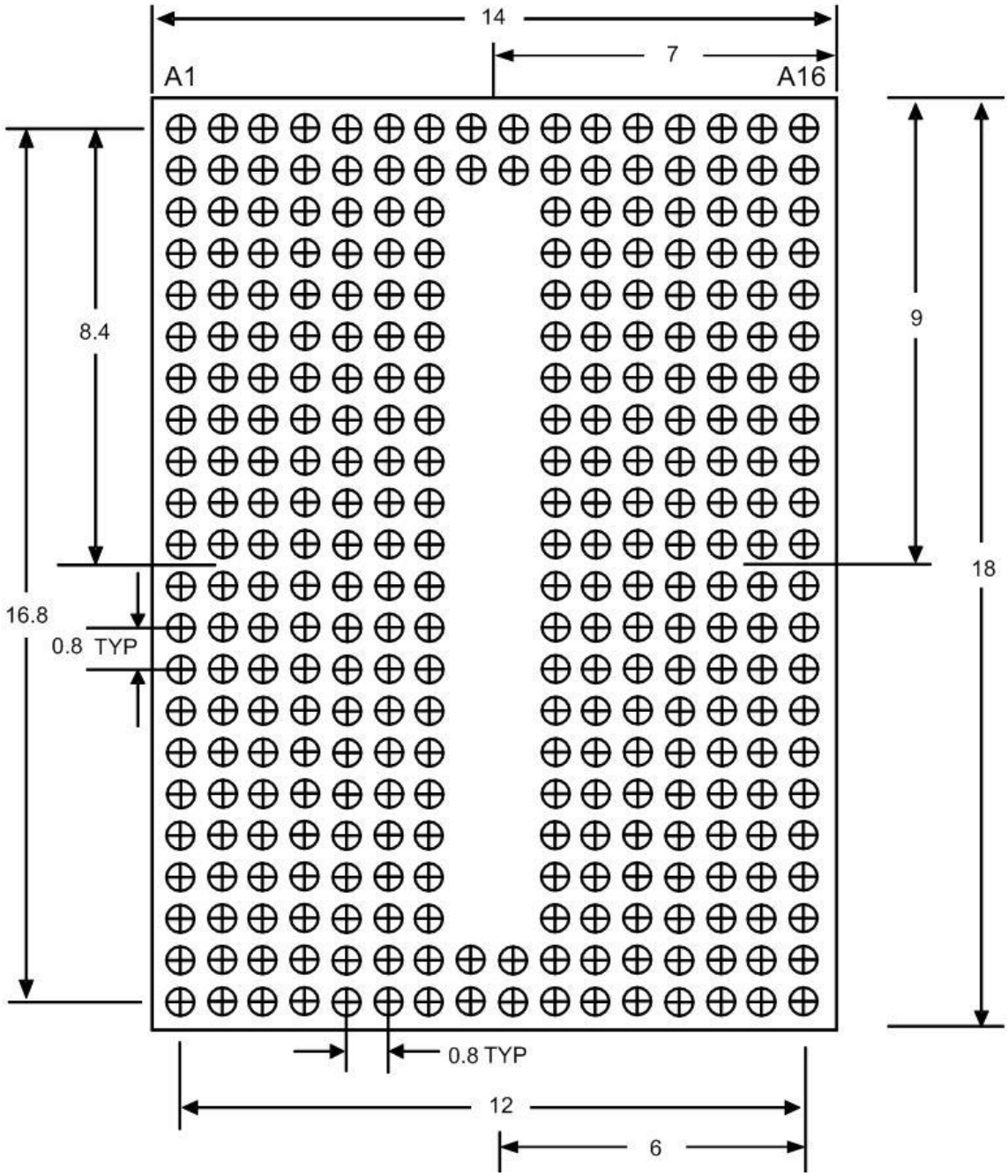


Figure 2-21 BGA-316 ball spacing requirements (top view, dimensions in millimeters)

2.7. BGA-178, BGA-154, and BGA-146 Ball Assignments

Figure 2-22 defines the ball assignments for devices using 178-ball BGA packaging with dual 8-bit data access. Figure 2-23 defines the ball assignments for devices using 154-ball BGA packaging with dual 8-bit data access. Figure 2-24 defines the ball assignments for devices using 146-ball BGA packaging with dual 8-bit data access. Figure 2-25, Figure 2-26, Figure 2-27 define

the ball spacing requirements for the 178-ball, 154-ball and 146-ball BGA packages. The package size for the 178-ball package is 13.5mm x 13.5mm. The package size for the 154-ball package is either 11.5x13.5mm or 12.8x13.5 mm. The package size for 146-ball package is 10x18mm. The 154-ball package removes the outer columns from the 178-ball package resulting in a smaller package size. The 154-ball package ball assignment is also re-enumerated to begin at column 1 (i.e. BGA-178 column 2 becomes BGA-154 column 1). The 146-ball package transposes the rows and columns from the 178-ball package and removes the 2 outer columns on each side. The 146-ball package ball assignment is also re-enumerated to begin at column 1 (i.e. BGA-178 row N becomes BGA-146 column 1). Depending on the data interface selected, balls may have different usages and/or meanings. Refer to for the specific use for each ball in each data interface. ONFI does not support ODT pin. Ball-map showing ODT_*_n/WP_*_n muxing is just as a reference to JEDEC

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	NC	NC	NC	NC								NC	NC	NC	NC
B	NC	NU	NU	NU								NU	NU	NU	NC
C	NC	NU	NU	VCCQ	VSS	VPP	VSS	VCC	VSS	VCCQ	VSS	VCCQ	NU	NU	NC
D	NC	NU	VCCQ	VCC	RFU	VPP	PSL_0 ZQ_0	VREFQ_0	RFU	VSP	VSP	VCC	VCCQ	NU	NC
E	NC	NU	VSS	DQ5_0	VCCQ	DQ7_0	CE1_0_n	CE0_0_n	WP_1_n ODT_1_n	DQ0_1	VCCQ	DQ2_1	VSS	NU	NC
F	NC	NU	VCCQ	DQ4_0	VSS	DQ6_0	CE2_0_n	R/B0_0_n	ALE_1	DQ1_1	VSS	DQ3_1	VCCQ	NU	NC
G		NU	VCC	RE_0_n W/R_0_n	RE_0_c	WE_0_n CLK_0	CE3_0_n	R/B1_0_n	CLE_1	DBI_1 or NU	DQS_1_c	DQS_1_t	VSS	NU	
H															
J		NU	VSS	DQS_0_t	DQS_0_c	DBI_0 or NU	CLE_0	R/B1_1_n	CE3_1_n	WE_1_n CLK_1	RE_1_c	RE_1_n W/R_1_n	VCC	NU	
K	NC	NU	VCCQ	DQ3_0	VSS	DQ1_0	ALE_0	R/B0_1_n	CE2_1_n	DQ6_1	VSS	DQ4_1	VCCQ	NU	NC
L	NC	NU	VSS	DQ2_0	VCCQ	DQ0_0	WP_0_n ODT_0_n	CE0_1_n	CE1_1_n	DQ7_1	VCCQ	DQ5_1	VSS	NU	NC
M	NC	NU	VCCQ	VCC	VSP	VSP	RFU	VREFQ_1	PSL_1 ZQ_1	VPP	RFU	VCC	VCCQ	NU	NC
N	NC	NU	NU	VCCQ	VSS	VCCQ	VSS	VCC	VSS	VPP	VSS	VCCQ	NU	NU	NC
P	NC	NU	NU	NU								NU	NU	NU	NC
R	NC	NC	NC	NC								NC	NC	NC	NC

Figure 2-22 BGA-178 ball assignments for dual 8-bit data access

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC								NC	NC	NC
B	NU	NU	NU								NU	NU	NU
C	NU	NU	VCCQ	VSS	VPP	VSS	VCC	VSS	VCCQ	VSS	VCCQ	NU	NU
D	NU	VCCQ	VCC	RFU	VPP	PSL_0 ZQ_0	VREFQ_0	RFU	VSP	VSP	VCC	VCCQ	NU
E	NU	VSS	DQ5_0	VCCQ	DQ7_0	CE1_0_n	CE0_0_n	WP_1_n ODT_1_n	DQ0_1	VCCQ	DQ2_1	VSS	NU
F	NU	VCCQ	DQ4_0	VSS	DQ6_0	CE2_0_n	R/B0_0_n	ALE_1	DQ1_1	VSS	DQ3_1	VCCQ	NU
G	NU	VCC	RE_0_n W/R_0_n	RE_0_c	WE_0_n CLK_0	CE3_0_n	R/B1_0_n	CLE_1	DBI_1 or NU	DQS_1_c	DQS_1_t	VSS	NU
H													
J	NU	VSS	DQS_0_t	DQS_0_c	DBI_0 or NU	CLE_0	R/B1_1_n	CE3_1_n	WE_1_n CLK_1	RE_1_c	RE_1_n W/R_1_n	VCC	NU
K	NU	VCCQ	DQ3_0	VSS	DQ1_0	ALE_0	R/B0_1_n	CE2_1_n	DQ6_1	VSS	DQ4_1	VCCQ	NU
L	NU	VSS	DQ2_0	VCCQ	DQ0_0	WP_0_n ODT_0_n	CE0_1_n	CE1_1_n	DQ7_1	VCCQ	DQ5_1	VSS	NU
M	NU	VCCQ	VCC	VSP	VSP	RFU	VREFQ_1	PSL_1 ZQ_1	VPP	RFU	VCC	VCCQ	NU
N	NU	NU	VCCQ	VSS	VCCQ	VSS	VCC	VSS	VPP	VSS	VCCQ	NU	NU
P	NU	NU	NU								NU	NU	NU
R	NC	NC	NC								NC	NC	NC

Figure 2-23 BGA-154 ball assignments for dual 8-bit data access

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	NC	NC				NC	NC	NC	NC
B	NU	NU	NU	NU	NU		NU	NU	NU	NU	NU
C	NU	VCCQ	VSS	VCCQ	VSS		VCC	VCCQ	VSS	VCCQ	NU
D	VCCQ	VCC	DQ2_0	DQ3_0	DQS_0_t		RE_0_n W/R_0_n	DQ4_0	DQ5_0	VCC	VCCQ
E	VSS	VSP	VCCQ	VSS	DQS_0_c		RE_0_c	VSS	VCCQ	RFU	VSS
F	VCCQ	VSP	DQ0_0	DQ1_0	DBI_0 or NU		WE_0_n CLK_0	DQ6_0	DQ7_0	VPP	VPP
G	VSS	RFU	WP_0_n ODT_0_n	ALE_0	CLE_0		CE3_0_n	CE2_0_n	CE1_0_n	PSL_0 ZQ_0	VSS
H	VCC	VREFQ_1	CE0_1_n	R/B0_1_n	R/B1_1_n		R/B1_0_n	R/B0_0_n	CE0_0_n	VREFQ_0	VCC
J	VSS	PSL_1 ZQ_1	CE1_1_n	CE2_1_n	CE3_1_n		CLE_1	ALE_1	WP_1_n ODT_1_n	RFU	VSS
K	VPP	VPP	DQ7_1	DQ6_1	WE_1_n CLK_1		DBI_1 or NU	DQ1_1	DQ0_1	VSP	VCCQ
L	VSS	RFU	VCCQ	VSS	RE_1_c		DQS_1_c	VSS	VCCQ	VSP	VSS
M	VCCQ	VCC	DQ5_1	DQ4_1	RE_1_n W/R_1_n		DQS_1_t	DQ3_1	DQ2_1	VCC	VCCQ
N	NU	VCCQ	VSS	VCCQ	VCC		VSS	VCCQ	VSS	VCCQ	NU
P	NU	NU	NU	NU	NU		NU	NU	NU	NU	NU
R	NC	NC	NC	NC				NC	NC	NC	NC

Figure 2-24 BGA-146 ball assignments for dual 8-bit data access

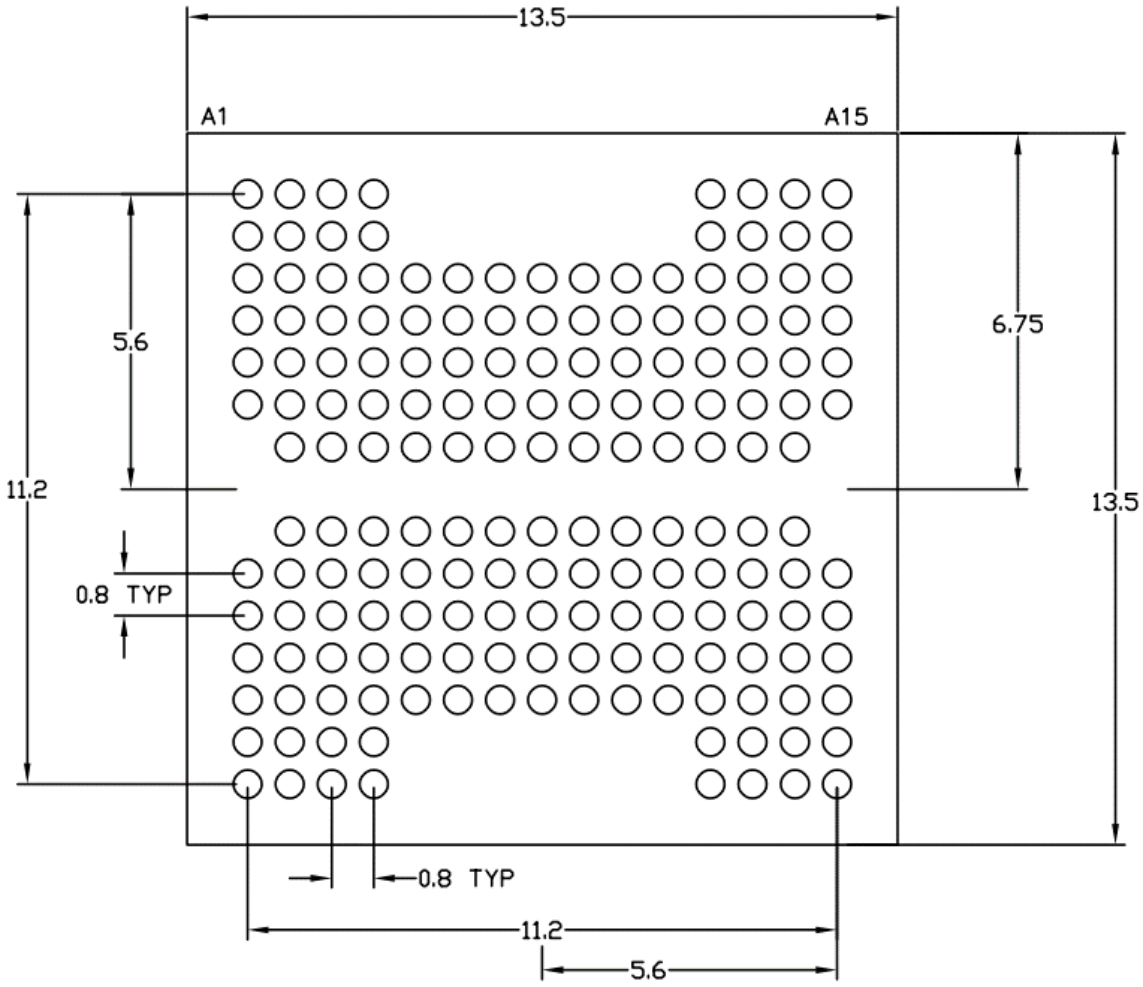


Figure 2-25 BGA-178 ball spacing requirements (top view, dimensions in millimeters)

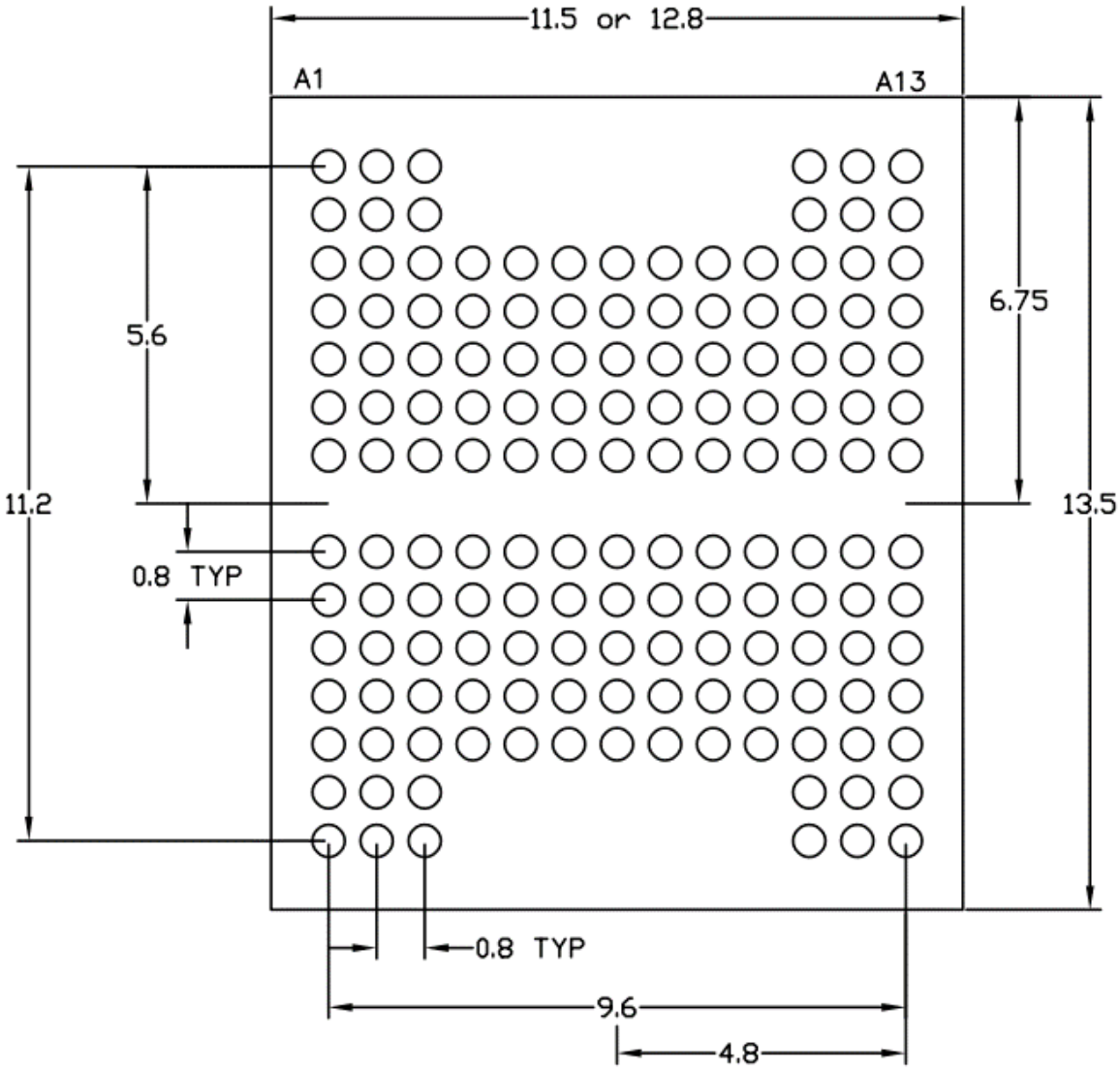


Figure 2-26 BGA-154 ball spacing requirements (top view, dimensions in millimeters)

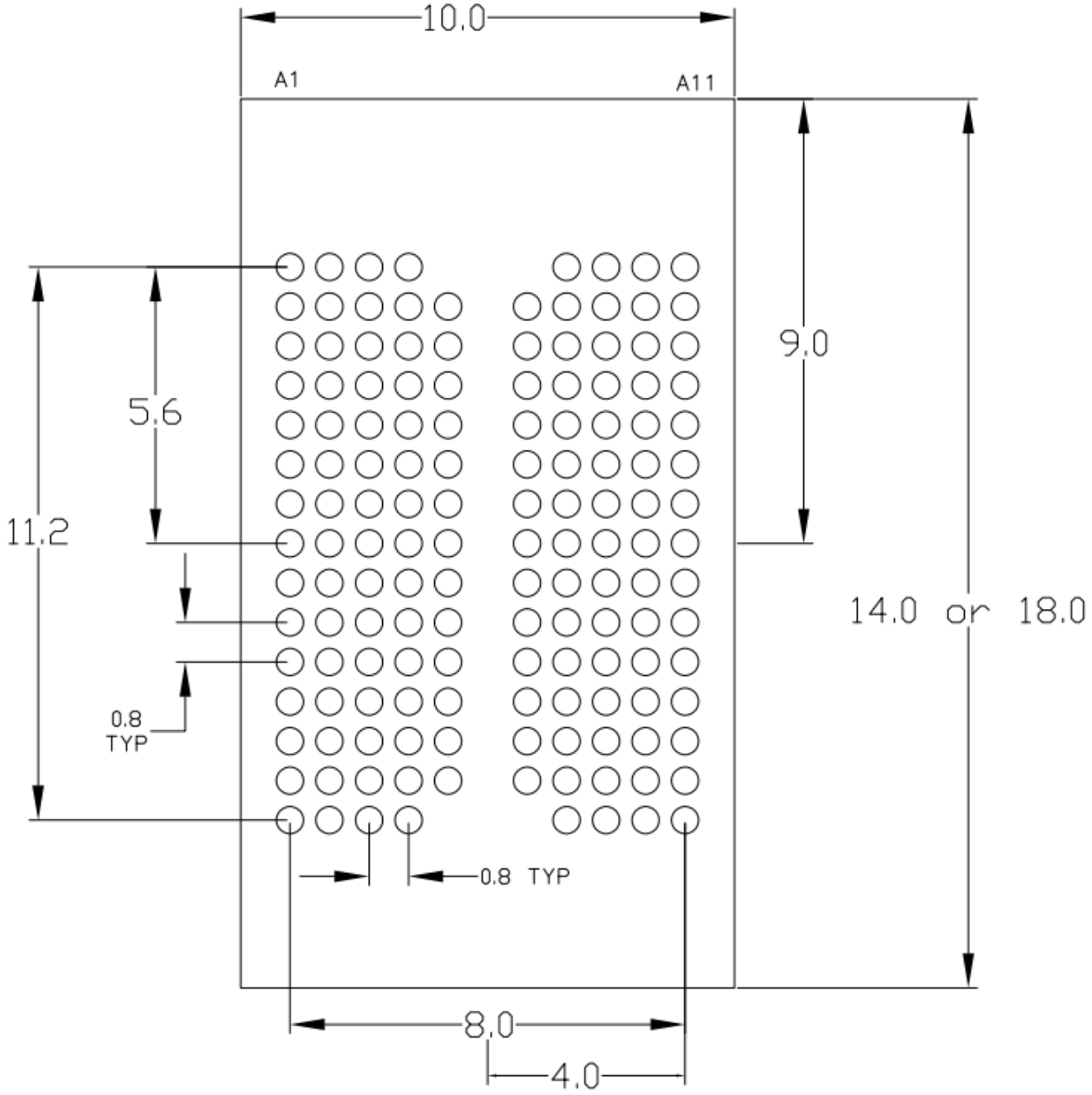


Figure 2-27 BGA-146 ball spacing requirements (top view, dimensions in millimeters)

2.8. Signal Descriptions

Table 2-1 provides the signal descriptions.

Signal Name	Input / Output	Description
R/B_x_n	O	**Ready/Busy** The Ready/Busy signal indicates the target status. When low, the signal indicates that one or more LUN operations are in progress. This signal is an open drain output and requires an external pull-up. See section 2.18 for requirements.
RE_x_n (RE_x_t)	I	**Read Enable (True)** The Read Enable (True) signal enables serial data output. This signal shares the same pin as W/R_x_n in the NV-DDR data interface.
RE_x_c	I	**Read Enable Complement** The Read Enable Complement signal is the complementary signal to Read Enable True, optionally used in the NV-DDR2 NV-DDR3 or NV-LPDDR4 data interface. Specifically, Read Enable Complement has the opposite value of Read Enable True when CE_n is low, i.e., if RE_x_t is high then RE_x_c is low; if RE_x_t is low then RE_x_c is high.
W/R_x_n	I	**Write/Read Direction** The Write/Read Direction signal indicates the owner of the DQ bus and DQS signal in the NV-DDR data interface. This signal shares the same pin as RE_x_n in the SDR, NV-DDR2, and NV-DDR3 data interfaces.
CE_x_n	I	**Chip Enable** The Chip Enable signal selects the target. When Chip Enable is high and the target is in the ready state, the target goes into a low-power standby state. When Chip Enable is low, the target is selected. See section 2.9 for additional requirements.
Vcc	I	**Power** The Vcc signal is the power supply to the device.
VccQ	I	**I/O Power** The VccQ signal is the power supply for input and/or output signals. Refer to section 2.11.1.
Vss	I	**Ground** The Vss signal is the power supply ground.
VssQ	I	**I/O Ground** The VssQ signal is the ground for input and/or output signals. Refer to section 2.11.1.
VREFQ_x	I	**Voltage Reference** This signal is used as an external voltage reference for input and I/O signals when the NV-DDR2 or NV-DDR3 data interface is selected. This signal is not used when the SDR, NV-DDR or NV-LPDDR4 data interfaces are selected.
Vpp	I	**High Voltage Power** The Vpp signal is an optional external high voltage power supply to the device. This high voltage power supply may be used to enhance Erase and Program operations (e.g., improved power efficiency).
CLE_x	I	**Command Latch Enable** The Command Latch Enable signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data). Refer to section 4.3.

Signal Name	Input / Output	Description
ALE_x	I	**Address Latch Enable** The Address Latch Enable signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data). Refer to section 4.3.
WE_x_n	I	**Write Enable** The Write Enable signal controls the latching of commands, addresses, and input data in the SDR data interface. The Write Enable signal controls the latching of commands and addresses in the NV-DDR2 NV-DDR3 or NV-LPDDR4 data interface. Data, commands, and addresses are latched on the rising edge of WE_x_n. This signal shares the same pin as CLK_x in the NV-DDR data interface.
CLK_x	I	**Clock** The Clock signal is used as the clock in the NV-DDR data interface. This signal shares the same pin as WE_x_n in the SDR, NV-DDR2, and NV-DDR3 data interface.
WP_x_n	I	**Write Protect** The Write Protect signal disables Flash array program and erase operations. See section 2.19 for requirements.
IO0_0 – IO7_0 (DQ0_0 – DQ7_0)	I/O	**I/O Port 0, bits 0-7** The I/O port is an 8-bit wide bidirectional port for transferring address, command, and data to and from the device. Also known as DQ0_0 – DQ7_0 for the NV-DDR, NV-DDR2, and NV-DDR3 data interfaces.
DQS (DQS_x_t)	I/O	**Data Strobe (True)** The data strobe signal that indicates the data valid window for the NV-DDR and NV-DDR2 data interfaces.
DBI_x	I/O	**Data Bus Inversion** The is an optional function for NAND device to designate if the DQ signals are inverted by transmitter side or not.
DQS_x_c	I/O	**Data Strobe Complement** The Data Strobe Complement signal is the complementary signal to Data Strobe True, optionally used in the NV-DDR2 NV-DDR3 or NV-LPDDR4 data interface. Specifically, Data Strobe Complement has the opposite value of Data Strobe True when CE_n is low, i.e. if DQS_x_t is high then DQS_x_c is low; if DQS_x_t is low then DQS_x_c is high.
IO8 – IO15	I/O	**I/O Port 0, bits 8-15** These signals are used in a 16-bit wide target configuration. The signals are the upper 8 bits for the 16-bit wide bidirectional port used to transfer data to and from the device. These signals are only used in the SDR data interface.
IO0_1 – IO7_1 (DQ0_1 – DQ7_1)	I/O	**I/O Port 1, bits 0-7** The I/O port is an 8-bit wide bidirectional port for transferring address, command, and data to and from the device. These pins may be used as an additional 8-bit wide bidirectional port for devices that support two independent data buses. Also known as DQ0_1 – DQ7_1 for the NV-DDR, NV-DDR2, and NV-DDR3 data interfaces.
ENo	O	**Enumeration output** The ENo signal is an optional output signal used for CE_n reduction Enumeration. Refer to section 2.20.
ENi	I	**Enumeration input** The ENi signal is an optional input signal used for CE_n reduction Enumeration. Refer to section 2.20.

Signal Name	Input / Output	Description
VSP_x		**Vendor Specific** The function of these signals is defined and specified by the NAND vendor. Devices shall have an internal pull-up or pull-down resistor on these signals to yield ONFI compliant behavior when a signal is not connected by the host. Any VSP signal not used by the NAND vendor shall not be connected internal to the device. The VSP signals shall be treated as NU signals by the user.
R		**Reserved** These pins shall not be connected by the host.
RFT		**Reserved for Test** These pins shall not be connected by the host.
NU		**Not Usable** A pin that is not to be used in normal applications and that may or may not have an internal connection.
NC		**No (internal) connection** A pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device, provided that the voltage applied to this terminal (by means of wiring) does not exceed the highest supply voltage rating of the circuit.
ZQ_x	na	**Reference pin for ZQ calibration** This is used on ZQ calibration and ZQ signal shall be connected to Vss through RZQ resistor

Table 2-1 Signal descriptions

Table 2-2, Table 2-3, and Table 2-5 provide the signal mapping to pin/pad/ball for each package type listed within the ONFI specification. These signal mappings are required if the packages listed in this specification are implemented. The “SDR only” signal mappings apply to packages where the device is not NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 capable. When the device is NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 capable, the “DDR”, “DDR2” or “DDR3” signal mappings shall be used. If a signal is marked as “na” then the corresponding package does not implement that signal. Any signal that does not have an associated number is implicitly numbered “0”. For example, WP_n is equivalent to WP0_n.

Devices may be implemented with other package types and be ONFI compliant if all other ONFI requirements within this specification are satisfied.

Signal Name	M/O/R	TSOP / WSOP SDR x8	TSOP / WSOP NV-DDR x8	TSOP / WSOP SDR x16	LGA SDR x8	LGA SDR x16	BGA-63 SDR x8	BGA-63 NV-DDR x8	BGA-63 SDR x16	BGA-100 SDR x8	BGA-100 NV-DDR x8	BGA-100 NV-DDR2/3 x8
R/B0_n	M	7	7	7	na	E5	C8	C8	C8	na	na	na
R/B1_n	O	6	6	6	na	E7	D8	D8	D8	na	na	na
R/B2_n	O	5	5	5	na	A7	E8	E8	E8	na	na	na
R/B3_n	O	4	4	4	na	OA8	F8	F8	F8	na	na	na
R/B0_0_n	M	na	na	na	E5	na	na	na	na	J6	J6	J6
R/B0_1_n	O	na	na	na	E7	na	na	na	na	H6	H6	H6
R/B1_0_n	O	na	na	na	A7	na	na	na	na	J7	J7	J7
R/B1_1_n	O	na	na	na	OA8	na	na	na	na	H7	H7	H7
RE_0_n (t)	M	8	na	8	C7	C7	D4	na	D4	M6	na	M6
RE_1_n (t)	O	na	na	na	D6	na	na	na	na	L6	na	L6
RE_0_c	na	na	na	na	na	na	na	na	na	na	na	P6
RE_1_c	na	na	na	na	na	na	na	na	na	na	na	N6
W/R_0_n	M	na	8	na	na	na	na	D4	na	na	M6	na
W/R_1_n	O	na	na	na	na	na	na	na	na	na	L6	na
CE0_n	M	9	9	9	na	A5	C6	C6	C6	na	na	na
CE1_n	O	10	10	10	na	C5	D6	D6	D6	na	na	na
CE2_n	O	14	14	14	na	A1	D7	D7	D7	na	na	na
CE3_n	O	15	15	15	na	OA0	E7	E7	E7	na	na	na
CE0_0_n	M	na	na	na	A5	na	na	na	na	K7	K7	K7
CE0_1_n	O	na	na	na	C5	na	na	na	na	K6	K6	K6
CE1_0_n	O	na	na	na	A1	na	na	na	na	K5	K5	K5
CE1_1_n	O	na	na	na	OA0	na	na	na	na	J5	J5	J5
Vcc	M	12	12	12	B6	B6	D3	D3	D3	F2	F2	F2
		37	37	37	M6	M6	G4	G4	G4	F3	F3	F3
										F4	F4	F4
										F5	F5	F5
										F6	F6	F6
										F7	F7	F7
										F8	F8	F8
										F9	F9	F9
VccQ	M	34	34	34	N1	N1	H8	H8	H8	H3	H3	H3
		39	39	39	N7	N7	J6	J6	J6	H8	H8	H8
										L2	L2	L2
										L4	L4	L4
										L7	L7	L7
										L9	L9	L9
										P3	P3	P3
										P8	P8	P8

Signal Name	M/O/R	TSOP / WSOP SDR x8	TSOP / WSOP NV-DDR x8	TSOP / WSOP SDR x16	LGA SDR x8	LGA SDR x16	BGA-63 SDR x8	BGA-63 NV-DDR x8	BGA-63 SDR x16	BGA-100 SDR x8	BGA-100 NV-DDR x8	BGA-100 NV-DDR2/3 x8
Vss	M	13 36	13 36	13 36	B2 F6 L3	B2 F6 L3	C5 F7	C5 F7	C5 F7	G2 G3 G4 G5 G6 G7 G8 G9	G2 G3 G4 G5 G6 G7 G8 G9	G2 G3 G4 G5 G6 G7 G8 G9
VssQ	M	25 48	25 48	25 48	M2 OE8	M2 OE8	K8 K3	K8 K3	K8 K3	H2 H9 L3 L8 M4 M7 P2 P9	H2 H9 L3 L8 M4 M7 P2 P9	H2 H9 L3 L8 M4 M7 P2 P9
VREFQ_0	R	na	na	na	na	na	na	na	na	na	na	H5
VREFQ_1	R	na	na	na	na	na	na	na	na	na	na	H4
VDDi	O	3	3	3	OB8	OB8	na	F3	F3	E9	E9	E9
Vpp	O	2 23	2 23	2 23	na	na	na	na	na	na	na	na
CLE_0	M	16	16	16	A3	A3	D5	D5	D5	M5	M5	M5
CLE_1	O	na	na	na	C3	na	na	na	na	L5	L5	L5
ALE_0	M	17	17	17	C1	C1	C4	C4	C4	K4	K4	K4
ALE_1	O	na	na	na	D2	na	na	na	na	J4	J4	J4
WE_0_n	M	18	na	18	E3	E3	C7	na	C7	P7	na	P7
WE_1_n	O	na	na	na	E1	na	na	na	na	N7	na	N7
CLK_0	M	na	18	na	na	na	na	H7	na	na	P7	na
CLK_1	O	na	na	na	na	na	na	na	na	na	N7	na
WP_0_n	M	19	19	19	F2	F2	C3	C3	C3	E5	E5	E5
WP_1_n	O	na	na	na	G5	na	na	na	na	D5	D5	D5
IO0_0 / DQ0_0	M	29	29	29	G3	G3	H4	H4	H4	K2	K2	K2
IO1_0 / DQ1_0	M	30	30	30	H2	H2	J4	J4	J4	N2	N2	N2
IO2_0 / DQ2_0	M	31	31	31	J3	J3	K4	K4	K4	K3	K3	K3
IO3_0 / DQ3_0	M	32	32	32	K2	K2	K5	K5	K5	N3	N3	N3
IO4_0 / DQ4_0	M	41	41	41	L5	L5	K6	K6	K6	N8	N8	N8
IO5_0 / DQ5_0	M	42	42	42	K6	K6	J7	J7	J7	K8	K8	K8
IO6_0 / DQ6_0	M	43	43	43	J5	J5	K7	K7	K7	N9	N9	N9
IO7_0 / DQ7_0	M	44	44	44	H6	H6	J8	J8	J8	K9	K9	K9

Signal Name	M/O/R	TSOP / WSOP SDR x8	TSOP / WSOP NV-DDR x8	TSOP / WSOP SDR x16	LGA SDR x8	LGA SDR x16	BGA-63 SDR x8	BGA-63 NV-DDR x8	BGA-63 SDR x16	BGA-100 SDR x8	BGA-100 NV-DDR x8	BGA-100 NV-DDR2/3 x8
IO8	M	na	na	26	na	G1	na	na	H3	na	na	na
IO9	M	na	na	27	na	J1	na	na	J3	na	na	na
IO10	M	na	na	28	na	L1	na	na	H5	na	na	na
IO11	M	na	na	33	na	N3	na	na	J5	na	na	na
IO12	M	na	na	40	na	N5	na	na	H6	na	na	na
IO13	M	na	na	45	na	L7	na	na	G6	na	na	na
IO14	M	na	na	46	na	J7	na	na	H7	na	na	na
IO15	M	na	na	47	na	G7	na	na	G7	na	na	na
IO0_1 / DQ0_1	O	na	na	na	G1	na	na	na	na	J2	J2	J2
IO1_1 / DQ1_1	O	na	na	na	J1	na	na	na	na	M2	M2	M2
IO2_1 / DQ2_1	O	na	na	na	L1	na	na	na	na	J3	J3	J3
IO3_1 / DQ3_1	O	na	na	na	N3	na	na	na	na	M3	M3	M3
IO4_1 / DQ4_1	O	na	na	na	N5	na	na	na	na	M8	M8	M8
IO5_1 / DQ5_1	O	na	na	na	L7	na	na	na	na	J8	J8	J8
IO6_1 / DQ6_1	O	na	na	na	J7	na	na	na	na	M9	M9	M9
IO7_1 / DQ7_1	O	na	na	na	G7	na	na	na	na	J9	J9	J9
DQS_0_t	M	na	35	na	na	na	na	J5	na	na	P5	P5
DQS_1_t	O	na	na	na	na	na	na	na	na	na	N5	N5
DQS_0_c	R	na	na	na	na	na	na	na	na	na	na	P4
DQS_1_c	R	na	na	na	na	na	na	na	na	na	na	N4
VSP0_0	O	38	38	38	na	na	G5	G5	G5	E7	E7	E7
VSP1_0	O	35	na	35	na	na	G8	G8	G8	E6	E6	E6
VSP2_0	O	20	20	20	na	na	G3	G3	G3	E4	E4	E4
VSP0_1	O	na	na	na	na	na	na	na	na	D7	D7	D7
VSP1_1	O	na	na	na	na	na	na	na	na	D6	D6	D6
VSP2_1	O	na	na	na	na	na	na	na	na	D4	D4	D4
ENi	O	21	21	21	na	na	na	na	na	K5	K5	K5
ENo	O	22	22	22	na	na	na	na	na	H7	H7	H7
ZQ_0	O	na	na	na	na	na	na	na	na	na	na	D2
ZQ_1	O	na	na	na	na	na	na	na	na	na	na	D9

Table 2-2 Signal mappings: TSOP, LGA, BGA-63 and BGA-100 packages

Signal Name	M/O/R	BGA-132 SDR x8	BGA-132 NV-DDR x8	BGA-132 NV-DDR2/3 x8	BGA-132 NV-LPDDR4 x8	BGA-152 SDR x8	BGA-152 NV-DDR x8	BGA-152 NV-DDR2/3 x8	BGA-152 NV-LPDDR4 x8
R/B0_0_n	M	J4	J4	J4	J4	J5	J5	J5	J5
R/B0_1_n	O	J8	J8	J8	J8	J9	J9	J9	J9
R/B1_0_n	O	J5	J5	J5	J5	J6	J6	J6	J6
R/B1_1_n	O	J7	J7	J7	J7	J8	J8	J8	J8
RE_0_n (t)	M	N5	na	N5	N5	N6	na	N6	N6
RE_1_n (t)	O	E7	na	E7	E7	E8	na	E8	E8
RE_0_c	na	na	na	M7	M7	na	na	M8	M8
RE_1_c	na	na	na	F5	F5	na	na	F6	F6
W/R_0_n	M	na	N5	na	na	na	N6	na	na
W/R_1_n	O	na	E7	na	na	na	E8	na	na
CE0_0_n	M	K4	K4	K4	K4	K5	K5	K5	K5
CE0_1_n	O	H8	H8	H8	H8	H9	H9	H9	H9
CE1_0_n	O	K5	K5	K5	K5	K6	K6	K6	K6
CE1_1_n	O	H7	H7	H7	H7	H8	H8	H8	H8
CE2_0_n	O	L4	L4	L4	H2	L5	L5	L5	H3
CE2_1_n	O	G8	G8	G8	K10	G9	G9	G9	K11
CE3_0_n	O	L5	L5	L5	H3	L6	L6	L6	H4
CE3_1_n	O	G7	G7	G7	K9	G8	G8	G8	K10
Vcc	M	D7	D7	D7	D7	D8	D8	D8	D8
		J3	J3	J3	J3	J4	J4	J4	J4
		J9	J9	J9	J9	J10	J10	J10	J10
		P5	P5	P5	P5	P6	P6	P6	P6
VccQ	M	D2	D2	D2	D2	D3	D3	D3	D3
		D3	D3	D3	D3	D4	D4	D4	D4
		D9	D9	D9	D9	D10	D10	D10	D10
		D10	D10	D10	D10	D11	D11	D11	D11
		G3	G3	G3	G3	G4	G4	G4	G4
		G9	G9	G9	G9	G10	G10	G10	G10
		L3	L3	L3	L3	L4	L4	L4	L4
		L9	L9	L9	L9	L10	L10	L10	L10
		P2	P2	P2	P2	P3	P3	P3	P3
		P3	P3	P3	P3	P4	P4	P4	P4
		P9	P9	P9	P9	P10	P10	P10	P10
		P10	P10	P10	P10	P11	P11	P11	P11
Vss	M	D5	D5	D5	D5	D6	D6	D6	D6
		J2	J2	J2	J2	J3	J3	J3	J3
		J10	J10	J10	J10	J11	J11	J11	J11
		P7	P7	P7	P7	P8	P8	P8	P8

Signal Name	M/O/R	BGA-132 SDR x8	BGA-132 NV-DDR x8	BGA-132 NV-DDR2/3 x8	BGA-132 NV-LPDDR4 x8	BGA-152 SDR x8	BGA-152 NV-DDR x8	BGA-152 NV-DDR2/3 x8	BGA-152 NV-LPDDR4 x8
VssQ	M	E2	E2	E2	E2	E3	E3	E3	E3
		E4	E4	E4	E4	E5	E5	E5	E5
		E8	E8	E8	E8	E9	E9	E9	E9
		E10	E10	E10	E10	E11	E11	E11	E11
		G2	G2	G2	G2	G3	G3	G3	G3
		G10	G10	G10	G10	G11	G11	G11	G11
		L2	L2	L2	L2	L3	L3	L3	L3
		L10	L10	L10	L10	L11	L11	L11	L11
		N2	N2	N2	N2	N3	N3	N3	N3
		N4	N4	N4	N4	N5	N5	N5	N5
		N8	N8	N8	N8	N9	N9	N9	N9
		N10	N10	N10	N10	N11	N11	N11	N11
	O				G8				G9
	O				L5				L6
VREFQ_0	R	na	na	M4	M4	na	na	M5	M5
VREFQ_1	R	na	na	F8	F8	na	na	F9	F9
VDDi	O	K10	K10	K10	K10	K11	K11	K11	K11
Vpp	O	K7	K7	K7	K7	K8	K8	K8	K8
CLE_0	M	L7	L7	L7	L7	L8	L8	L8	L8
CLE_1	O	G5	G5	G5	G5	G6	G6	G6	G6
ALE_0	M	L8	L8	L8	L8	L9	L9	L9	L9
ALE_1	O	G4	G4	G4	G4	G5	G5	G5	G5
WE_0_n	M	M5	na	M5	M5	M6	na	M6	M6
WE_1_n	O	F7	na	F7	F7	F8	na	F8	F8
CLK_0	M	na	M5	na	na	na	M6	na	na
CLK_1	O	na	F7	na	na	na	F8	na	na
WP_0_n	M	K8	K8	K8	K8	K9	K9	K9	K9
WP_1_n	O	H4	H4	H4	H4	H5	H5	H5	H5
IO0_0 / DQ0_0	M	M10	M10	M10	M10	M11	M11	M11	M11
IO1_0 / DQ1_0	M	M9	M9	M9	M9	M10	M10	M10	M10
IO2_0 / DQ2_0	M	N9	N9	N9	N9	N10	N10	N10	N10
IO3_0 / DQ3_0	M	P8	P8	P8	P8	P9	P9	P9	P9
IO4_0 / DQ4_0	M	P4	P4	P4	P4	P5	P5	P5	P5
IO5_0 / DQ5_0	M	N3	N3	N3	N3	N4	N4	N4	N4
IO6_0 / DQ6_0	M	M3	M3	M3	M3	M4	M4	M4	M4
IO7_0 / DQ7_0	M	M2	M2	M2	M2	M3	M3	M3	M3
IO0_1 / DQ0_1	O	F2	F2	F2	F2	F3	F3	F3	F3
IO1_1 / DQ1_1	O	F3	F3	F3	F3	F4	F4	F4	F4
IO2_1 / DQ2_1	O	E3	E3	E3	E3	E4	E4	E4	E4
IO3_1 / DQ3_1	O	D4	D4	D4	D4	D5	D5	D5	D5
IO4_1 / DQ4_1	O	D8	D8	D8	D8	D9	D9	D9	D9
IO5_1 / DQ5_1	O	E9	E9	E9	E9	E10	E10	E10	E10
IO6_1 / DQ6_1	O	F9	F9	F9	F9	F10	F10	F10	F10
IO7_1 / DQ7_1	O	F10	F10	F10	F10	F11	F11	F11	F11

Signal Name	M/O/R	BGA-132 SDR x8	BGA-132 NV-DDR x8	BGA-132 NV-DDR2/3 x8	BGA-132 NV-LPDDR4 x8	BGA-152 SDR x8	BGA-152 NV-DDR x8	BGA-152 NV-DDR2/3 x8	BGA-152 NV-LPDDR4 x8
DQS_0_t	M	na	N7	N7	N7	na	N8	N8	N8
DQS_1_t	O	na	E5	E5	E5	na	E6	E6	E6
DQS_0_c	R	na	na	M8	M8	na	na	M9	M9
DQS_1_c	R	na	na	F4	F4	na	na	F5	F5
VSP0_0	O	na	na	na	na	na	na	na	na
VSP1_0	O	na	na	na	na	na	na	na	na
VSP2_0	O	na	na	na	na	na	na	na	na
VSP0_1	O	na	na	na	na	na	na	na	na
VSP1_1	O	na	na	na	na	na	na	na	na
VSP2_1	O	na	na	na	na	na	na	na	na
VSP0	O	K2	K2	K2	K2	K3	K3	K3	K3
VSP1	O	H10	H10	H10	H10	H11	H11	H11	H11
VSP2	O	K9	K9	K9	K9	K10	K10	K10	K10
ENi	O	H3	H3	H3	H3	H4	H4	H4	H4
ENo	O	H2	H2	H2	H2	H3	H3	H3	H3
ZQ_0	O	na	na	K3	K3	na	na	K4	K4
ZQ_1	O	na	na	H9	H9	na	na	H10	H10
DBI_0	O	na	na	na	L5	na	na	na	L6
DBI_1	O	na	na	na	G7	na	na	na	G8

Table 2-3 Signal mappings: BGA-132, and BGA-152 package

Signal Name	M/O/R	BGA-272 SDR x8	BGA-272 NV-DDR x8	BGA-272 NV-DDR2/3 x8	BGA-272 NV-LPDDR4 x8	BGA-252 SDR x8	BGA-252 NV-DDR x8	BGA-252 NV-DDR2/3 x8	BGA-252 NV-LPDDR4 x8
R/B0_0_n	O	H13	H13	H13	H13	H12	H12	H12	H12
R/B0_1_n	O	R4	R4	R4	R4	R3	R3	R3	R3
R/B0_2_n	O	J13	J13	J13	J13	J12	J12	J12	J12
R/B0_3_n	O	P4	P4	P4	P4	P3	P3	P3	P3
R/B1_0_n	O	H14	H14	H14	H14	H13	H13	H13	H13
R/B1_1_n	O	R3	R3	R3	R3	R2	R2	R2	R2
R/B1_2_n	O	J14	J14	J14	J14	J13	J13	J13	J13
R/B1_3_n	O	P3	P3	P3	P3	P2	P2	P2	P2
RE_0_n (t)	M	K6	na	K6	K6	K5	na	K5	K5
RE_1_n (t)	O	N11	na	N11	N11	N10	na	N10	N10
RE_2_n (t)	O	L6	na	L6	L6	L5	na	L5	L5
RE_3_n (t)	O	M11	na	M11	M11	M10	na	M10	M10

Signal Name	M/O/R	BGA-272 SDR x8	BGA-272 NV-DDR x8	BGA-272 NV-DDR2/3 x8	BGA-272 NV-LPDDR4 x8	BGA-252 SDR x8	BGA-252 NV-DDR x8	BGA-252 NV-DDR2/3 x8	BGA-252 NV-LPDDR4 x8
RE_0_c	O	na	na	K7	K7	na	na	K6	K6
RE_1_c	O	na	na	N10	N10	na	na	N9	N9
RE_2_c	O	na	na	L7	L7	na	na	L6	L6
RE_3_c	O	na	na	M10	M10	na	na	M9	M9
W/R_0_n	M	na	K6	na	na	na	K5	na	na
W/R_1_n	O	na	N11	na	na	na	N10	na	na
W/R_2_n	O	na	L6	na	na	na	L5	na	na
W/R_3_n	O	na	M11	na	na	na	M10	na	na
CE0_0_n	M	K11	K11	K11	K11	K10	K10	K10	K10
CE0_1_n	O	N6	N6	N6	N6	N5	N5	N5	N5
CE0_2_n	O	K10	K10	K10	K10	K9	K9	K9	K9
CE0_3_n	O	N7	N7	N7	N7	N6	N6	N6	N6
CE1_0_n	O	H11	H11	H11	H11	H10	H10	H10	H10
CE1_1_n	O	R6	R6	R6	R6	R5	R5	R5	R5
CE1_2_n	O	J11	J11	J11	J11	J10	J10	J10	J10
CE1_3_n	O	P6	P6	P6	P6	P5	P5	P5	P5
CE2_0_n	O	K13	K13	K13	K13	K12	K12	K12	K12
CE2_1_n	O	N4	N4	N4	N4	N3	N3	N3	N3
CE2_2_n	O	K12	K12	K12	K12	K11	K11	K11	K11
CE2_3_n	O	N5	N5	N5	N5	N4	N4	N4	N4
CE3_0_n	O	H12	H12	H12	H12	H11	H11	H11	H11
CE3_1_n	O	R5	R5	R5	R5	R4	R4	R4	R4
CE3_2_n	O	J12	J12	J12	J12	J11	J11	J11	J11
CE3_3_n	O	P5	P5	P5	P5	P4	P4	P4	P4
Vcc	M	B10	B10	B10	B10	B9	B9	B9	B9
		C14	C14	C14	C14	C13	C13	C13	C13
		D2	D2	D2	D2	D1	D1	D1	D1
		D15	D15	D15	D15	D14	D14	D14	D14
		E2	E2	E2	E2	E1	E1	E1	E1
		K2	K2	K2	K2	K1	K1	K1	K1
		N15	N15	N15	N15	N14	N14	N14	N14
		V15	V15	V15	V15	V14	V14	V14	V14
		W2	W2	W2	W2	W1	W1	W1	W1
		W15	W15	W15	W15	W14	W14	W14	W14
		Y3	Y3	Y3	Y3	Y2	Y2	Y2	Y2
		AA7	AA7	AA7	AA7	AA6	AA6	AA6	AA6

Signal Name	M/O/R	BGA-272 SDR x8	BGA-272 NV-DDR x8	BGA-272 NV-DDR2/3 x8	BGA-272 NV-LPDDR4 x8	BGA-252 SDR x8	BGA-252 NV-DDR x8	BGA-252 NV-DDR2/3 x8	BGA-252 NV-LPDDR4 x8
VccQ	M	B4	B4	B4	B4	B3	B3	B3	B3
		B11	B11	B11	B11	B10	B10	B10	B10
		B13	B13	B13	B13	B12	B12	B12	B12
		C3	C3	C3	C3	C2	C2	C2	C2
		F15	F15	F15	F15	F14	F14	F14	F14
		G2	G2	G2	G2	G1	G1	G1	G1
		G10	G10	G10	G10	G9	G9	G9	G9
		G15	G15	G15	G15	G14	G14	G14	G14
		H2	H2	H2	H2	H1	H1	H1	H1
		R15	R15	R15	R15	R14	R14	R14	R14
		T2	T2	T2	T2	T1	T1	T1	T1
		T7	T7	T7	T7	T6	T6	T6	T6
		T15	T15	T15	T15	T14	T14	T14	T14
		U2	U2	U2	U2	U1	U1	U1	U1
		Y14	Y14	Y14	Y14	Y13	Y13	Y13	Y13
		AA4	AA4	AA4	AA4	AA3	AA3	AA3	AA3
		AA6	AA6	AA6	AA6	AA5	AA5	AA5	AA5
		AA13	AA13	AA13	AA13	AA12	AA12	AA12	AA12

Signal Name	M/O/R	BGA-272 SDR x8	BGA-272 NV-DDR x8	BGA-272 NV-DDR2/3 x8	BGA-272 NV-LPDDR4 x8	BGA-252 SDR x8	BGA-252 NV-DDR x8	BGA-252 NV-DDR2/3 x8	BGA-252 NV-LPDDR4 x8
VSS	M	B5	B5	B5	B5	B4	B4	B4	B4
		B6	B6	B6	B6	B5	B5	B5	B5
		B7	B7	B7	B7	B6	B6	B6	B6
		B12	B12	B12	B12	B11	B11	B11	B11
		C4	C4	C4	C4	C3	C3	C3	C3
		C5	C5	C5	C5	C4	C4	C4	C4
		C10	C10	C10	C10	C9	C9	C9	C9
		C11	C11	C11	C11	C10	C10	C10	C10
		C12	C12	C12	C12	C12	C12	C12	C12
		C13	C13	C13	C13	C12	C12	C12	C12
		D3	D3	D3	D3	D2	D2	D2	D2
		D4	D4	D4	D4	D3	D3	D3	D3
		D5	D5	D5	D5	D4	D4	D4	D4
		D12	D12	D12	D12	D11	D11	D11	D11
		D13	D13	D13	D13	D12	D12	D12	D12
		D14	D14	D14	D14	D13	D13	D13	D13
		E3	E3	E3	E3	E2	E2	E2	E2
		E4	E4	E4	E4	E3	E3	E3	E3
		E5	E5	E5	E5	E4	E4	E4	E4
		E12	E12	E12	E12	E11	E11	E11	E11
		E13	E13	E13	E13	E12	E12	E12	E12
		E14	E14	E14	E14	E13	E13	E13	E13
		E15	E15	E15	E15	E14	E14	E14	E14
		F2	F2	F2	F2	F1	F1	F1	F1
		F3	F3	F3	F3	F2	F2	F2	F2
		F4	F4	F4	F4	F3	F3	F3	F3
		F12	F12	F12	F12	F11	F11	F11	F11
		F13	F13	F13	F13	F12	F12	F12	F12
		F14	F14	F14	F14	F13	F13	F13	F13
		G3	G3	G3	G3	G2	G2	G2	G2
		G4	G4	G4	G4	G3	G3	G3	G3
		H3	H3	H3	H3	H2	H2	H2	H2
		H4	H4	H4	H4	H3	H3	H3	H3
		H7	H7	H7	H7	H6	H6	H6	H6
		H15	H15	H15	H15	H14	H14	H14	H14
		J4	J4	J4	J4	J3	J3	J3	J3
		J5	J5	J5	J5	J4	J4	J4	J4
		J6	J6	J6		J5	J5	J5	
		J7	J7	J7		J6	J6	J6	
		L12	L12	L12	L12	L11	L11	L11	L11

Signal Name	M/O/R	BGA-272 SDR x8	BGA-272 NV-DDR x8	BGA-272 NV-DDR2/3 x8	BGA-272 NV-LPDDR4 x8	BGA-252 SDR x8	BGA-252 NV-DDR x8	BGA-252 NV-DDR2/3 x8	BGA-252 NV-LPDDR4 x8
VSS	M	L13	L13	L13	L13	L12	L12	L12	L12
		L14	L14	L14	L14	L13	L13	L13	L13
		L15	L15	L15	L15	L14	L14	L14	L14
		M2	M2	M2	M2	M1	M1	M1	M1
		M3	M3	M3	M3	M2	M2	M2	M2
		M4	M4	M4	M4	M3	M3	M3	M3
		M5	M5	M5	M5	M4	M4	M4	M4
		P10	P10	P10		P9	P9	P9	
		P11	P11	P11		P10	P10	P10	
		P12	P12	P12	P12	P11	P11	P11	P11
		P13	P13	P13	P13	P12	P12	P12	P12
		R2	R2	R2	R2	R1	R1	R1	R1
		R10	R10	R10	R10	R9	R9	R9	R9
		R13	R13	R13	R13	R12	R12	R12	R12
		R14	R14	R14	R14	R13	R13	R13	R13
		T13	T13	T13	T13	T12	T12	T12	T12
		T14	T14	T14	T14	T14	T14	T14	T14
		U3	U3	U3	U3	U2	U2	U2	U2
		U4	U4	U4	U4	U3	U3	U3	U3
		U5	U5	U5	U5	U4	U4	U4	U4
		U13	U13	U13	U13	U12	U12	U12	U12
		U14	U14	U14	U14	U13	U13	U13	U13
		U15	U15	U15	U15	U14	U14	U14	U14
		V2	V2	V2	V2	V1	V1	V1	V1
		V3	V3	V3	V3	V2	V2	V2	V2
		V4	V4	V4	V4	V3	V3	V3	V3
		V5	V5	V5	V5	V4	V4	V4	V4
		V12	V12	V12	V12	V11	V11	V11	V11
		V13	V13	V13	V13	V12	V12	V12	V12
		V14	V14	V14	V14	V13	V13	V13	V13
		W3	W3	W3	W3	W2	W2	W2	W2
		W4	W4	W4	W4	W3	W3	W3	W3
		W5	W5	W5	W5	W4	W4	W4	W4
		W12	W12	W12	W12	W11	W11	W11	W11
		W13	W13	W13	W13	W12	W12	W12	W12
		W14	W14	W14	W14	W13	W13	W13	W13
		Y4	Y4	Y4	Y4	Y3	Y3	Y3	Y3
		Y5	Y5	Y5	Y5	Y4	Y4	Y4	Y4
		Y6	Y6	Y6	Y6	Y5	Y5	Y5	Y5
		Y7	Y7	Y7	Y7	Y6	Y6	Y6	Y6

Signal Name	M/O/R	BGA-272 SDR x8	BGA-272 NV-DDR x8	BGA-272 NV-DDR2/3 x8	BGA-272 NV-LPDDR4 x8	BGA-252 SDR x8	BGA-252 NV-DDR x8	BGA-252 NV-DDR2/3 x8	BGA-252 NV-LPDDR4 x8
Vss	M	Y12 Y13 AA5 AA10 AA11 AA12	Y12 Y13 AA5 AA10 AA11 AA12	Y12 Y13 AA5 AA10 AA11 AA12	Y12 Y13 AA5 AA10 AA11 AA12	Y11 Y12 AA4 AA9 AA10 AA11	Y11 Y12 AA4 AA9 AA10 AA11	Y11 Y12 AA4 AA9 AA10 AA11	Y11 Y12 AA4 AA9 AA10 AA11
VREFQ	O	L10 L11 M6 M7	L10 L11 M6 M7	L10 L11 M6 M7	L10 L11 M6 M7	L9 L10 M5 M6	L9 L10 M5 M6	L9 L10 M5 M6	L9 L10 M5 M6
VDDi	O	K14 N3	K14 N3	K14 N3	K14 N3	K13 N2	K13 N2	K13 N2	K13 N2
Vpp	O	K15 N2	K15 N2	K15 N2	K15 N2	K14 N1	K14 N1	K14 N1	K14 N1
CLE_0	M	K5	K5	K5	K5	K4	K4	K4	K4
CLE_1	O	N12	N12	N12	N12	N11	N11	N11	N11
CLE_2	O	L5	L5	L5	L5	L4	L4	L4	L4
CLE_3	O	M12	M12	M12	M12	M11	M11	M11	M11
ALE_0	M	K4	K4	K4	K4	K3	K3	K3	K3
ALE_1	O	N13	N13	N13	N13	N12	N12	N12	N12
ALE_2	O	L4	L4	L4	L4	L3	L3	L3	L3
ALE_3	O	M13	M13	M13	M13	M12	M12	M12	M12
WE_0_n	M	H10	na	H10	H10	H9	na	H9	H9
WE_1_n	O	R7	na	R7	R7	R6	na	R6	R6
WE_2_n	O	J10	na	J10	J10	J9	na	J9	J9
WE_3_n	O	P7	na	P7	P7	P6	na	P6	P6
CLK_0	M	na	H10	na	na	na	H9	na	na
CLK_1	O	na	R7	na	na	na	R6	na	na
CLK_2	O	na	J10	na	na	na	J9	na	na
CLK_3	O	na	P7	na	na	na	P6	na	na
WP_0_n	M	K3	K3	K3	K3	K2	K2	K2	K2
WP_1_n	O	N14	N14	N14	N14	N13	N13	N13	N13
WP_2_n	O	L3	L3	L3	L3	L2	L2	L2	L2
WP_3_n	O	M14	M14	M14	M14	M13	M13	M13	M13
IO0_0 / DQ0_0	M	C7	C7	C7	C7	C6	C6	C6	C6
IO1_0 / DQ1_0	M	D7	D7	D7	D7	D6	D6	D6	D6
IO2_0 / DQ2_0	M	E7	E7	E7	E7	E6	E6	E6	E6
IO3_0 / DQ3_0	M	F5	F5	F5	F5	F4	F4	F4	F4
IO4_0 / DQ4_0	M	D11	D11	D11	D11	D10	D10	D10	D10
IO5_0 / DQ5_0	M	E11	E11	E11	E11	E10	E10	E10	E10
IO6_0 / DQ6_0	M	F11	F11	F11	F11	F10	F10	F10	F10
IO7_0 / DQ7_0	M	G12	G12	G12	G12	G11	G11	G11	G11

Signal Name	M/O/R	BGA-272 SDR x8	BGA-272 NV-DDR x8	BGA-272 NV-DDR2/3 x8	BGA-272 NV-LPDDR4 x8	BGA-252 SDR x8	BGA-252 NV-DDR x8	BGA-252 NV-DDR2/3 x8	BGA-252 NV-LPDDR4 x8
IO0_1 / DQ0_1	O	Y10	Y10	Y10	Y10	Y9	Y9	Y9	Y9
IO1_1 / DQ1_1	O	W10	W10	W10	W10	W9	W9	W9	W9
IO2_1 / DQ2_1	O	V10	V10	V10	V10	V9	V9	V9	V9
IO3_1 / DQ3_1	O	U12	U12	U12	U12	U11	U11	U11	U11
IO4_1 / DQ4_1	O	W6	W6	W6	W6	W5	W5	W5	W5
IO5_1 / DQ5_1	O	V6	V6	V6	V6	V5	V5	V5	V5
IO6_1 / DQ6_1	O	U6	U6	U6	U6	U5	U5	U5	U5
IO7_1 / DQ7_1	O	T5	T5	T5	T5	T4	T4	T4	T4
IO0_2 / DQ0_2	O	C6	C6	C6	C6	C5	C5	C5	C5
IO1_2 / DQ1_2	O	D6	D6	D6	D6	D5	D5	D5	D5
IO2_2 / DQ2_2	O	E6	E6	E6	E6	E5	E5	E5	E5
IO3_2 / DQ3_2	O	G5	G5	G5	G5	G4	G4	G4	G4
IO4_2 / DQ4_2	O	D10	D10	D10	D10	D9	D9	D9	D9
IO5_2 / DQ5_2	O	E10	E10	E10	E10	E9	E9	E9	E9
IO6_2 / DQ6_2	O	F10	F10	F10	F10	F9	F9	F9	F9
IO7_2 / DQ7_2	O	G11	G11	G11	G11	G10	G10	G10	G10
IO0_3 / DQ0_3	O	Y11	Y11	Y11	Y11	Y10	Y10	Y10	Y10
IO1_3 / DQ1_3	O	W11	W11	W11	W11	W10	W10	W10	W10
IO2_3 / DQ2_3	O	V11	V11	V11	V11	V10	V10	V10	V10
IO3_3 / DQ3_3	O	T12	T12	T12	T12	T11	T11	T11	T11
IO4_3 / DQ4_3	O	W7	W7	W7	W7	W6	W6	W6	W6
IO5_3 / DQ5_3	O	V7	V7	V7	V7	V6	V6	V6	V6
IO6_3 / DQ6_3	O	U7	U7	U7	U7	U6	U6	U6	U6
IO7_3 / DQ7_3	O	T6	T6	T6	T6	T5	T5	T5	T5

Signal Name	M/O/R	BGA-272 SDR x8	BGA-272 NV-DDR x8	BGA-272 NV-DDR2/3 x8	BGA-272 NV-LPDDR4 x8	BGA-252 SDR x8	BGA-252 NV-DDR x8	BGA-252 NV-DDR2/3 x8	BGA-252 NV-LPDDR4 x8
DQS_0_t	M	na	F7	F7	F7	na	F7	F7	F7
DQS_1_t	O	na	U10	U10	U10	na	U10	U10	U10
DQS_2_t	O	na	F6	F6	F6	na	F6	F6	F6
DQS_3_t	O	na	U11	U11	U11	na	U11	U11	U11
DQS_0_c	O	na	na	G7	G7	na	na	G7	G7
DQS_1_c	O	na	na	T10	T10	na	na	T10	T10
DQS_2_c	O	na	na	G6	G6	na	na	G6	G6
DQS_3_c	O	na	na	T11	T11	na	na	T11	T11
VSP0 (R)	O	H5	H5	H5	H5	H4	H4	H4	H4
VSP1 (R)	O	R12	R12	R12	R12	R11	R11	R11	R11
VSP2 (R)	O	H6	H6	H6	H6	H5	H5	H5	H5
VSP3 (R)	O	R11	R11	R11	R11	R10	R10	R10	R10
VSP4 (R)	O	G13	G13	K14	K14	G12	G12	K13	K13
VSP5 (R)	O	T4	T4	N3	N3	T3	T3	N2	N2
VSP6 (R)	O	G14	G14	J15	J15	G13	G13	J14	J14
VSP7 (R)	O	T3	T3	P2	P2	T2	T2	P1	P1
VSP8 (R)	O	K14	K14			K13	K13		
VSP9 (R)	O	N3	N3			N2	N2		
VSP10 (R)	O	J15	J15			J14	J14		
VSP11 (R)	O	P2	P2			P1	P1		
ENi	O	J2	J2	J2	J2	J1	J1	J1	J1
ENo	O	J3	J3	J3	J3	J2	J2	J2	J2
ZQ_0	O	na	na	G14	G14	na	na	G13	G13
ZQ_1	O	na	na	T3	T3	na	na	T2	T2
ZQ_2	O	na	na	G13	G13	na	na	G12	G12
ZQ_3	O	na	na	T4	T4	na	na	T3	T3
DBI_0	O	na	na	na	J7	na	na	na	J6
DBI_1	O	na	na	na	P10	na	na	na	P9
DBI_2	O	na	na	na	J6	na	na	na	J5
DBI_3	O	na	na	na	P11	na	na	na	P10

Table 2-4 Signal mappings: BGA-272 and BGA-252 package

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Signal Name	M/O/R	BGA-316 SDR x8 16 CE_n	BGA-316 NV-DDR x8 16 CE_n	BGA-316 NV-DDR2/3 x8 16 CE_n	BGA-316 NV-LPDDR4 x8 16 CE_n	BGA-316 SDR x8 32 CE_n	BGA-316 NV-DDR x8 32 CE_n	BGA-316 NV-DDR2/3 x8 32 CE_n	BGA-316 NV-LPDDR4 x8 32 CE_n
R/B0_0_n	O	F11	F11	F11	F11	F11	F11	F11	F11
R/B0_1_n	O	U6	U6	U6	U6	U6	U6	U6	U6
R/B0_2_n	O	E11	E11	E11	E11	E11	E11	E11	E11
R/B0_3_n	O	V6	V6	V6	V6	V6	V6	V6	V6
RE_0_n (t)	M	K10	na	K10	K10	K10	na	K10	K10
RE_1_n (t)	O	N7	na	N7	N7	N7	na	N7	N7
RE_2_n (t)	O	K7	na	K7	K7	K7	na	K7	K7
RE_3_n (t)	O	N10	na	N10	N10	N10	na	N10	N10
RE_0_c	O	na	na	J10	J10	na	na	J10	J10
RE_1_c	O	na	na	P7	P7	na	na	P7	P7
RE_2_c	O	na	na	J7	J7	na	na	J7	J7
RE_3_c	O	na	na	P10	P10	na	na	P10	P10
W/R_0_n	M	na	K10	na	na	na	K10	na	na
W/R_1_n	O	na	N7	na	na	na	N7	na	na
W/R_2_n	O	na	K7	na	na	na	K7	na	na
W/R_3_n	O	na	N10	na	na	na	N10	na	na

Signal Name	M/O/R	BGA-316 SDR x8 16 CE_n	BGA-316 NV-DDR x8 16 CE_n	BGA-316 NV-DDR2/3 x8 16 CE_n	BGA-316 NV-LPDDR4 x8 16 CE_n	BGA-316 SDR x8 32 CE_n	BGA-316 NV-DDR x8 32 CE_n	BGA-316 NV-DDR2/3 x8 32 CE_n	BGA-316 NV-LPDDR4 x8 32 CE_n
CE0_0_n	M	K12	K12	K12	K12	K12	K12	K12	K12
CE0_1_n	O	N5	N5	N5	N5	N5	N5	N5	N5
CE0_2_n	O	J12	J12	J12	J12	J12	J12	J12	J12
CE0_3_n	O	P5	P5	P5	P5	P5	P5	P5	P5
CE1_0_n	O	H12	H12	H12	H12	H12	H12	H12	H12
CE1_1_n	O	R5	R5	R5	R5	R5	R5	R5	R5
CE1_2_n	O	G12	G12	G12	G12	G12	G12	G12	G12
CE1_3_n	O	T5	T5	T5	T5	T5	T5	T5	T5
CE2_0_n	O	K13	K13	K13	K13	K13	K13	K13	K13
CE2_1_n	O	N4	N4	N4	N4	N4	N4	N4	N4
CE2_2_n	O	J13	J13	J13	J13	J13	J13	J13	J13
CE2_3_n	O	P4	P4	P4	P4	P4	P4	P4	P4
CE3_0_n	O	H13	H13	H13	H13	H13	H13	H13	H13
CE3_1_n	O	R4	R4	R4	R4	R4	R4	R4	R4
CE3_2_n	O	G13	G13	G13	G13	G13	G13	G13	G13
CE3_3_n	O	T4	T4	T4	T4	T4	T4	T4	T4
CE4_0_n	O	na	na	na	na	K14	K14	K14	K14
CE4_1_n	O	na	na	na	na	N3	N3	N3	N3
CE4_2_n	O	na	na	na	na	J14	J14	J14	J14
CE4_3_n	O	na	na	na	na	P3	P3	P3	P3
CE5_0_n	O	na	na	na	na	H14	H14	H14	H14
CE5_1_n	O	na	na	na	na	R3	R3	R3	R3
CE5_2_n	O	na	na	na	na	G14	G14	G14	G14
CE5_3_n	O	na	na	na	na	T3	T3	T3	T3
CE6_0_n	O	na	na	na	na	F13	F13	F13	F13
CE6_1_n	O	na	na	na	na	U4	U4	U4	U4
CE6_2_n	O	na	na	na	na	E13	E13	E13	E13
CE6_3_n	O	na	na	na	na	V4	V4	V4	V4
CE7_0_n	O	na	na	na	na	F14	F14	F14	F14
CE7_1_n	O	na	na	na	na	U3	U3	U3	U3
CE7_2_n	O	na	na	na	na	E14	E14	E14	E14
CE7_3_n	O	na	na	na	na	V3	V3	V3	V3

Signal Name	M/O/R	BGA-316 SDR x8 16 CE_n	BGA-316 NV-DDR x8 16 CE_n	BGA-316 NV-DDR2/3 x8 16 CE_n	BGA-316 NV-LPDDR4 x8 16 CE_n	BGA-316 SDR x8 32 CE_n	BGA-316 NV-DDR x8 32 CE_n	BGA-316 NV-DDR2/3 x8 32 CE_n	BGA-316 NV-LPDDR4 x8 32 CE_n
Vcc	M	B9	B9	B9	B9	B9	B9	B9	B9
		B11	B11	B11	B11	B11	B11	B11	B11
		B13	B13	B13	B13	B13	B13	B13	B13
		C4	C4	C4	C4	C4	C4	C4	C4
		D2	D2	D2	D2	D2	D2	D2	D2
		D15	D15	D15	D15	D15	D15	D15	D15
		G4	G4	G4	G4	G4	G4	G4	G4
		G15	G15	G15	G15	G15	G15	G15	G15
		H2	H2	H2	H2	H2	H2	H2	H2
		K15	K15	K15	K15	K15	K15	K15	K15
		N2	N2	N2	N2	N2	N2	N2	N2
		R15	R15	R15	R15	R15	R15	R15	R15
		T2	T2	T2	T2	T2	T2	T2	T2
		T13	T13	T13	T13	T13	T13	T13	T13
		W2	W2	W2	W2	W2	W2	W2	W2
		W15	W15	W15	W15	W15	W15	W15	W15
		Y13	Y13	Y13	Y13	Y13	Y13	Y13	Y13
		AA4	AA4	AA4	AA4	AA4	AA4	AA4	AA4
		AA6	AA6	AA6	AA6	AA6	AA6	AA6	AA6
		AA8	AA8	AA8	AA8	AA8	AA8	AA8	AA8
VccQ	M	B4	B4	B4	B4	B4	B4	B4	B4
		B6	B6	B6	B6	B6	B6	B6	B6
		C10	C10	C10	C10	C10	C10	C10	C10
		E2	E2	E2	E2	E2	E2	E2	E2
		F4	F4	F4	F4	F4	F4	F4	F4
		G2	G2	G2	G2	G2	G2	G2	G2
		H4	H4	H4	H4	H4	H4	H4	H4
		K2	K2	K2	K2	K2	K2	K2	K2
		L15	L15	L15	L15	L15	L15	L15	L15
		M2	M2	M2	M2	M2	M2	M2	M2
		N15	N15	N15	N15	N15	N15	N15	N15
		R13	R13	R13	R13	R13	R13	R13	R13
		T15	T15	T15	T15	T15	T15	T15	T15
		U13	U13	U13	U13	U13	U13	U13	U13
		V15	V15	V15	V15	V15	V15	V15	V15
		Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
		AA11	AA11	AA11	AA11	AA11	AA11	AA11	AA11
		AA13	AA13	AA13	AA13	AA13	AA13	AA13	AA13

Signal Name	M/O/R	BGA-316 SDR x8 16 CE_n	BGA-316 NV-DDR x8 16 CE_n	BGA-316 NV-DDR2/3 x8 16 CE_n	BGA-316 NV-LPDDR4 x8 16 CE_n	BGA-316 SDR x8 32 CE_n	BGA-316 NV-DDR x8 32 CE_n	BGA-316 NV-DDR2/3 x8 32 CE_n	BGA-316 NV-LPDDR4 x8 32 CE_n
VSS	M	B5	B5	B5	B5	B5	B5	B5	B5
		B7	B7	B7	B7	B7	B7	B7	B7
		B10	B10	B10	B10	B10	B10	B10	B10
		B12	B12	B12	B12	B12	B12	B12	B12
		C3	C3	C3	C3	C3	C3	C3	C3
		C5	C5	C5	C5	C5	C5	C5	C5
		C11	C11	C11	C11	C11	C11	C11	C11
		D3	D3	D3	D3	D3	D3	D3	D3
		D10	D10	D10	D10	D10	D10	D10	D10
		D11	D11	D11	D11	D11	D11	D11	D11
		D12	D12	D12	D12	D12	D12	D12	D12
		D13	D13	D13	D13	D13	D13	D13	D13
		D14	D14	D14	D14	D14	D14	D14	D14
		E3	E3	E3	E3	E3	E3	E3	E3
		E10	E10	E10		E10	E10	E10	
		E13	E13	E13	E13	F2	F2	F2	F2
		E14	E14	E14	E14	F3	F3	F3	F3
		F2	F2	F2	F2	F5	F5	F5	F5
		F3	F3	F3	F3	F10	F10	F10	
		F5	F5	F5	F5	F15	F15	F15	F15
		F10	F10	F10		G3	G3	G3	G3
		F13	F13	F13	F13	G5	G5	G5	G5
		F14	F14	F14	F14	H3	H3	H3	H3
		F15	F15	F15	F15	H5	H5	H5	H5
		G3	G3	G3	G3	J4	J4	J4	J4
		G5	G5	G5	G5	J15	J15	J15	J15
		G14	G14	G14	G14	K3	K3	K3	K3
		H3	H3	H3	H3	K4	K4	K4	K4
		H5	H5	H5	H5	L14	L14	L14	L14
		H14	H14	H14	H14	M3	M3	M3	M3
		J4	J4	J4	J4	N13	N13	N13	N13
		J14	J14	J14	J14	N14	N14	N14	N14
		J15	J15	J15	J15	P2	P2	P2	P2
		K3	K3	K3	K3	P13	P13	P13	P13
		K4	K4	K4	K4	R12	R12	R12	R12
		K14	K14	K14	K14	R14	R14	R14	R14
		L14	L14	L14	L14	T12	T12	T12	T12
		M3	M3	M3	M3	T14	T14	T14	T14
		N3	N3	N3	N3	U2	U2	U2	U2
		N13	N13	N13	N13	U7	U7	U7	

Signal Name	M/O/R	BGA-316 SDR x8 16 CE_n	BGA-316 NV-DDR x8 16 CE_n	BGA-316 NV-DDR2/3 x8 16 CE_n	BGA-316 NV-LPDDR4 x8 16 CE_n	BGA-316 SDR x8 32 CE_n	BGA-316 NV-DDR x8 32 CE_n	BGA-316 NV-DDR2/3 x8 32 CE_n	BGA-316 NV-LPDDR4 x8 32 CE_n
Vss	M	N14 P2 P3 P13 R3 R12 R14 T3 T12 T13 U2 U3 U4 U7 U12 U14 U15 V3 V4 V7 V14 W3 W4 W5 W6 W7 W14 Y6 Y12 Y14 AA5 AA7 AA10 AA12	N14 P2 P3 P13 R3 R12 R14 T3 T12 T13 U2 U3 U4 U7 U12 U14 U15 V3 V4 V7 V14 W3 W4 W5 W6 W7 W14 Y6 Y12 Y14 AA5 AA7 AA10 AA12	N14 P2 P3 P13 R3 R12 R14 T3 T12 T13 U2 U3 U4 U7 U12 U14 U15 V3 V4 V7 V14 W3 W4 W5 W6 W7 W14 Y6 Y12 Y14 AA5 AA7 AA10 AA12	N14 P2 P3 P13 R3 R12 R14 T3 T12 T13 U2 U3 U4 U12 U14 U15 V3 V4 V14 W3 W4 W5 W6 W7 W14 Y6 Y12 Y14 AA5 AA7 AA10 AA12	U12 U14 U15 V7 V14 W3 W4 W5 W6 W7 W14 Y6 Y12 Y14 AA5 AA7 AA10 AA12	U12 U14 U15 V7 V14 W3 W4 W5 W6 W7 W14 Y6 Y12 Y14 AA5 AA7 AA10 AA12	U12 U14 U15 V7 V14 W3 W4 W5 W6 W7 W14 Y6 Y12 Y14 AA5 AA7 AA10 AA12	U12 U14 U15 V14 W3 W4 W5 W6 W7 W14 Y6 Y12 Y14 AA5 AA7 AA10 AA12
VREFQ	O	L3 M14	L3 M14	L3 M14	L3 M14	L3 M14	L3 M14	L3 M14	L3 M14
VDDi	O	L2 M15	L2 M15	L2 M15	L2 M15	L2 M15	L2 M15	L2 M15	L2 M15
Vpp	O	C14 Y3	C14 Y3	C14 Y3	C14 Y3	C14 Y3	C14 Y3	C14 Y3	C14 Y3
CLE_0 CLE_1 CLE_2 CLE_3	M O O O	H10 R7 H11 R6	H10 R7 H11 R6	H10 R7 H11 R6	H10 R7 H11 R6	H10 R7 H11 R6	H10 R7 H11 R6	H10 R7 H11 R6	H10 R7 H11 R6

Signal Name	M/O/R	BGA-316 SDR x8 16 CE_n	BGA-316 NV-DDR x8 16 CE_n	BGA-316 NV-DDR2/3 x8 16 CE_n	BGA-316 NV-LPDDR4 x8 16 CE_n	BGA-316 SDR x8 32 CE_n	BGA-316 NV-DDR x8 32 CE_n	BGA-316 NV-DDR2/3 x8 32 CE_n	BGA-316 NV-LPDDR4 x8 32 CE_n
ALE_0	M	K11	K11	K11	K11	K11	K11	K11	K11
ALE_1	O	N6	N6	N6	N6	N6	N6	N6	N6
ALE_2	O	J11	J11	J11	J11	J11	J11	J11	J11
ALE_3	O	P6	P6	P6	P6	P6	P6	P6	P6
WE_0_n	M	L10	na	L10	L10	L10	na	L10	L10
WE_1_n	O	M7	na	M7	M7	M7	na	M7	M7
WE_2_n	O	L7	na	L7	L7	L7	na	L7	L7
WE_3_n	O	M10	na	M10	M10	M10	na	M10	M10
CLK_0	M	na	L10	na	na	na	L10	na	na
CLK_1	O	na	M7	na	na	na	M7	na	na
CLK_2	O	na	L7	na	na	na	L7	na	na
CLK_3	O	na	M10	na	na	na	M10	na	na
WP_0_n	M	G10	G10	G10	G10	G10	G10	G10	G10
WP_1_n	O	T7	T7	T7	T7	T7	T7	T7	T7
WP_2_n	O	G11	G11	G11	G11	G11	G11	G11	G11
WP_3_n	O	T6	T6	T6	T6	T6	T6	T6	T6
IO0_0 / DQ0_0	M	M6	M6	M6	M6	M6	M6	M6	M6
IO1_0 / DQ1_0	M	L6	L6	L6	L6	L6	L6	L6	L6
IO2_0 / DQ2_0	M	K6	K6	K6	K6	K6	K6	K6	K6
IO3_0 / DQ3_0	M	J6	J6	J6	J6	J6	J6	J6	J6
IO4_0 / DQ4_0	M	F7	F7	F7	F7	F7	F7	F7	F7
IO5_0 / DQ5_0	M	E7	E7	E7	E7	E7	E7	E7	E7
IO6_0 / DQ6_0	M	D7	D7	D7	D7	D7	D7	D7	D7
IO7_0 / DQ7_0	M	C7	C7	C7	C7	C7	C7	C7	C7
IO0_1 / DQ0_1	O	L11	L11	L11	L11	L11	L11	L11	L11
IO1_1 / DQ1_1	O	M11	M11	M11	M11	M11	M11	M11	M11
IO2_1 / DQ2_1	O	N11	N11	N11	N11	N11	N11	N11	N11
IO3_1 / DQ3_1	O	P11	P11	P11	P11	P11	P11	P11	P11
IO4_1 / DQ4_1	O	U10	U10	U10	U10	U10	U10	U10	U10
IO5_1 / DQ5_1	O	V10	V10	V10	V10	V10	V10	V10	V10
IO6_1 / DQ6_1	O	W10	W10	W10	W10	W10	W10	W10	W10
IO7_1 / DQ7_1	O	Y10	Y10	Y10	Y10	Y10	Y10	Y10	Y10
IO0_2 / DQ0_2	O	M5	M5	M5	M5	M5	M5	M5	M5
IO1_2 / DQ1_2	O	L5	L5	L5	L5	L5	L5	L5	L5
IO2_2 / DQ2_2	O	K5	K5	K5	K5	K5	K5	K5	K5
IO3_2 / DQ3_2	O	J5	J5	J5	J5	J5	J5	J5	J5
IO4_2 / DQ4_2	O	F6	F6	F6	F6	F6	F6	F6	F6
IO5_2 / DQ5_2	O	E6	E6	E6	E6	E6	E6	E6	E6
IO6_2 / DQ6_2	O	D6	D6	D6	D6	D6	D6	D6	D6
IO7_2 / DQ7_2	O	C6	C6	C6	C6	C6	C6	C6	C6

Signal Name	M/O/R	BGA-316 SDR x8 16 CE_n	BGA-316 NV-DDR x8 16 CE_n	BGA-316 NV-DDR2/3 x8 16 CE_n	BGA-316 NV-LPDDR4 x8 16 CE_n	BGA-316 SDR x8 32 CE_n	BGA-316 NV-DDR x8 32 CE_n	BGA-316 NV-DDR2/3 x8 32 CE_n	BGA-316 NV-LPDDR4 x8 32 CE_n
IO0_3 / DQ0_3	O	L12	L12	L12	L12	L12	L12	L12	L12
IO1_3 / DQ1_3	O	M12	M12	M12	M12	M12	M12	M12	M12
IO2_3 / DQ2_3	O	N12	N12	N12	N12	N12	N12	N12	N12
IO3_3 / DQ3_3	O	P12	P12	P12	P12	P12	P12	P12	P12
IO4_3 / DQ4_3	O	U11	U11	U11	U11	U11	U11	U11	U11
IO5_3 / DQ5_3	O	V11	V11	V11	V11	V11	V11	V11	V11
IO6_3 / DQ6_3	O	W11	W11	W11	W11	W11	W11	W11	W11
IO7_3 / DQ7_3	O	Y11	Y11	Y11	Y11	Y11	Y11	Y11	Y11

Signal Name	M/O/R	BGA-316 SDR x8 16 CE_n	BGA-316 NV-DDR x8 16 CE_n	BGA-316 NV-DDR2/3 x8 16 CE_n	BGA-316 NV-LPDDR4 x8 16 CE_n	BGA-316 SDR x8 32 CE_n	BGA-316 NV-DDR x8 32 CE_n	BGA-316 NV-DDR2/3 x8 32 CE_n	BGA-316 NV-LPDDR4 x8 32 CE_n
DQS_0_t	M	G7	G7	G7	G7	na	G7	G7	G7
DQS_1_t	O	T10	T10	T10	T10	na	T10	T10	T10
DQS_2_t	O	G6	G6	G6	G6	na	G6	G6	G6
DQS_3_t	O	T11	T11	T11	T11	na	T11	T11	T11
DQS_0_c	O	na	na	H7	H7	na	na	H7	H7
DQS_1_c	O	na	na	R10	R10	na	na	R10	R10
DQS_2_c	O	na	na	H6	H6	na	na	H6	H6
DQS_3_c	O	na	na	R11	R11	na	na	R11	R11
VSP0 (R)	O	D4	D4	D4	D4	D4	D4	D4	D4
VSP1 (R)	O	W13	W13	W13	W13	W13	W13	W13	W13
VSP2 (R)	O	D5	D5	D5	D5	D5	D5	D5	D5
VSP3 (R)	O	V13	V13	V13	V13	V13	V13	V13	V13
VSP4 (R)	O	E5	E5	E5	E5	E5	E5	E5	E5
VSP5 (R)	O	V12	V12	V12	V12	V12	V12	V12	V12
VSP6 (R)	O	E4	E4	E4	E4	E4	E4	E4	E4
VSP7 (R)	O	W12	W12	W12	W12	W12	W12	W12	W12
VSP8 (R)	O	E12	E12	E12	E12	E12	E12	E12	E12
VSP9 (R)	O	V5	V5	V5	V5	V5	V5	V5	V5
VSP10 (R)	O	F12	F12	F12	F12	F12	F12	F12	F12
VSP11 (R)	O	U5	U5	U5	U5	U5	U5	U5	U5
VSP12 (R)	O	P15	P15	P15	P15	P15	P15	P15	P15
VSP13 (R)	O	M4	M4	M4	M4	M4	M4	M4	M4
VSP14 (R)	O	P14	P14	P14	P14	P14	P14	P14	P14
VSP15 (R)	O	L4	L4	L4	L4	L4	L4	L4	L4
VSP16 (R)	O	M13	M13	M13	M13	M13	M13	M13	M13
VSP17 (R)	O	J3	J3	J3	J3	J3	J3	J3	J3
VSP18 (R)	O	L13	L13	L13	L13	L13	L13	L13	L13
VSP19 (R)	O	J2	J2	J2	J2	J2	J2	J2	J2
ENi	O	C12	C12	C12	C12	C12	C12	C12	C12
ENo	O	C13	C13	C13	C13	C13	C13	C13	C13
ZQ_0	O	na	na	F12	F12	na	na	F12	F12
ZQ_1	O	na	na	U5	U5	na	na	U5	U5
ZQ_2	O	na	na	E12	E12	na	na	E12	E12
ZQ_3	O	na	na	V5	V5	na	na	V5	V5
DBI_0	O	na	na	na	F10	na	na	na	F10
DBI_1	O	na	na	na	U7	na	na	na	U7
DBI_2	O	na	na	na	E10	na	na	na	E10
DBI_3	O	na	na	na	V7	na	na	na	V7

Table 2-5 Signal mappings: BGA-316 packages

Signal Name	M/O/R	BGA-178 SDR x8	BGA-178 NV-DDR x8	BGA-178 NV-DDR2/3 x8	BGA-178 NV-LPDDR4 x8	BGA-154 SDR x8	BGA-154 NV-DDR x8	BGA-154 NV-DDR2/3 x8	BGA-154 NV-LPDDR4 x8	BGA-146 SDR x8	BGA-146 NV-DDR x8	BGA-146 NV-DDR2/3 x8	BGA-146 NV-LPDDR4 x8
R/B0_0_n	M	F8	F8	F8	F8	F7	F7	F7	F7	H8	H8	H8	H8
R/B0_1_n	O	K8	K8	K8	K8	K7	K7	K7	K7	H4	H4	H4	H4
R/B1_0_n	O	G8	G8	G8	G8	G7	G7	G7	G7	H7	H7	H7	H7
R/B1_1_n	O	J8	J8	J8	J8	J7	J7	J7	J7	H5	H5	H5	H5
RE_0_n (t)	M	G4	na	G4	G4	G3	na	G3	G3	D7	na	D7	D7
RE_1_n (t)	O	J12	na	J12	J12	J11	na	J11	J11	M5	na	M5	M5
RE_0_c	O	na	na	G5	G5	na	na	G4	G4	na	na	E7	E7
RE_1_c	O	na	na	J11	J11	na	na	J10	J10	na	na	L5	L5
W/R_0_n	M	na	G4	na	na	na	G3	na	na	na	D7	na	na
W/R_1_n	O	na	J12	na	na	na	J11	na	na	na	M5	na	na
CE0_0_n	M	E8	E8	E8	E8	E7	E7	E7	E7	H9	H9	H9	H9
CE0_1_n	O	L8	L8	L8	L8	L7	L7	L7	L7	H3	H3	H3	H3
CE1_0_n	O	E7	E7	E7	E7	E6	E6	E6	E6	G9	G9	G9	G9
CE1_1_n	O	L9	L9	L9	L9	L8	L8	L8	L8	J3	J3	J3	J3
CE2_0_n	O	F7	F7	F7	F7	F6	F6	F6	F6	G8	G8	G8	G8
CE2_1_n	O	K9	K9	K9	K9	K8	K8	K8	K8	J4	J4	J4	J4
CE3_0_n	O	G7	G7	G7	G7	G6	G6	G6	G6	G7	G7	G7	G7
CE3_1_n	O	J9	J9	J9	J9	J9	J9	J9	J9	J5	J5	J5	J5
Vcc	M	C8	C8	C8	C8	C7	C7	C7	C7	H11	H11	H11	H11
		N8	N8	N8	N8	N7	N7	N7	N7	H1	H1	H1	H1
		D4	D4	D4	D4	D3	D3	D3	D3	D10	D10	D10	D10
		M12	M12	M12	M12	M11	M11	M11	M11	M2	M2	M2	M2
		G3	G3	G3	G3	G2	G2	G2	G2	C7	C7	C7	C7
		J13	J13	J13	J13	J12	J12	J12	J12	N5	N5	N5	N5
VccQ	M	C4	C4	C4	C4	C3	C3	C3	C3	D11	D11	D11	D11
		N12	N12	N12	N12	N11	N11	N11	N11	M1	M1	M1	M1
		D3	D3	D3	D3	D2	D2	D2	D2	C10	C10	C10	C10
		M13	M13	M13	M13	M12	M12	M12	M12	N2	N2	N2	N2
		E5	E5	E5	E5	E4	E4	E4	E4	E9	E9	E9	E9
		L11	L11	L11	L11	L10	L10	L10	L10	L3	L3	L3	L3
		F3	F3	F3	F3	F2	F2	F2	F2	C8	C8	C8	C8
		K13	K13	K13	K13	K12	K12	K12	K12	N4	N4	N4	N4
		K3	K3	K3	K3	K2	K2	K2	K2	C4	C4	C4	C4
		F13	F13	F13	F13	F12	F12	F12	F12	N8	N8	N8	N8
		L5	L5	L5	L5	L4	L4	L4	L4	E3	E3	E3	E3
		E11	E11	E11	E11	E10	E10	E10	E10	L9	L9	L9	L9
		M3	M3	M3	M3	M2	M2	M2	M2	C2	C2	C2	C2
		D13	D13	D13	D13	D12	D12	D12	D12	N10	N10	N10	N10
		N4	N4	N4	N4	N3	N3	N3	N3	D1	D1	D1	D1
		C12	C12	C12	C12	C11	C11	C11	C11	M11	M11	M11	M11
		N6	N6	N6	N6	N5	N5	N5	N5	F1	F1	F1	F1
		C10	C10	C10	C10	C9	C9	C9	C9	K11	K11	K11	K11

Signal Name	M/O/R	BGA-178 SDR x8	BGA-178 NV-DDR x8	BGA-178 NV-DDR2/3 x8	BGA-178 NV-LPDDR4 x8	BGA-154 SDR x8	BGA-154 NV-DDR x8	BGA-154 NV-DDR2/3 x8	BGA-154 NV-LPDDR4 x8	BGA-146 SDR x8	BGA-146 NV-DDR x8	BGA-146 NV-DDR2/3 x8	BGA-146 NV-LPDDR4 x8
Vss	M	C5	C5	C5	C5	C4	C4	C4	C4	E11	E11	E11	E11
		N11	N11	N11	N11	N10	N10	N10	N10	L1	L1	L1	L1
		C7	C7	C7	C7	C6	C6	C6	C6	G11	G11	G11	G11
		N9	N9	N9	N9	N8	N8	N8	N8	J1	J1	J1	J1
		E3	E3	E3	E3	E2	E2	E2	E2	C9	C9	C9	C9
		L13	L13	L13	L13	L12	L12	L12	L12	N3	N3	N3	N3
		F5	F5	F5	F5	F4	F4	F4	F4	E8	E8	E8	E8
		K11	K11	K11	K11	K10	K10	K10	K10	L4	L4	L4	L4
		J3	J3	J3	J3	J2	J2	J2	J2	C5	C5	C5	C5
		G13	G13	G13	G13	G12	G12	G12	G12	N7	N7	N7	N7
		K5	K5	K5	K5	K4	K4	K4	K4	E4	E4	E4	E4
		F11	F11	F11	F11	F10	F10	F10	F10	L8	L8	L8	L8
		L3	L3	L3	L3	L2	L2	L2	L2	C3	C3	C3	C3
		E13	E13	E13	E13	E12	E12	E12	E12	N9	N9	N9	N9
		N5	N5	N5	N5	N4	N4	N4	N4	E1	E1	E1	E1
		C11	C11	C11	C11	C10	C10	C10	C10	L11	L11	L11	L11
VREFQ_0	R	na	na	D8	D8	na	na	D7	D7	na	na	H10	H10
VREFQ_1	R	na	na	M8	M8	na	na	M7	M7	na	na	H2	H2
VDDi	O	na	na	na	na	na	na	na	na	na	na	na	na
Vpp	O	C6	C6	C6	C6	C5	C5	C5	C5	F11	F11	F11	F11
		D6	D6	D6	D6	D5	D5	D5	D5	F10	F10	F10	F10
		M10	M10	M10	M10	M9	M9	M9	M9	K2	K2	K2	K2
		N10	N10	N10	N10	N9	N9	N9	N9	K1	K1	K1	K1
CLE_0	M	J7	J7	J7	J7	J6	J6	J6	J6	G5	G5	G5	G5
CLE_1	O	G9	G9	G9	G9	G8	G8	G8	G8	J7	J7	J7	J7
ALE_0	M	K7	K7	K7	K7	K6	K6	K6	K6	G4	G4	G4	G4
ALE_1	O	F9	F9	F9	F9	F8	F8	F8	F8	J8	J8	J8	J8
WE_0_n	M	G6	na	G6	G6	G5	na	G5	G5	F7	na	F7	F7
WE_1_n	O	J10	na	J10	J10	J9	na	J9	J9	K5	na	K5	K5
CLK_0	M	na	G6	na	na	na	G5	na	na	na	F7	na	na
CLK_1	O	na	J10	na	na	na	J9	na	na	na	K5	na	na
WP_0_n	M	L7	L7	L7	L7	L6	L6	L6	L6	G3	G3	G3	G3
WP_1_n	O	E9	E9	E9	E9	E8	E8	E8	E8	J9	J9	J9	J9
IO0_0 / DQ0_0	M	L6	L6	L6	L6	L5	L5	L5	L5	F3	F3	F3	F3
IO1_0 / DQ1_0	M	K6	K6	K6	K6	K5	K5	K5	K5	F4	F4	F4	F4
IO2_0 / DQ2_0	M	L4	L4	L4	L4	L3	L3	L3	L3	D3	D3	D3	D3
IO3_0 / DQ3_0	M	K4	K4	K4	K4	K3	K3	K3	K3	D4	D4	D4	D4
IO4_0 / DQ4_0	M	F4	F4	F4	F4	F3	F3	F3	F3	D8	D8	D8	D8
IO5_0 / DQ5_0	M	E4	E4	E4	E4	E3	E3	E3	E3	D9	D9	D9	D9
IO6_0 / DQ6_0	M	F6	F6	F6	F6	F5	F5	F5	F5	F8	F8	F8	F8
IO7_0 / DQ7_0	M	E6	E6	E6	E6	E5	E5	E5	E5	F9	F9	F9	F9

Signal Name	M/O/R	BGA-178 SDR x8	BGA-178 NV-DDR x8	BGA-178 NV-DDR2/3 x8	BGA-178 NV-LPDDR4 x8	BGA-154 SDR x8	BGA-154 NV-DDR x8	BGA-154 NV-DDR2/3 x8	BGA-154 NV-LPDDR4 x8	BGA-146 SDR x8	BGA-146 NV-DDR x8	BGA-146 NV-DDR2/3 x8	BGA-146 NV-LPDDR4 x8
IO0_1 / DQ0_1	O	E10	E10	E10	E10	E9	E9	E9	E9	K9	K9	K9	K9
IO1_1 / DQ1_1	O	F10	F10	F10	F10	F9	F9	F9	F9	K8	K8	K8	K8
IO2_1 / DQ2_1	O	E12	E12	E12	E12	E11	E11	E11	E11	M9	M9	M9	M9
IO3_1 / DQ3_1	O	F12	F12	F12	F12	F11	F11	F11	F11	M8	M8	M8	M8
IO4_1 / DQ4_1	O	K12	K12	K12	K12	K11	K11	K11	K11	M4	M4	M4	M4
IO5_1 / DQ5_1	O	L12	L12	L12	L12	L11	L11	L11	L11	M3	M3	M3	M3
IO6_1 / DQ6_1	O	K10	K10	K10	K10	K9	K9	K9	K9	K4	K4	K4	K4
IO7_1 / DQ7_1	O	L10	L10	L10	L10	L9	L9	L9	L9	K3	K3	K3	K3
DQS_0_t	M	na	J4	J4	J4	na	J3	J3	J3	na	D5	D5	D5
DQS_1_t	O	na	G12	G12	G12	na	G11	G11	G11	na	M7	M7	M7
DQS_0_c	R	na	na	J5	J5	na	na	J4	J4	na	na	E5	E5
DQS_1_c	R	na	na	G11	G11	na	na	G10	G10	na	na	L7	L7
VSP0	O	M5	M5	M5	M5	M4	M4	M4	M4	E2	E2	E2	E2
VSP1	O	D11	D11	D11	D11	D10	D10	D10	D10	L10	L10	L10	L10
VSP2	O	M6	M6	M6	M6	M5	M5	M5	M5	F2	F2	F2	F2
VSP3	O	D10	D10	D10	D10	D9	D9	D9	D9	K10	K10	K10	K10
ENi	O	na	na	na	na	na	na	na	na	na	na	na	na
ENo	O	na	na	na	na	na	na	na	na	na	na	na	na
ZQ_0	O	na	na	D7	D7	na	na	D6	D6	na	na	G10	G10
ZQ_1	O	na	na	M9	M9	na	na	M8	M8	na	na	J2	J2
DBI_0	O	na	na	na	J6	na	na	na	J5	na	na	na	F5
DBI_1	O	na	na	na	G10	na	na	na	G9	na	na	na	K7

Table 2-6 Signal mappings: BGA-178, BGA-154 and BGA-146 packages

2.9. CE_n Signal Requirements

If one or more LUNs are active and the host sets CE_n to one, then those operations continue executing until completion at which point the NAND Target enters standby. After the CE_n signal is transitioned to one, the host may drive a different CE_n signal to zero and begin operations on another NAND Target. Note that if using a dual x8 package (e.g. BGA-100), then operations may execute in parallel on two different CE_n signals if they are connected to different 8-bit data buses.

When SR[6] for a particular LUN is cleared to zero and the CE_n signal for the corresponding NAND Target is pulled low, the host may only issue the Reset, Synchronous Reset, Reset LUN, Read Status, Read Status Enhanced, or Volume Select commands to that LUN.

2.9.1. Requirements for CLK (NV-DDR)

When using the NV-DDR data interface, the following requirements shall be met if the device does not support CLK being stopped during data input:

1. CLK shall only stop or start when CE_n is high.

When using the NV-DDR data interface, the following requirements shall be met if the device supports CLK being stopped during data input:

1. CLK shall only stop or start when either:
    a. CE_n is high, or
    b. CE_n is low and the bus state is data input

When using the NV-DDR data interface, the following requirements shall always be met:

1. CLK shall only change frequency when CE_n is high.
2. When CE_n is low, CLK shall maintain the same frequency.
3. CE_n shall only transition from one to zero when the CLK is stable and has a valid period based on the timing mode selected.
4. The interface shall be in an idle state (see section 4.3) when CE_n changes value. CE_n shall only transition when the following are true:
    a. ALE and CLE are both cleared to zero, and
    b. There is no data transfer on the DQ/DQS signals during the current clock period.

2.10. Absolute Maximum DC Ratings

Stresses greater than those listed in Table 2-7 may cause permanent damage to the device. This is a stress rating only. Operation beyond the recommended operating conditions specified in Table 2-8 and the DC and operating characteristics listed in Table 2-11 and Table 2-12 is not recommended. Except as defined in section 2.12, extended exposure beyond these conditions may affect device reliability.

Table 2-7 defines the voltage on any pin relative to Vss and/or VssQ for devices based on their Vcc and VccQ typical voltages.

Parameter	Symbol	Rating	Units
VPP Supply Voltage	V_{PP}	-0.6 to +16	V
Vcc = 3.3V and VccQ = 3.3V nominal			
Vcc Supply Voltage	V_{CC}	-0.6 to +4.6	V
Voltage Input	V_{IN}	-0.6 to +4.6	
VccQ Supply Voltage	V_{CCQ}	-0.6 to +4.6	
Vcc = 3.3V and VccQ = 1.8V nominal			
Vcc Supply Voltage	V_{CC}	-0.6 to +4.6	V
Voltage Input	V_{IN}	-0.2 to +2.4	
VccQ Supply Voltage	V_{CCQ}	-0.2 to +2.4	
Vcc = 3.3V and VccQ = 1.2V nominal			
Vcc Supply Voltage	V_{CC}	-0.6 to +4.6	V
Voltage Input	V_{IN}	-0.2 to +1.5	
VccQ Supply Voltage	V_{CCQ}	-0.2 to +1.5	
Vcc = 2.5V and VccQ = 1.8V nominal			
Vcc Supply Voltage	V_{CC}	-0.3 to +3.2	V
Voltage Input	V_{IN}	-0.2 to +2.4	
VccQ Supply Voltage	V_{CCQ}	-0.2 to +2.4	
Vcc = 2.5V and VccQ = 1.2V nominal			
Vcc Supply Voltage	V_{CC}	-0.3 to +3.2	V
Voltage Input	V_{IN}	-0.2 to +1.5	
VccQ Supply Voltage	V_{CCQ}	-0.2 to +1.5	
Vcc = 1.8V and VccQ = 1.8V nominal			
Vcc Supply Voltage	V_{CC}	-0.2 to +2.4	V
Voltage Input	V_{IN}	-0.2 to +2.4	
VccQ Supply Voltage	V_{CCQ}	-0.2 to +2.4	

Table 2-7 Absolute maximum DC ratings

2.11. Recommended DC Operating Conditions

3.3V or 1.8V VccQ operating conditions may be utilized for SDR or NV-DDR data interfaces. 1.8V VccQ operating conditions shall be used for the NV-DDR2 data interface. 1.2V VccQ operating conditions shall be used for the NV-DDR3 and NV-LPDDR4 data interface.

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage for 3.3V devices[4]	V_{CC}	2.7	3.3	3.6	V
Supply voltage for 2.5V devices[4]	V_{CC}	2.35	2.5	2.75	V
Supply voltage for 1.8V devices[4]	V_{CC}	1.7	1.8	1.95	V
Supply voltage for 3.3V I/O signaling[1,4]	V_{CCQ}	2.7	3.3	3.6	V
Supply voltage for 1.8V I/O signaling[2,4]	V_{CCQ}	1.7	1.8	1.95	V
Supply voltage for 1.2V I/O signaling[4]	V_{CCQ}	1.14	1.2	1.26	V
Ground voltage supply	V_{SS}	0	0	0	V
Ground voltage supply for I/O signaling	V_{SSQ}	0	0	0	V
External voltage supply[3]	V_{PP}	10.8	12.0	13.2	V

NOTE:
1. 3.3V VccQ is not supported for NV-DDR2.
2. 3.3V and 1.8V VccQ are not supported for NV-DDR3 or NV-LPDDR4.
3. The maximum external voltage supply current (I_{PP}) is 5 mA per LUN.
4. AC Noise on the supply voltages shall not exceed +/- 3%. 10 kHz to 800 MHz AC and DC noise together shall stay within the Min-Max range specified in this table.

Table 2-8 Recommended DC operating conditions

2.11.1. I/O Power (VccQ) and I/O Ground (VssQ)

VccQ and Vcc may be distinct and unique voltages. VccQ shall be less than or equal to Vcc, including during power-on ramp. The device shall support one of the following VccQ/Vcc combinations:

- Vcc = 3.3V, VccQ = 3.3V
- Vcc = 3.3V, VccQ = 1.8V
- Vcc = 3.3V, VccQ = 1.2V
- Vcc = 2.35-3.6V, VccQ = 1.8V
- Vcc = 2.35-3.6V, VccQ = 1.2V
- Vcc = 2.5V, VccQ = 1.8V
- Vcc = 2.5V, VccQ = 1.2V
- Vcc = 1.8V, VccQ = 1.8V

All parameters, timing modes, and other characteristics are relative to the supported voltage combination.

If a device has the same Vcc and VccQ voltage levels, then VccQ and VssQ are not required to be connected internal to the device. Specifically, the device may use Vcc and Vss exclusively as the I/O and core voltage supply.

2.12. AC Overshoot/Undershoot Requirements

The device may have AC overshoot or undershoot from VccQ and VssQ levels. Table 2-9 defines the maximum values that the AC overshoot or undershoot may attain. The SDR, NV-DDR and NV-DDR2 values apply for both 3.3V and 1.8V VccQ levels. The NV-DDR3 and NV-LPDDR4 values apply for only 1.2V VccQ levels.

The maximum overshoot area above VccQ and the maximum undershoot area below VssQ is symmetric and varies depending on timing mode; refer to Table 2-9. These values apply to the maximum data signaling frequency for a given timing mode. If the data signaling frequency for maximum overshoot or undershoot conditions is less than the selected timing mode, then the values for the applicable slower timing mode may be used.

NAND devices may have different maximum amplitude requirements for overshoot and undershoot than the controller. If the controller has more stringent requirements termination or other means of reducing overshoot or undershoot may be required to reduce beyond the NAND requirements.

Parameter	Maximum Overshoot above VccQ and Maximum Undershoot below VssQ		
	Area		Amplitude
	SDR		
All timing modes	3 V-ns		1V
	NV-DDR		
Timing Modes 0-2	3 V-ns		1V
Timing Mode 3	2.25 V-ns		
Timing Mode 4	1.8 V-ns		
Timing Mode 5	1.5 V-ns		
	NV-DDR2		
	I/O signals and RE_n	ALE, CLE, WE_n	All signals
Timing Mode 0-1	3 V-ns	3 V-ns	1V
Timing Mode 2	2.25 V-ns		
Timing Mode 3	1.8 V-ns		
Timing Mode 4	1.5 V-ns		
Timing Mode 5	1.1 V-ns		
Timing Mode 6	0.9 V-ns		
Timing Mode 7	0.75 V-ns		
Timing Mode 8	0.56 V-ns		
Timing Mode 9	0.45 V-ns		
Timing Mode 10	0.38 V-ns		
	NV-DDR3[1] / NV-LPDDR4[1]		
	I/O signals and RE_n	ALE, CLE, WE_n	All signals
Timing Mode 0-1	2.00 V-ns	3 V-ns	0.35 V
Timing Mode 2	1.20 V-ns		
Timing Mode 3	0.96 V-ns		
Timing Mode 4	0.80 V-ns		
Timing Mode 5	0.60 V-ns		
Timing Mode 6	0.48 V-ns		
Timing Mode 7	0.40 V-ns		
Timing Mode 8	0.30 V-ns		
Timing Mode 9	0.24 V-ns		
Timing Mode 10	0.20 V-ns		
Timing Mode 11	0.15 V-ns		
Timing Mode 12	0.13 V-ns		
Timing Mode 13	0.12 V-ns		
Timing Mode 14	0.11 V-ns		
Timing Mode 15	0.10 V-ns		
Timing Mode 16	0.09 V-ns		
Timing Mode 17	0.08 V-ns		
Timing Mode 18	0.073 V-ns		
Timing Mode 19	0.067 V-ns		
Timing Mode 20	0.057 V-ns		
Timing Mode 21	0.05 V-ns		
Timing Mode 22	0.044 V-ns		
NOTE 1: Intended for devices with no clamp protection and is guaranteed by design.			

Table 2-9 AC Overshoot/Undershoot Maximum Values

Figure 2-28 displays pictorially the parameters described in Table 2-9.

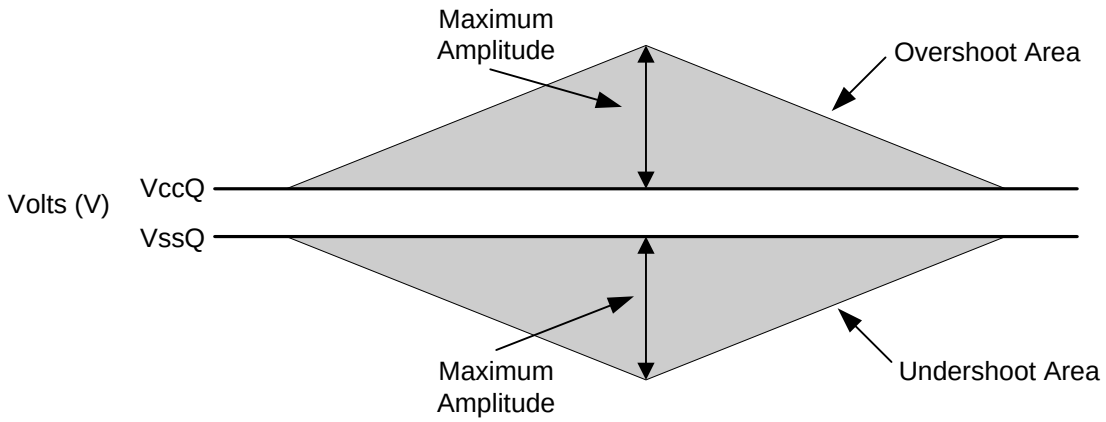


Figure 2-28 Overshoot/Undershoot Diagram

2.13. DC and Operating Characteristics

All operating current ratings in this section are specified per active logical unit (LUN). A LUN is active when there is a command outstanding to it. All other current ratings in this section are specified per LUN (regardless of whether it is active).

The test conditions and measurement methodology for the ICC values is defined in Appendix D.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Array read current	ICC1	Refer to Appendix D	-	-	100	mA
Array program current	ICC2		-	-	100	mA
Array erase current	ICC3		-	-	100	mA
I/O burst read current	ICC4R		-	-	50/100/135/180/250[5]	mA
	ICCQ4R[4]		-	-	50/100/135/180/250[5]	mA
I/O burst write current	ICC4W		-	-	50/100/135/180/250[5]	mA
	ICCQ4W		-	-	50/100/135/180/250[5]	mA
Bus idle current	ICC5		-	-	15	mA
Standby current	ISB	CE_n=VccQ-0.2V, WP_n=0V/VccQ	-	-	100	µA
Staggered power-up current	IST[1]	CE_n=VccQ-0.2V tRise = 1 ms cLine = 0.1 µF	-	-	10	mA
Vpp Idle current	IPPI[6]	-	-	-	10	uA
Vpp Active current	IPPA[6]	-	-	-	5	mA

NOTE:
1. Refer to Appendix C for an exception to the IST current requirement.
2. ICC1, ICC2, and ICC3 as listed in this table are active current values. For details on how to calculate the active current from the measured values, refer to Appendix D.
3. During cache operations, increased ICC current is allowed while data is being transferred on the bus and an array operation is ongoing. For a cached read this value is ICC1 + $ICC4_R$; for a cached write this value is ICC2(active) + $ICC4_W$.
4. For $ICCQ4_R$ the test conditions in Appendix D specify IOUT = 0 mA. When Iout is not equal to 0 mA, additional VccQ switching current will be drawn that is highly dependent on system configuration. IccQ due to loading without IOUT = 0 mA may be calculated for each output pin assuming 50% data switching as (IccQ = 0.5 * C_L * VccQ * frequency), where C_L is the capacitive load.
5. When the data frequency is above 2400 MT/s and below or equal to 3600MT/s, then the LUN may consume 250 mA. When the data frequency is above 800 MT/s and below or equal to 2400MT/s, then the LUN may consume 180 mA. When the data frequency is above 400MT/s and below or equal to 800 MT/s, then the LUN may consume 135 mA. When the data frequency is above 200 MT/s and below or equal to 400 MT/s, then the LUN may consume 100 mA. When the data frequency is below or equal to 200 MT/s, then the LUN may consume 50 mA.
6. IPP Idle current is IPP current measured when Vpp is supplied and Vpp is not enabled via Set Feature. IPP Active current is IPP current measured when Vpp is supplied and Vpp is enabled via Set Feature.

Table 2-10 DC and Operating Conditions for raw NAND, measured on Vcc or VccQ rail

The maximum input leakage current requirements (ILI) in Table 2-11, Table 2-12. Table 2-13, and Table 2-14 are tested across the entire allowed VccQ range, specified in Table 2-8. The maximum output leakage current requirements (ILO) in Table 2-11 are tested across the entire allowed VccQ range, specified in Table 7. Table 2-18 specifies output leakage current requirements (ILO) with VOUT for conditions of VccQ of 1.8V and 1.2V across the entire allowed VccQ range specified in Table 2-8 for 1.8V I/O signaling and 1.2V I/O signaling.

DC signal specifications apply to the following signals and only when using the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interfaces: CLK, DQ[7:0], DQS, ALE, CLE, and W/R_n. For all signals in SDR and all other signals in NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4, the AC signal specification shall be met. For signals where DC signal specifications apply, the transition times are measured between VIL (DC) and VIH (AC) for rising input signals and between VIH (DC) and VIL (AC) for falling input signals. The receiver will effectively switch as a result of the signal crossing the AC input level and remain in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.

The parameters in Table 2-11, Table 2-12, and Table 2-13 apply to power-on default values in the

device. If I/O drive strength settings or other device settings are changed, these values may be modified. The output characteristics for a device that supports driver strength settings (as indicated in the parameter page) are specified in the impedance tables (see section 4.11.3.3).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Standby current[3]	ISBQ	CE_n=VccQ-0.2V, WP_n=0V/VccQ	-	-	25	µA
Input leakage current	ILI	VIN=0V to VccQ	-	-	±10	µA
Output leakage current	ILO	VOUT=0V to VccQ	-	-	±10	µA
DC Input high voltage	VIH (DC)	-	VccQ * 0.7	-	VccQ + 0.3	V
AC Input high voltage	VIH (AC)	-	VccQ * 0.8	-	(Note 2)	V
DC Input low voltage	VIL (DC)	-	-0.3	-	VccQ * 0.3	V
AC Input low voltage	VIL (AC)	-	(Note 2)	-	VccQ * 0.2	V
Output high voltage[1]	VOH	IOH=-400 µA	VccQ * 0.67	-	-	V
Output low voltage[1]	VOL	IOL=2.1 mA		-	0.4	V
Output low current (R/B_n)	IOL(R/B_n)	VOL=0.4 V	8	10	-	mA

NOTE:
1. VOH and VOL defined in this table shall only apply to SDR only devices that do not support driver strength settings. If driver strength settings are supported, then section 4.11.3.3 shall be used to derive the output driver impedance values.
2. Refer to section 2.12 for AC Overshoot and Undershoot requirements.
3. During ISBQ testing, DQS, RE_n, and DQ[7:0] are floating.

Table 2-11 DC and Operating Conditions for VccQ of 3.3V, measured on VccQ rail

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Standby current [3]	ISBQ	CE_n=VccQ-0.2V, WP_n=0V/VccQ	-	-	75	µA
Input leakage current	ILI	VIN=0V to VccQ	-	-	±10	µA
DC Input high voltage	VIH (DC)	-	VccQ * 0.7	-	VccQ+0.3	V
AC Input high voltage	VIH (AC)	-	VccQ * 0.8	-	(Note 2)	V
DC Input low voltage	VIL (DC)	-	-0.3	-	VccQ * 0.3	V
AC Input low voltage	VIL (AC)	-	(Note 2)	-	VccQ * 0.2	V
Output high voltage[1]	VOH	IOH=-100 µA	VccQ – 0.1	-	-	V
Output low voltage[1]	VOL	IOL=100 µA	-	-	0.1	V
Output low current (R/B_n)	IOL(R/B_n)	VOL=0.2 V	3	4	-	mA

NOTE:
1. VOH and VOL defined in this table shall only apply to SDR only devices that do not support driver strength settings. If driver strength settings are supported then section 4.11.3.3 shall be used to derive the output driver impedance values.
2. Refer to section 2.12 for AC Overshoot and Undershoot requirements.
3. During ISBQ testing, DQS, W/R_n, and DQ[7:0] are floating.

Table 2-12 DC and Operating Conditions for VccQ of 1.8V (NV-DDR), measured on VccQ rail

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Standby current[3]	ISBQ	CE_n=VccQ-0.2V, WP_n=0V/VccQ	-	-	75	µA
Input leakage current	ILI	VIN=0V to VccQ	-	-	±10	µA
VREFQ leakage current	IVREFQ	VREFQ=VccQ/2 (All other pins not under test = 0V)	-	-	±5	µA
DC Input high voltage	VIH.SSTL[4] (DC)	-	VREFQ + 125	-	VccQ + 300	mV
AC Input high voltage	VIH.SSTL[4] (AC)	-	VREFQ + 250	-	(Note 1)	mV
DC Input low voltage	VIL.SSTL[4] (DC)	-	-300	-	VREFQ - 125	mV
AC Input low voltage	VIL.SSTL[4] (AC)	-	(Note 1)	-	VREFQ - 250	mV
DC Input high voltage (CE_n, WP_n)	VIH.CMOS[5] (DC)	-	VccQ * 0.7	-	VccQ + 300	mV
AC Input high voltage (CE_n, WP_n)	VIH.CMOS[5] (AC)	-	VccQ *0.8	-	(Note 1)	mV
DC Input low voltage (CE_n, WP_n)	VIL.CMOS[5] (DC)	-	-300	-	VccQ * 0.3	mV
AC Input low voltage (CE_n, WP_n)	VIL.CMOS[5] (AC)	-	(Note 1)	-	VccQ * 0.2	mV
Output low current (R/B_n)	IOL(R/B_n)	VOL=0.2 V	3	4	-	mA

NOTE:
1. Refer to section 2.12 for AC Overshoot and Undershoot requirements.
2. CE_n and WP_n are CMOS signals and do not use SSTL levels.
3. During ISBQ testing, DQS_t/DQS_c, RE_t/RE_c, and DQ[7:0] are floating.
4. SSTL signals are RE_t/RE_c, DQS_t/DQS_c, DQ[7:0]
5. CLE, ALE and WE_n signals may support only one of either SSTL or CMOS Vih/Vil levels, or both SSTL and CMOS levels. See vendor data sheet to see which levels are supported by the CLE, ALE and WE_n pins of a device.

Table 2-13 DC and Operating Conditions for VccQ of 1.8V (NV-DDR2), measured on VccQ rail

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Standby current[3]	ISBQ	CE_n=VccQ-0.2V, WP_n=0V/VccQ	-	-	125	µA
Input leakage current	ILI	VIN=0V to VccQ	-	-	±10	µA
VREFQ leakage current	IVREFQ	VREFQ=VccQ/2 (All other pins not under test = 0V)	-	-	±5	µA
DC Input high voltage w/o V_{REFQ}	VIH.SSTL[4,5] (DC)		VccQ * 0.7	-	VccQ	mV
AC Input high voltage w/o V_{REFQ}	VIH.SSTL[4,5] (AC)		VccQ *0.8	-	(Note 1)	mV
DC Input low voltage w/o V_{REFQ}	VIL.SSTL[4,5] (DC)		VssQ	-	VccQ * 0.2	mV
AC Input low voltage w/o V_{REFQ}	VIL.SSTL[4,5] (AC)		(Note 1)	-	VccQ * 0.1	mV
DC Input high voltage w/ V_{REFQ}[9]	VIH.SSTL[4,7] (DC)	Timing mode 0 – 15	VREFQ + 100	-	VccQ	mV
		Timing mode 16 - 21	VREFQ + 80			
		Timing mode 22	VREFQ + 70			
AC Input high voltage w/ V_{REFQ}[9]	VIH.SSTL[4,7] (AC)	Timing mode 0 – 15	VREFQ + 150	-	(Note 1)	mV
		Timing mode 16 – 21	VREFQ + 100			
		Timing mode 22	VREFQ + 95			
DC Input low voltage w/ V_{REFQ}[9]	VIL.SSTL[4,7] (DC)	Timing mode 0 – 15	VssQ	-	VREFQ - 100	mV
		Timing mode 16 - 21			VREFQ - 80	
		Timing mode 22			VREFQ - 70	
AC Input low voltage w/ V_{REFQ}[9]	VIL.SSTL[4,7] (AC)	Timing mode 0 – 15	(Note 1)	-	VREFQ - 150	mV
		Timing mode 16 – 21			VREFQ - 100	
		Timing mode 22			VREFQ - 95	
DQ RX Mask Voltage total[7]	VDIVW.SSTL[8]	Timing mode 0 – 14	-	-	-	mV
		Timing mode 15	200			
		Timing mode 16 - 21	180			
		Timing mode 22	140			
DQ AC Input pulse amplitude pk-pk	VIHL.SSTL[8,10,11,12] (AC)	Timing Mode 16 - 21	220	-	-	mV
		Timing mode 22	190			
DC Input high voltage (CE_n, WP_n)	VIH.CMOS[6] (DC)	-	VccQ * 0.7	-	VccQ	mV
AC Input high voltage (CE_n, WP_n)	VIH.CMOS[6] (AC)	-	VccQ *0.8	-	(Note 1)	mV
DC Input low voltage (CE_n, WP_n)	VIL.CMOS[6] (DC)	-	VssQ	-	VccQ * 0.3	mV
AC Input low voltage (CE_n, WP_n)	VIL.CMOS[6] (AC)	-	(Note 1)	-	VccQ * 0.2	mV
Output low current (R/B_n)	IOL(R/B_n)	VOL=0.2 V	3	4	-	mA

NOTE:
1. Refer to section 2.12 for AC Overshoot and Undershoot requirements.
2. CE_n and WP_n are CMOS signals and do not use SSTL levels.
3. During ISBQ testing, DQS_t/DQS_c, RE_t/RE_c, DQ[7:0] and DBI are floating.
4. SSTL signals are RE_t/RE_c, DQS_t/DQS_c, DQ[7:0] and DBI. For RE_t, RE_n, DQS_t and DQS_c these are single-ended signal requirements.
5. Specifications apply to command, address bus cycles and unterminated data input cycles
6. CLE, ALE and WE_n signals may support only one of either SSTL or CMOS Vih/Vil levels, or both SSTL and CMOS levels. See vendor data sheet to see which levels are supported by the CLE, ALE and WE_n pins of a device.
7. For DQ signals, above 1600MT/s (Timing Mode > 15) these specifications are replaced by the DQ Rx Mask and VIHL.SSTL (AC) specifications shall be used
8. Only applies when RX mask is used. See section 4.18.6 for RX mask definition
9. V_{REFQ} may be External V_{REFQ} or Internal V_{REFQ} (see vendor datasheet for Internal V_{REFQ} support). If internal VrefQ Is used, then Vcent_DQ is the reference for SSTL signals.
10. The DQ only input pulse amplitude must meet or exceed VIHL_AC at any point over the total UI, except when no transitions are occurring for that UI.
11. VIHL_AC is centered around Vcent_DQ (pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ (pin_mid). For CTT interface, Vcent_DQ (pin_mid) is replaced by VrefQ as the center reference level in the case where External VrefQ is used or Internal VrefQ without Vref training is used.
12. There are no timing requirements above or below VIHL_AC levels.

Table 2-14 DC and Operating Conditions for VccQ of 1.2V (NV-DDR3), measured on VccQ rail

The Controller DQ RX Mask specifications in the Table 2-15 below are applicable to controllers that support the data rates listed in the tables below. These specifications do not apply to NAND component

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DQ RX Mask Voltage total	VDIVW.SSTL	Timing mode 0 – 14	-	-	-	mV
		Timing mode 15	200			
		Timing mode 16 - 21	180			
		Timing mode 22	140			

NOTES:
1. Vcent_DQ (pin_mid) shall be replaced by VrefQ in the case where External VrefQ is used or Internal VrefQ without Vref training is used.
2. At 1600Mbps, use of Rx mask specifications is optional, see vendor datasheet whether Rx mask specifications are supported by the device at that data rate.
3. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment.

Table 2-15 Controller DC RX Mask Conditions for VccQ of 1.2V (NV-DDR3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Standby current[3]	ISBQ	CE_n=VccQ-0.2V, WP_n=0V/VccQ	-	-	125	µA
Input leakage current	ILI	VIN=0V to VccQ	-	-	±10	µA
DC Input high voltage unterminated	VIH.UNTERM[4,5,10] (DC)	-	VccQ * 0.5	-	VccQ	mV
AC Input high voltage unterminated	VIH.UNTERM[4,5,10] (AC)	-	VccQ *0.5	-	(Note 1)	mV
DC Input low voltage unterminated	VIL.UNTERM[4,5,10] (DC)	-	VssQ	-	80	mV
DC Input low voltage unterminated	VIL.UNTERM[4,5,10] (AC)	-	(Note 1)	-	60	mV
DC Input high voltage	VIH.LTT[4] (DC)	Timing mode 16 - 21	Vcent_DQ + 80	-	VccQ	mV
		Timing mode 22	Vcent_DQ + 60			
AC Input high voltage	VIH.LTT[4] (AC)	Timing mode 16 - 21	Vcent_DQ + 100	-	(Note 1)	mV
		Timing mode 22	Vcent_DQ + 85			
DC Input low voltage	VIL.LTT[4] (DC)	Timing mode 16 - 21	VssQ	-	Vcent_DQ - 80	mV
		Timing mode 22			Vcent_DQ - 60	
AC Input low voltage	VIL.LTT[4] (AC)	Timing mode 16 - 21	(Note 1)	-	Vcent_DQ - 100	mV
		Timing mode 22			Vcent_DQ - 85	
DQ RX Mask Voltage total	VDIVW.LTT[6]	Timing mode 16 - 21	160	-	-	mV
		Timing mode 22	120			
DQ AC Input pulse amplitude pk-pk	VIHL.LTT[6,11,12,13] (AC)	Timing mode 16 - 21	200	-	-	mV
		Timing mode 22	170			
DC Input high voltage (CE_n, WP_n, CLE, ALE, WE_n)	VIH.CMOS (DC)	-	VccQ * 0.7	-	VccQ	mV
AC Input high voltage (CE_n, WP_n, CLE, ALE, WE_n)	VIH.CMOS (AC)	-	VccQ *0.8	-	(Note 1)	mV
DC Input low voltage (CE_n, WP_n, CLE, ALE, WE_n)	VIL.CMOS (DC)	-	VssQ	-	VccQ * 0.3	mV
AC Input low voltage (CE_n, WP_n, CLE, ALE, WE_n)	VIL.CMOS (AC)	-	(Note 1)	-	VccQ * 0.2	mV
Output low current (R/B_n)	IOL(R/B_n)	VOL=0.2 V	3	4	-	mA

NOTE:
1. Refer to section 2.12 for AC Overshoot and Undershoot requirements.
2. CE_n, WE_n, ALE, CLE and WP_n are CMOS signals and do not use SSTL levels.
3. During ISBQ testing, DQS_t/DQS_c, RE_t/RE_c, DQ[7:0] and DBI are floating.
4. LTT signals are RE_t/RE_c, DQS_t/DQS_c, DQ[7:0] and DBI. For RE_t, RE_n, DQS_t and DQS_c these are single-ended signal requirements.
5. Termination is disabled during command cycles, address cycles and during data input/output cycles when ODT from the NAND (target and non-target) and the controller are disabled.
6. Only applies when RX mask is used. See section 4.18.6 for RX mask definition
7. Vcent_DQ shall be regarded as Vcent_RE, Vcent_DQS and Vcent_DQ for RE_t/RE_c, DQS_t/DQS_c, DBI and DQ[7:0] signals respectively.
8. For DQ signals, DC signal requirements are replaced with the Rx Mask
9. For DQ signals, AC signal requirements are replaced with the VIHL_AC specification.
10. NAND vendors may support a higher VIL.UNTERM or lower VIH.UNTERM specification. See vendor datasheet.
11. The DQ only input pulse amplitude must meet or exceed VIHL_AC at any point over the total UI, except when no transitions are occurring for that UI.

12. VIHL_AC is centered around Vcent_DQ (pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ (pin_mid). For CTT interface, Vcent_DQ (pin_mid) is replaced by VrefQ as the center reference level in the case where External VrefQ is used or Internal VrefQ without Vref training is used.
13. There are no timing requirements above or below VIHL_AC levels.

Table 2-16 DC and Operating Conditions for VccQ of 1.2V (NV-LPDDR4), measured on VccQ rail

The Controller DQ RX Mask specifications in the Table 2-15 below are applicable to controllers that support the data rates listed in the tables below. These specifications do not apply to NAND component

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DQ RX Mask Voltage total	VDIVW.SSTL	Timing mode 0 – 14	-	-	-	mV
		Timing mode 15	200			
		Timing mode 16 - 21	180			
		Timing mode 22	140			

NOTES:
1. Vcent_DQ (pin_mid) shall be replaced by VrefQ in the case where External VrefQ is used or Internal VrefQ without Vref training is used.
2. At 1600Mbps, use of Rx mask specifications is optional, see vendor datasheet whether Rx mask specifications are supported by the device at that data rate.
3. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment.

Table 2-17 Controller DC RX Mask Conditions for VccQ of 1.2V (NV-LPDDR4)

Symbol	Parameter	Max
ILO_{pd}	Output leakage current: DQ are disabled: VOUT=VCCQ;	20uA[1]
ILO_{pu}	Output leakage current: DQ are disabled: VOUT=0V; ODT disabled	20uA[1]

NOTE:
1. Absolute leakage value per DQ pin per NAND die. The following signals are required to meet output leakage (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c)

Table 2-18 Output Leakage

The differential AC and DC input levels are defined in Table 2-19. These levels are used to calculate differential signal slew rate, refer to section 4.14.

Parameter	Symbol	Min	Max	Units
Differential input high	VIHdiff (DC)	2 x [VIH.SSTL (DC) – VREFQ]	Refer to Note 1.	V
Differential input low	VILdiff (DC)	Refer to Note 1.	2 x [VIL.SSTL (DC) – VREFQ]	V
Differential input high AC	VIHdiff (AC)	2 x [VIH.SSTL (AC) – VREFQ]	Refer to Note 1.	V
Differential input low AC	VILdiff (AC)	Refer to Note 1.	2 x [VIL.SSTL (AC) – VREFQ]	V

NOTE:
1. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [VIH(DC) max, VIL (DC) min] for single-ended signals as well as the limitations for overshoot and undershoot in Table 2-13.

Table 2-19 NV-DDR3 Differential AC and DC Input Levels

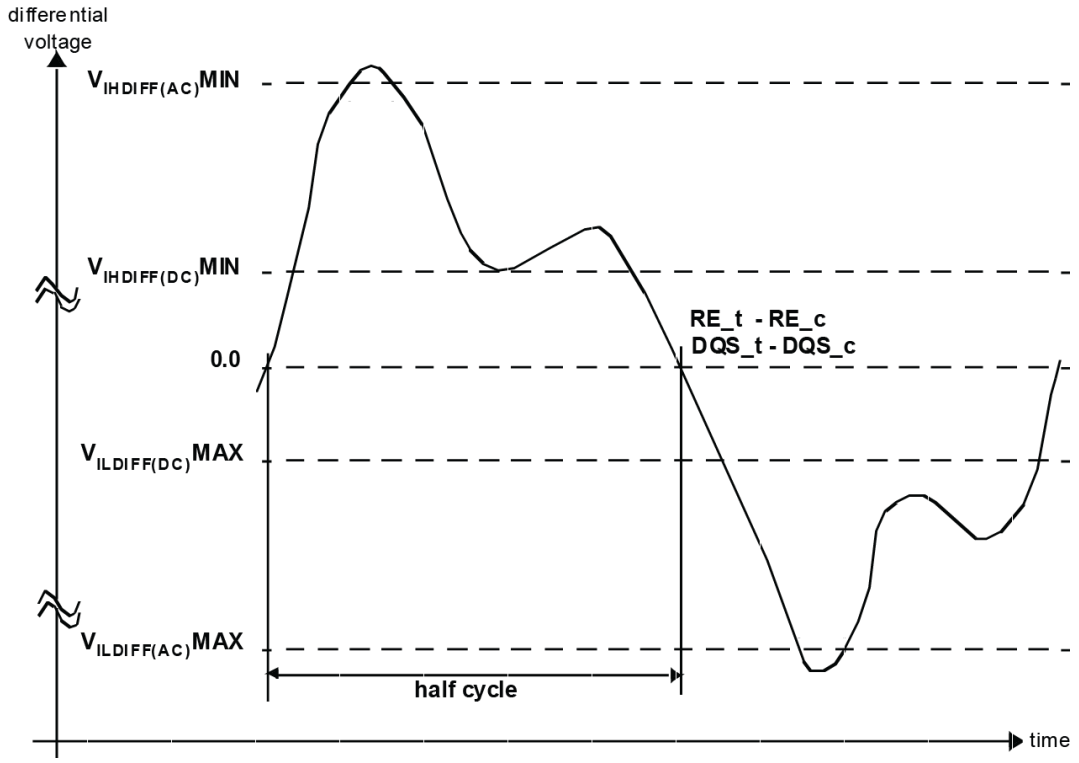


Figure 2-29 Definition of Differential AC Swing

2.13.1. Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (RE_t, DQS_t, RE_c, or DQS_c) shall comply with requirements for single-ended signals. RE_t and RE_c shall meet VSEH(AC)min / VSEL(AC)max in every half-cycle. DQS_t and DQS_c shall meet VSEH(AC)min / VSEL(AC)max in every half-cycle preceding and following a valid transition.

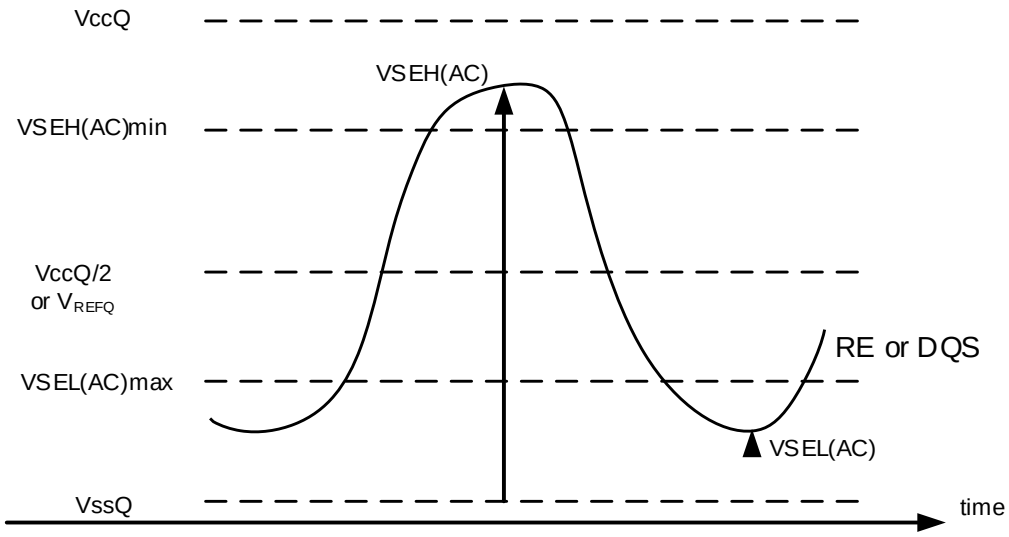


Figure 2-30 Single-Ended Requirements for Differential Signals

While control (e.g., ALE, CLE) and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VccQ/2; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL(AC)max, VSEH(AC)min has no bearing on timing but adds a restriction on the common mode characteristics of these signals.

Symbol	Parameter	Minimum	Maximum	Unit
$V_{SEH(AC)}$	NV-DDR2 Single-Ended high-level	VccQ/2 + 0.250	Note 1	V
$V_{SEL(AC)}$	NV-DDR2 Single-Ended low-level	Note 1	VccQ/2 – 0.250	V
$V_{SEH(AC)}$	NV-DDR3 Single-Ended high-level	VIH.SSTL(AC) w/ VREF	Note 1	V
$V_{SEL(AC)}$	NV-DDR3 Single-Ended low-level	Note 1	VIL.SSTL(AC) w/ VREF	V
$V_{SEH(AC)}$	NV-LPDDR4 Single-Ended high-level	V_{REFQ} + 0.100	Note 1	V
$V_{SEL(AC)}$	NV-LPDDR4 Single-Ended low-level	Note 1	V_{REFQ} – 0.100	V

NOTE:
1. These values are not defined. However, the single-ended signals RE_t, RE_c, DQS_t, DQS_c, shall be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Table 2-20 Single-Ended Levels for RE_t, DQS_t, RE_c, and DQS_c

2.13.2. External VREFQ Tolerance

The DC-tolerance limits and AC-noise limits for the reference voltage VREFQ are illustrated in Figure 2-31. It shows a valid reference voltage VREFQ(t) as a function of time. VREFQ(DC) is the linear average of VREFQ(t) over a long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of VccQ, also measured over a long period of time (e.g. 1 sec). This average shall meet the minimum/maximum requirements defined in Table 2-21. VREFQ(t) may temporarily deviate from VREFQ(DC) by no more than +/- 1% VccQ. VREFQ(t) shall not track noise on VccQ if this would result in VREFQ deviating outside of these specifications.

The location of the VREFQ tolerance measurement is across the pins of the VREFQ de-cap that is closest to the NAND package VREFQ pin.

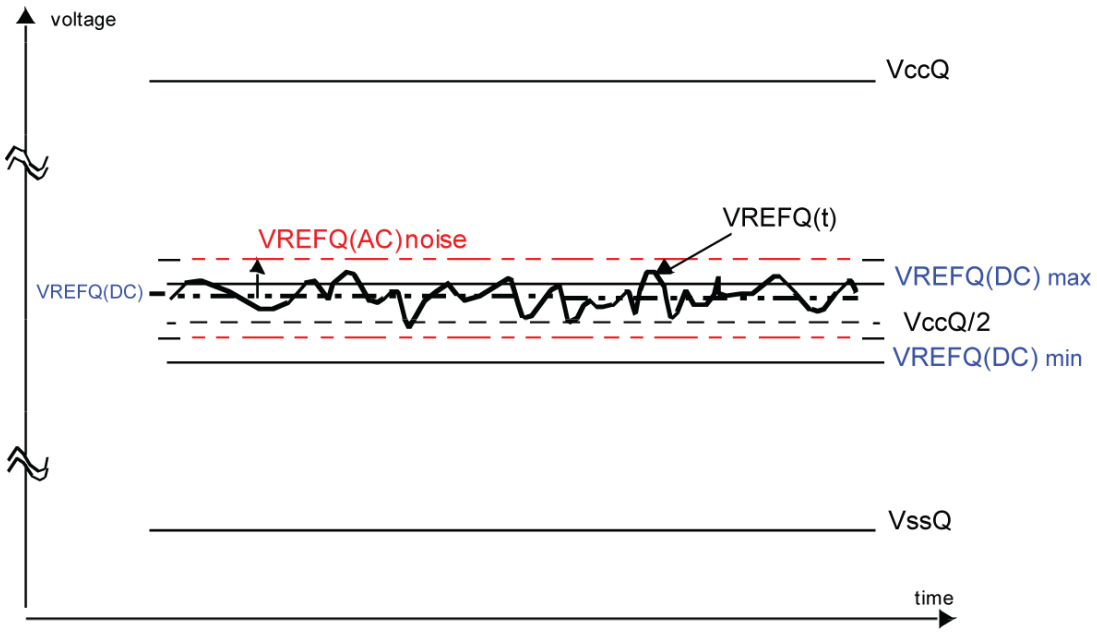


Figure 2-31 Illustration of VREFQ tolerance and VREF AC-noise limits

Parameter	Symbol	Minimum	Maximum	Unit
Reference Voltage	VREFQ(DC)	0.49 x VccQ	0.51 x VccQ	V

Table 2-21 External VREFQ specification

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREFQ.

This clarifies that the setup/hold specification and derating values need to include time and voltage associated with VREFQ AC-noise. Timing and voltage effects due to AC-noise on VREFQ up to the specified limit (+/-1% of VccQ) are included in timings and their associated deratings. During any transaction, if the device induces VREFQ noise that is greater than 20 MHz and causes a VREFQ violation, the device shall still meet specifications.

External VREFQ may be turned off when all CE_n (NAND Targets) that use the external VREFQ are high. Before CE_n is pulled low to enable operation, external VREFQ shall be stable and within the VREFQ tolerance.

2.13.3. Internal VREFQ Specification

The Table 2-22 shows the minimum required range of internal VREFQ. NAND devices may offer a wider allowable range (see vendor datasheet). A host shall not set the NAND internal VREFQ to a setting beyond the allowable range even during Write Training Internal VREFQ training. These specs define the allowable range for NAND internal VrefQ settings but does not represent the needed settings for high-speed operations. The needed settings for high-speed operations is obtained from either NAND vendor recommendation or through Internal VrefQ Training. NAND Devices could support either Value1 or Value3 settings (see vendor datasheet)

Parameter	Symbol	Minimum	Maximum	Unit
NV-DDR3 minimum allowable range upper limit	VREFQHI.SSTL	-	0.55 x VccQ	V
NV-DDR3 minimum allowable range lower limit	VREFQLO.SSTL	0.45 x VccQ	-	V
NV-LPDDR4 minimum allowable range upper limit	VREFQHI.LTT	-	0.40 x VccQ	V
NV-LPDDR4 minimum allowable range lower limit	VREFQLO.LTT	160	-	mV
Internal VREFQ Tolerance	VREFQ.TOL	-1.75%	+1.75%	VccQ

Table 2-22 Internal VREFQ specification for Value1

Parameter	Symbol	Minimum	Maximum	Unit
NV-DDR3 minimum allowable range upper limit	VREFQHI.SSTL	-	0.55 x VccQ	V
NV-DDR3 minimum allowable range lower limit	VREFQLO.SSTL	0.45 x VccQ	-	V
NV-LPDDR4 minimum allowable range upper limit	VREFQHI.LTT	-	0.3175 x VccQ	V
NV-LPDDR4 minimum allowable range lower limit	VREFQLO.LTT	160	-	mV
Internal VREFQ Tolerance	VREFQ.TOL	-1.75%	+1.75%	VccQ

Table 2-23 Internal VREFQ specification for Value3

2.14. Staggered Power-up

Subsystems that support multiple Flash devices may experience power system design issues related to the current load presented during the power-on condition. To limit the current load presented to the host at power-on, all devices shall support power-up in a low-power condition.

Until a Reset (FFh) command is received by the NAND Target after power-on, the NAND Target shall not draw more than IST of current per LUN. For example, a NAND Target that contains 4 LUNs may draw up to 40 mA of current until a Reset (FFh) command is received after power-on.

This value is measured with a nominal rise time (tRise) of 1 millisecond and a line capacitance (cLine) of 0.1 µF. The measurement shall be taken with 1 millisecond averaging intervals and shall begin after Vcc reaches Vcc_min and VccQ reaches VccQ_min.

2.15. Power Cycle Requirements

As part of a power cycle, the host shall hold both the Vcc and VccQ voltage levels below 100 mV for a minimum time of 100 ns. If these requirements are not met as part of a power cycle operation, the device may enter an indeterminate state.

2.16. Independent Data Buses

There may be two independent 8-bit data buses in some ONFI packages (i.e. the LGA and the 100-ball BGA package). There may be four independent 8-bit data buses in some ONFI packages (i.e. the BGA-316 and BGA-272 packages). For packages that support either two independent data buses or a single data bus (e.g. LGA-52) then CE0_n and CE2_n shall use the same pins as the first data bus CE_n pins (marked as CE0_0_n and CE1_0_n) and CE1_n and CE3_n shall use the same pins as the second data bus CE_n pins (marked as CE0_1_n and CE1_1_n). Note that CE0_n, CE1_n, CE2_n, and CE3_n may all use the first data bus and the first set of control signals (RE0_n, CLE0_n, ALE0_n, WE0_n, and WP0_n) if the device does not support independent data buses.

Any signal with a channel (i.e. 8-bit data bus) designator (for example, “x” for CE0_x_n) could not be used by another channel. For example, CE0_0 cannot be used on any channel other than channel 0 or R/B0_1 cannot be used for any channel other than channel 1.

In some package configurations, there are multiple CE_n signals per R/B_n signal. Table 2-24 describes the R/B_n signal that each CE_n uses in the case when there are two R/B_n signals and more than one CE_n per 8-bit data bus. Table 2-25 describes the R/B_n signal that each CE_n uses in the case when there is a single R/B_n signal per 8-bit data bus. Table 2-26 provides the case when there is a single CE_n and two R/B_n signals per 8-bit data bus. For packages that only support two 8-bit data buses, R/B0_2_n, R/B1_2_n, R/B0_3_n and R/B1_3_n shall be ignored.

Signal Name	CE_n
R/B0_0_n	CE0_0_n, CE2_0_n, CE4_0_n, CE6_0_n
R/B0_1_n	CE0_1_n, CE2_1_n, CE4_1_n, CE6_1_n
R/B0_2_n	CE0_2_n, CE2_2_n, CE4_2_n, CE6_2_n
R/B0_3_n	CE0_3_n, CE2_3_n, CE4_3_n, CE6_3_n
R/B1_0_n	CE1_0_n, CE3_0_n, CE5_0_n, CE7_0_n
R/B1_1_n	CE1_1_n, CE3_1_n, CE5_1_n, CE7_1_n
R/B1_2_n	CE1_2_n, CE3_2_n, CE5_2_n, CE7_2_n
R/B1_3_n	CE1_3_n, CE3_3_n, CE5_3_n, CE7_3_n

Table 2-24 R/B_n Signal Use per CE_n with two R/B_n signals per channel

Signal Name	CE_n
R/B0_0_n	CE0_0_n, CE1_0_n, CE2_0_n, CE3_0_n, CE4_0_n, CE5_0_n, CE6_0_n, CE7_0_n
R/B0_1_n	CE0_1_n, CE1_1_n, CE2_1_n, CE3_1_n, CE4_1_n, CE5_1_n, CE6_1_n, CE7_1_n
R/B0_2_n	CE0_2_n, CE1_2_n, CE2_2_n, CE3_2_n, CE4_2_n, CE5_2_n, CE6_2_n, CE7_2_n
R/B0_3_n	CE0_3_n, CE1_3_n, CE2_3_n, CE3_3_n, CE4_3_n, CE5_3_n, CE6_3_n, CE7_3_n

Table 2-25 R/B_n Signal Use per CE_n with a single R/B_n signal per channel

Signal Name	CE_n
R/B0_0_n	CE0_0_n
R/B0_1_n	CE0_1_n
R/B0_2_n	CE0_2_n
R/B0_3_n	CE0_3_n
R/B1_0_n	CE1_0_n
R/B1_1_n	CE1_1_n
R/B1_2_n	CE1_2_n
R/B1_3_n	CE1_3_n

Table 2-26 R/B_n Signal Use per CE_n with a two R/B_n signals per channel and one CE_n per channel

Implementations may tie the data lines and control signals (RE_n, CLE, ALE, WE_n, WP_n, and DQS) together for the two independent 8-bit data buses externally to the device.

2.17. Bus Width Requirements

All NAND Targets per device shall use the same data bus width. All targets shall either have an 8-bit bus width or a 16-bit bus width. Note that devices that support the NV-DDR, NV-DDR2 NV-DDR3 or NV-LPDDR4 data interface shall have an 8-bit bus width.

When the host supports a 16-bit bus width, only data is transferred at the 16-bit width. All address and command line transfers shall use only the lower 8-bits of the data bus. During command transfers, the host may place any value on the upper 8-bits of the data bus. During address transfers, the host shall set the upper 8-bits of the data bus to 00h.

2.18. Ready/Busy (R/B_n) Requirements

2.18.1. Power-On Requirements

Once V_{CC} and VccQ reach the V_{CC} minimum and VccQ minimum values, respectively, listed in Table 2-8 and power is stable, the R/B_n signal shall be valid after RB_valid_Vcc and shall be set to one (Ready) within RB_device_ready, as listed in Table 2-27. R/B_n is undefined until 50 µs has elapsed after V_{CC} has started to ramp. The R/B_n signal is not valid until both of these conditions are met.

Parameter	NAND
RB_valid_Vcc	10 µs
RB_device_ready	1 ms

Table 2-27 R/B_n Power-on Requirements

During power-on, VccQ shall be less than or equal to Vcc at all times. Figure 2-32 shows VccQ ramping after Vcc, however, they may ramp at the same time.

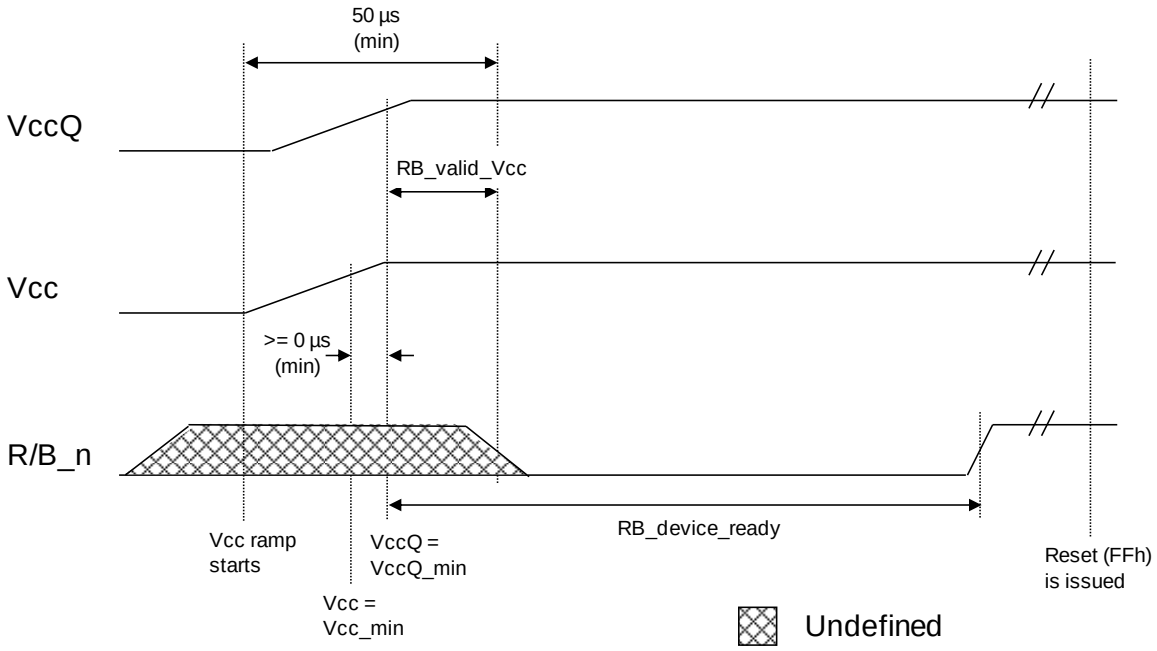


Figure 2-32 R/B_n Power-On Behavior

Ready/Busy is implemented as an open drain circuit, thus a pull-up resistor shall be used for termination. The combination of the pull-up resistor and the capacitive loading of the R/B_n circuit determines the rise time of R/B_n.

2.18.2. R/B_n and SR[6] Relationship

R/B_n shall reflect the logical AND of the SR[6] (Status Register bit 6) values for all LUNs on the corresponding NAND Target or Volume. In the case that more than one NAND target or Volume share an R/B_n signal, R/B_n shall reflect the logical AND of the SR[6] (Status Register bit 6) values for all LUNs connected to the shared R/B_n signal. For example, R/B0_0 is logical AND of the SR[6] values for all LUNs that share R/B0_0. Thus, R/B_n reflects whether any LUN is busy on a particular NAND Target or if there are multiple NAND Targets that share R/B_n, R/B_n reflects whether any LUN is busy on any of the shared NAND Targets.

2.19. Write Protect

When cleared to zero, the WP_n signal disables Flash array program and erase operations. This signal shall only be transitioned while there are no commands executing on the device. After modifying the value of WP_n, the host shall not issue a new command to the device for at least tWW delay time.

Figure 2-33 describes the tWW timing requirement, shown with the start of a Program command. The transition of the WP_n signal is asynchronous and unrelated to any CLK transition in the NV-DDR data interface. The bus shall be idle for tWW time after WP_n transitions from zero to one before a new command is issued by the host, including Program. The bus shall be idle for tWW time after WP_n transitions from one to zero before a new command is issued by the host.

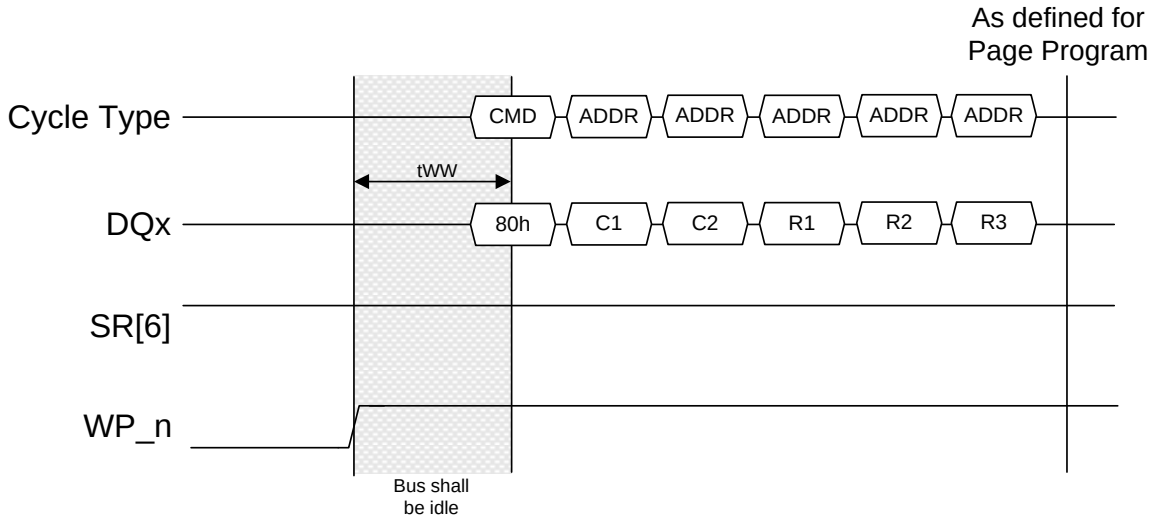


Figure 2-33 Write Protect timing requirements, example

2.20. CE_n Pin Reduction Mechanism

There may be a significant number of CE_n pins in high capacity implementations where there are many NAND packages with two to eight CE_n pins per package. The CE_n pin reduction mechanism enables a single CE_n pin from the host to be shared by multiple NAND Targets, thus enabling a significant reduction in CE_n pins required by the host. The CE_n pin reduction mechanism may be utilized with any data interface (SDR, NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4).

In the CE_n reduction mechanism, a NAND Target is appointed a Volume address during the initialization sequence, refer to section 3.2. After initialization is complete, the host may address a particular Volume (i.e. NAND Target) by using the Volume Select command.

Figure 2-34 shows an example topology using the CE_n pin reduction mechanism. ENi and ENo pins are added to each NAND package and a daisy chain is created between NAND packages. The first NAND package in the chain has ENi not connected. All other NAND packages have their ENi pin connected to the previous package's ENo pin in a daisy chain configuration.

Figure 2-35 shows a more complicated topology. This topology illustrates the difference between a Host Target and a NAND Target. Multiple NAND Targets may be connected to a single Host Target (i.e. CE_n signal).

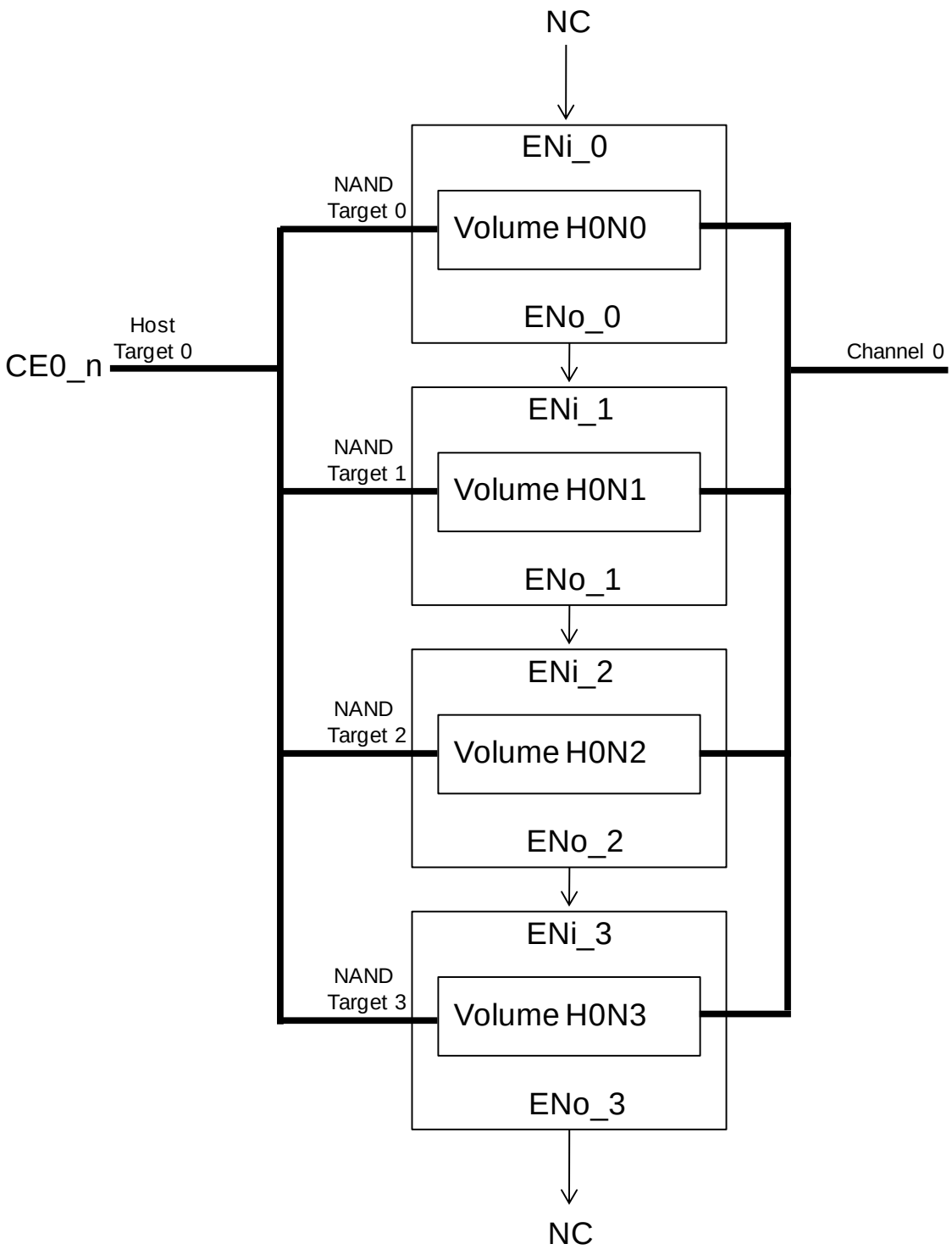


Figure 2-34 CE_n Pin Reduction Topology, example 1

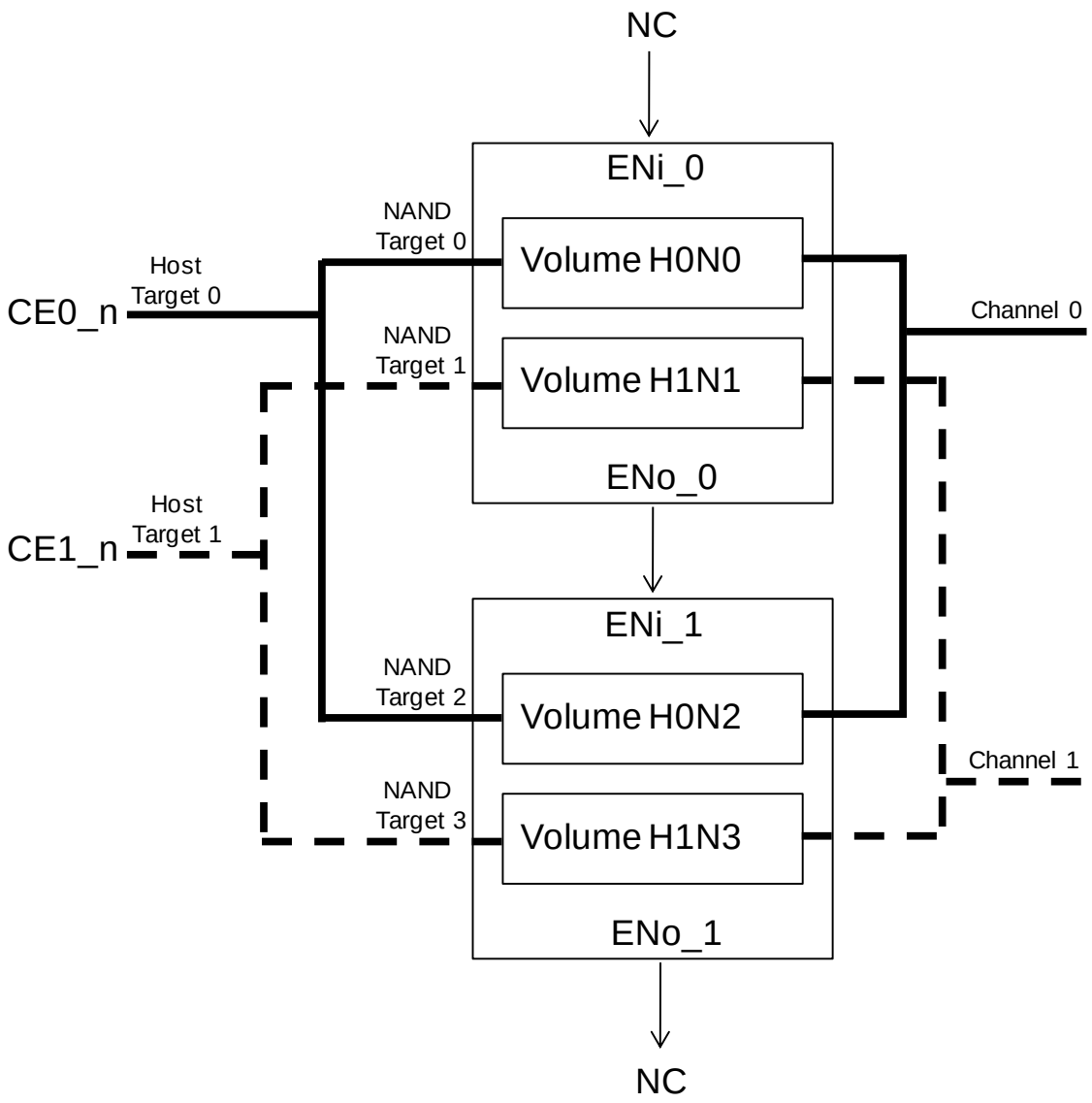


Figure 2-35 CE_n Pin Reduction Topology, example 2

CE_n pin reduction is not supported in all topologies. If two NAND Targets in the same NAND package share the same data bus, then each shall expose a separate CE_n pin external to the NAND package. In this case, the host shall use distinct Host Targets (CE_n signals) with each of these NAND Targets.

The state of ENi determines whether the NAND package is able to accept commands. ENi is pulled high internal to the NAND package. If the ENi pin is high and CE_n is low for the NAND Target, then the NAND Target shall accept commands. If the ENi pin is low for the NAND Target, then the NAND Target shall not accept commands. Note: The first command issued after a power-on is a special case, refer to the initialization sequence in section 3.5.2.

ENo is driven low by the device when CE_n is low and a Volume address is not appointed for the NAND Target. ENo is tri-stated by the device when the CE_n associated with the NAND Target is low and a Volume address is appointed for that NAND Target. When the CE_n signals for all NAND Targets that share an ENo signal are high, ENo is tristated by the device. Note that ENo is

pulled high by the subsequent package's ENi or ENo floats if it is not connected to a subsequent package after a Volume address is appointed.

After a Volume address has been appointed to a NAND Target, it becomes deselected and ignores the ENi pin until the next power cycle.

To be selected to process a command, the Volume Select command shall be issued to the Host Target using the Volume address that was previously appointed. After the CE_n signal is pulled high for tCEH time, all LUNs on a Volume revert to their previous states (refer to section 3.2.4).

2.20.1. Volume Appointment when CE_n Reduction Not Supported

Figure 2-36 shows an example topology that does not implement CE_n reduction. If CE_n reduction is not used (i.e. ENi and ENo are not connected) and the host wants to have the terminator on a package that does not share a CE_n with the selected NAND Target, then each NAND Target that may act as a terminator shall have a Volume appointed at initialization using the Set Features command using the Volume Configuration feature.

Each CE_n shall be individually pulled low and have a unique Volume address appointed. Once all NAND Targets have Volume addresses appointed, the appointed Volume addresses may be used for termination selection.

During operation, the CE_n signal for the selected Volume and for any NAND Targets assigned as a terminator for the selected Volume need to be brought low. When CE_n is brought low for an unselected Volume, all LUNs that are not assigned as terminators for the selected Volume are deselected. When Volume addresses are appointed, the Volume Select command should be used.

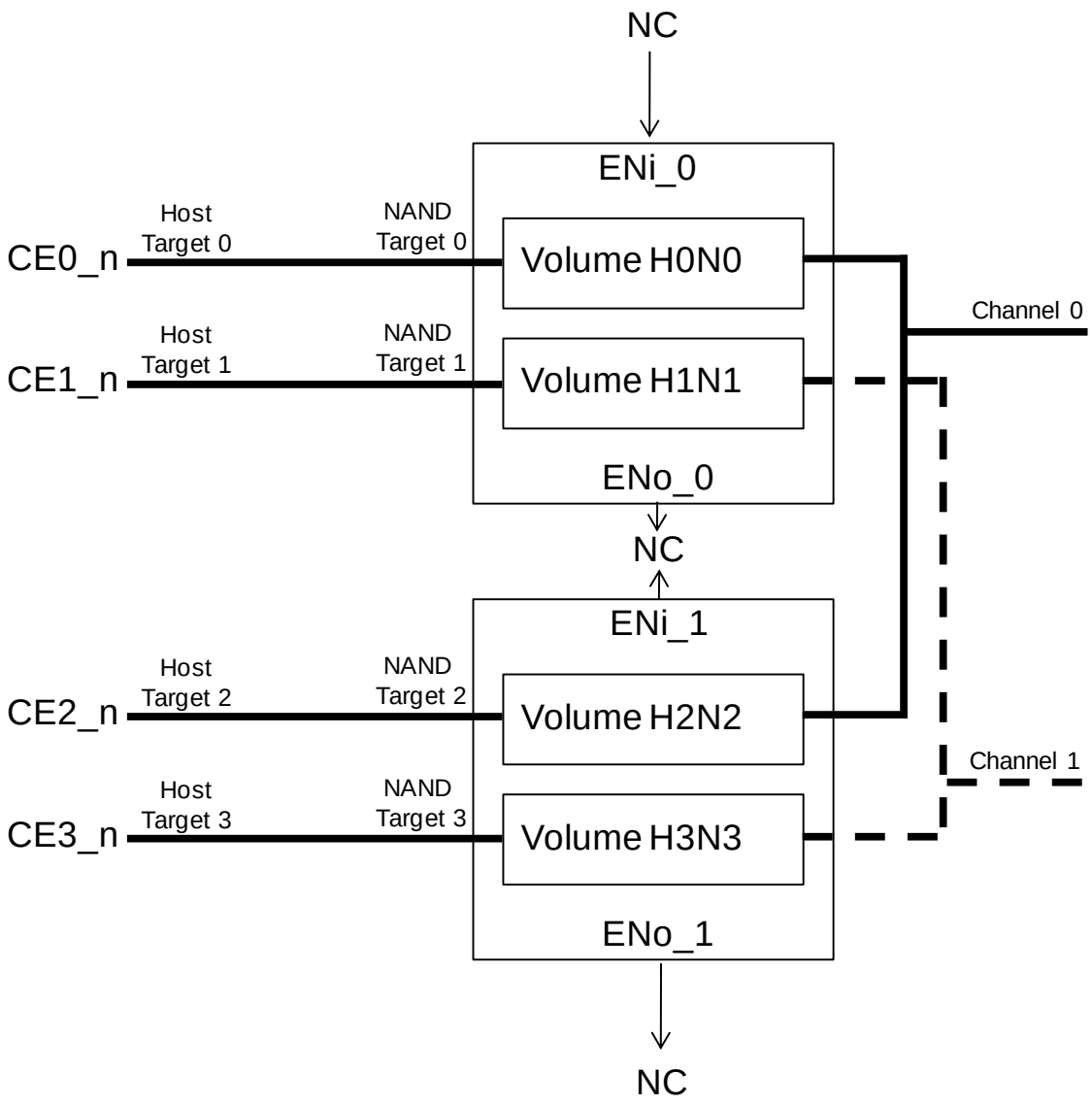


Figure 2-36 Discrete CE_n per package topology

3. Memory Organization

Figure 3-1 shows an example of a Target memory organization. In this case, there are two logical units where each logical unit has two planes.

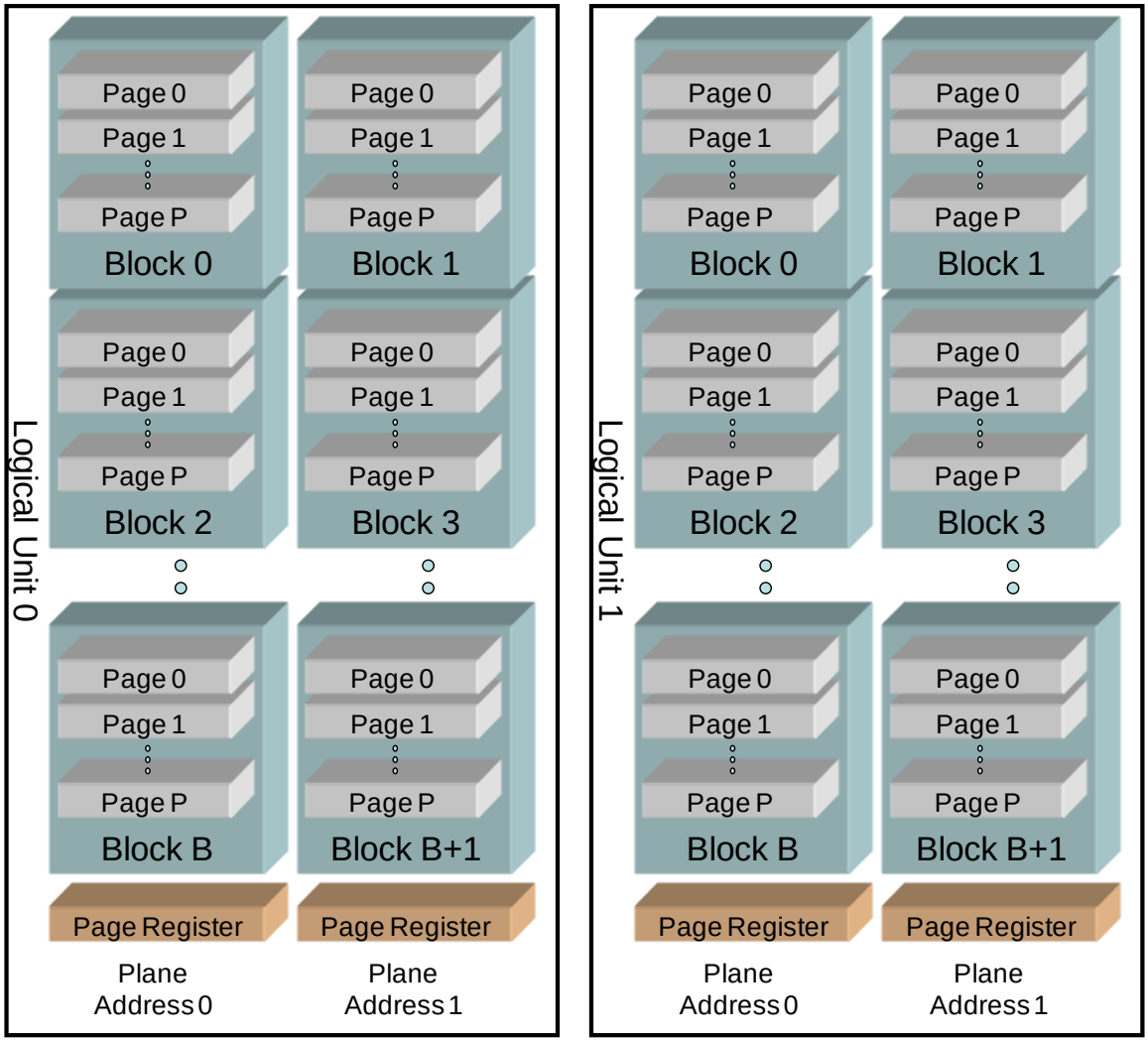


Figure 3-1 Target Memory Organization

A device contains one or more targets. A target is controlled by one CE_n signal. A target is organized into one or more logical units (LUNs).

A logical unit (LUN) is the minimum unit that can independently execute commands and report status. Specifically, separate LUNs may operate on arbitrary command sequences in parallel. For example, it is permissible to start a Page Program operation on LUN 0 and then prior to the operation's completion to start a Read command on LUN 1. See multiple LUN operation restrictions in section 3.1.3. A LUN contains at least one page register and a Flash array. The number of page registers is dependent on the number of multi-plane operations supported for that LUN. The Flash array contains a number of blocks.

A block is the smallest erasable unit of data within the Flash array of a LUN. There is no restriction on the number of blocks within the LUN. A block contains a number of pages.

A page is the smallest addressable unit for read and program operations. A page consists of a number of bytes or words. The number of user data bytes per page, not including the spare data area, shall be a power of two. The number of pages per block shall be a multiple of 32.

Each LUN shall have at least one page register. A page register is used for the temporary storage of data before it is moved to a page within the Flash array or after it is moved from a page within the Flash array.

The byte or word location within the page register is referred to as the column.

There are two mechanisms to achieve parallelism within this architecture. There may be multiple commands outstanding to different LUNs at the same time. To get further parallelism within a LUN, multi-plane operations may be used to execute additional dependent operations in parallel.

3.1. Addressing

There are two address types used: the column address and the row address. The column address is used to access bytes or words within a page, i.e. the column address is the byte/word offset into the page. The least significant bit of the column address shall always be zero in the NV-DDR, NV-DDR2, NV-DDR3 and NV-LPDDR4 data interfaces, i.e. an even number of bytes is always transferred. The row address is used to address pages, blocks, and LUNs.

When both the column and row addresses are required to be issued, the column address is always issued first in one or more 8-bit address cycles. The row addresses follow in one or more 8-bit address cycles. There are some functions that may require only row addresses, like Block Erase. In this case the column addresses are not issued.

For both column and row addresses the first address cycle always contains the least significant address bits and the last address cycle always contains the most significant address bits. If there are bits in the most significant cycles of the column and row addresses that are not used then they are required to be cleared to zero.

The row address structure is shown in Figure 3-2 with the least significant row address bit to the right and the most significant row address bit to the left.

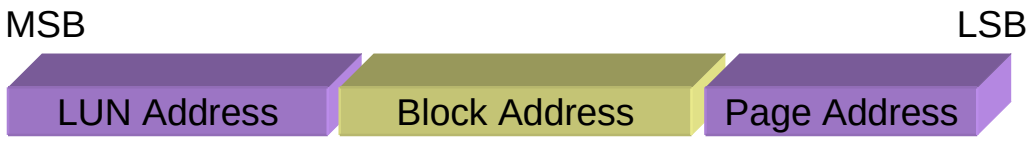


Figure 3-2 Row Address Layout

The number of blocks and number of pages per block is not required to be a power of two. In the case where one of these values is not a power of two, the corresponding address shall be rounded to an integral number of bits such that it addresses a range up to the subsequent power of two value. The host shall not access upper addresses in a range that is shown as not supported. For example, if the number of pages per block is 96, then the page address shall be rounded to 7 bits such that it can address pages in the range of 0 to 127. In this case, the host shall not access pages in the range from 96 to 127 as these pages are not supported.

The page address always uses the least significant row address bits. The block address uses the middle row address bits and the LUN address uses the most significant row address bit(s).

3.1.1. Multi-plane Addressing

The multi-plane address comprises the lowest order bits of the block address as shown in Figure 3-3. The following restrictions apply to the multi-plane address when executing a multi-plane command sequence on a particular LUN:

- The plane address bit(s) shall be distinct from any other multi-plane operation in the multi-plane command sequence.
- Some devices or multi-plane operations may require page addresses to be the same as other multi-plane operations in the multi-plane command sequence. Refer to the vendor datasheet for the multi-plane operation restrictions applicable to the device.

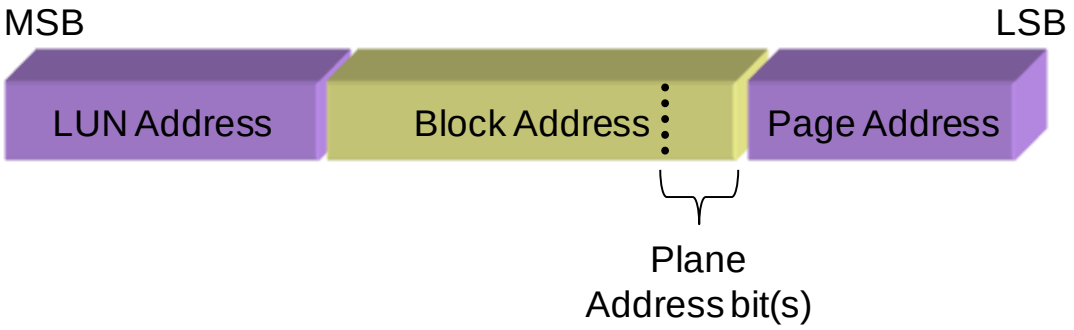


Figure 3-3 Plane Address Location

3.1.1.1. Multi-plane Block Address Restrictions

The device may indicate multi-plane block address restrictions. The specific cases are:

- No restriction: All block address bits may be different between two plane addresses.
- Full restriction: All block address bits (other than the plane address bits) shall be the same between two plane addresses.
- Lower bit XNOR restriction: If the XNOR of the lowest plane address bits (bit 0) is one between two plane addresses, then there is a full restriction between these two plane addresses. If the XNOR of the lower plane address bits is zero between two plane addresses, then there is no restriction between these two plane addresses.

Table 3-1 illustrates the three types of restrictions for a four plane operation.

Restriction Type	Plane Address 0	Plane Address 1	Plane Address 2	Plane Address 3
No restriction	Block A	Block B	Block C	Block D
XNOR restriction	Block A	Block B	Block A+2	Block B+2
Full restriction	Block A	Block A+1	Block A+2	Block A+3

Table 3-1 Four plane address restriction

Table 3-2 describes whether there is a lower bit XNOR restriction between two plane addresses A and B, based on their plane address bits for a 4 plane implementation. If there is a lower bit XNOR restriction, then the block addresses (other than the plane address bits) shall be the same between multi-plane addresses A and B.

Multi-plane Address bits A	Multi-plane Address bits B	Lower Bit XNOR	XNOR Restriction Between A and B
00b	01b	0 XNOR 1 = 0	No
00b	10b	0 XNOR 0 = 1	Yes
00b	11b	0 XNOR 1 = 0	No
01b	10b	1 XNOR 0 = 0	No
01b	11b	1 XNOR 1 = 1	Yes
10b	11b	0 XNOR 1 = 0	No

Table 3-2 4-way lower bit XNOR restriction

3.1.2. Logical Unit Selection

Logical units that are part of a NAND Target share a single data bus with the host. The host shall ensure that only one LUN is selected for data output to the host at any particular point in time to avoid bus contention.

The host selects a LUN for future data output by issuing a Read Status Enhanced command to that LUN. The Read Status Enhanced command shall deselect the output path for all LUNs that are not addressed by the command. The page register selected for output within the LUN is determined by the previous Read (Cache) commands issued and is not impacted by Read Status Enhanced.

3.1.3. Multiple LUN Operation Restrictions

LUNs are independent entities. A multiple LUN operation is one in which two or more LUNs are simultaneously processing commands. During multiple LUN operations the individual LUNs involved may be in any combination of busy or ready status

When a Page Program command (80h) is issued on any LUN that is not preceded by an 11h command, all idle LUNs may clear their page registers if the program page register clear enhancement is not supported or enabled. Thus, the host should not begin a Page Program command on a LUN while a Read Page operation is either ongoing or has completed but the data has not been read from another LUN, as the contents of the page register for the Read operation are lost. A Read Page can be issued to one LUN while a Page Program is ongoing within a second LUN without any restriction. If the program page register clear enhancement is enabled, this restriction does not apply.

When issuing a Page Program command (80h), the host should not select another LUN within the same Volume until after all data has been input and a 10h or 15h command has been issued. In the case of multi-plane operations, all data input for all multi-plane addresses should be completed prior to selecting another LUN.

When issuing Reads to multiple LUNs, the host shall take steps to avoid issues due to column address corruption. The host shall issue a Change Read Column before starting to read out data from a newly selected LUN.

If a multiple LUN operation has been issued, then the next status command issued shall be Read Status Enhanced. Read Status Enhanced causes LUNs that are not selected to turn off their output buffers. This ensures that only the LUN selected by the Read Status Enhanced command responds to a subsequent data output cycle. After a Read Status Enhanced command has been

completed, the Read Status command may be used until the next multiple LUN operation is issued.

When the host has issued Read Page commands to multiple LUNs at the same time, the host shall issue Read Status Enhanced before reading data from either LUN. This ensures that only the LUN selected by the Read Status Enhanced command responds to a data output cycle after being put in data output mode with a 00h command, and thus avoiding bus contention (NOTE: Some NAND vendors may require the use of Change Read Column Enhanced sequence instead of 00h command to output data from the NAND, see vendor datasheet). A Change Read Column (Enhanced) command is required for any LUN that Read Page commands are outstanding for prior to transferring data from that LUN that is part of the multiple LUN read sequence. An example sequence is shown below:

1) Read Page command issued to LUN 0
2) Read Page command issued to LUN 1
3) Read Status Enhanced selects LUN 0
4) Change Read Column (Enhanced) issued to LUN 0
5) Data transferred from LUN 0
6) Read Status Enhanced selects LUN 1
7) Change Read Column (Enhanced) issued to LUN 1
8) Data transferred from LUN 1

When issuing mixed combinations of commands to multiple LUNs (e.g. Reads to one LUN and Programs to another LUN), after the Read Status Enhanced command is issued to the selected LUN a Change Read Column or Change Read Column Enhanced command shall be issued prior to any data output from the selected LUN.

Support for Read Status Enhanced followed by Change Read Column is optional and a NAND vendor may require the use of either Change Read Column Enhanced command or a Read Status Enhanced command followed by a Change Read Column Enhanced sequence, instead. Refer to the vendor datasheet.

3.2. Volume Addressing

3.2.1. Appointing Volume Address

To appoint a Volume address, the Set Feature command is issued with a Feature Address of Volume Configuration. Refer to section 5.31.7. The Volume address is not retained across power cycles, and thus if Volume addressing is going to be used it needs to be appointed after each power-on prior to use of the NAND device(s).

3.2.2. Selecting a Volume

After Volume addresses have been appointed, every NAND Target (and associated LUN) is selected when the associated CE_n is pulled low. The host issues a Volume Select command to indicate the Volume (i.e. NAND Target) that shall execute the next command issued. Refer to section 5.24.

3.2.3. Multiple Volume Operations Restrictions

Volumes are independent entities. A multiple Volume operation is when two or more Volumes are simultaneously processing commands. Before issuing a command to an unselected Volume, CE_n shall be pulled high for a minimum of tCEH and the Volume Select command shall then be issued to select the Volume to issue a command to next. While commands (including multi-LUN

operations) are being performed on the selected Volume, a Volume Select command is not required.

Issuing the same command to multiple Volumes at the same time is not supported.

For a LUN level command (e.g. Read, Program), the host may select a different Volume during a data input or data output operation and then resume the data transfer operation at a later time for a LUN level command, however for devices that support >800 MT/s, when interrupting data input operations with a Volume Select command, the host may be required to issue an 11h command prior to the Volume Select command (see vendor datasheet). When re-selecting a Volume and associated LUN to complete the data input or data output operation, the following actions are required:

- Data input: The host shall wait tCCS and then issue a Change Row Address command prior to resuming data input. If Change Row Address is not supported, then all data shall be transferred before selecting a new Volume.
- Data output: The host shall issue a Change Read Column Enhanced or Random Data Out command prior to resuming data output. If neither of these commands is supported, then all data shall be transferred before selecting a new Volume.

For a Target level command (e.g. Get Features, Set Features), the host shall complete all data input or data output operations associated with that command prior to selecting a new Volume.

A Volume Select command shall not be issued during the following atomic portions of the Read, Program, Erase, and Copyback operations:

- Read (including Copyback Read)
  - <CMD: 00h> <ADDR: Column & Row> <CMD: 30h>
  - <CMD: 00h> <ADDR: Column & Row> <CMD: 31h>
  - <CMD: 00h> <ADDR: Column & Row> <CMD: 32h>
  - <CMD: 00h> <ADDR: Column & Row> <CMD: 35h>

- Program (including Copyback Program) **NOTE:** The Volume Select command may be issued prior to the 10h, 11h, or 15h command if the next command to this Volume is Change Row Address, however for devices supporting >800 MT/s, an 11h command may be required prior to the Volume Select command (see vendor datasheet). After Volume Select command is issued to resume data input, the host shall wait tCCS before issuing Change Row Address command.
  - <CMD: 80h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 10h>
  - <CMD: 80h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 11h>
  - <CMD: 80h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 15h>
  - <CMD: 81h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 10h>
  - <CMD: 81h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 11h>
  - <CMD: 81h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 15h>
  - <CMD: 85h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 10h>
  - <CMD: 85h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 11h>
  - <CMD: 85h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 15h>

- Erase
  - <CMD: 60h> <ADDR: Row> <CMD: D0h>
  - <CMD: 60h> <ADDR: Row> <CMD: D1h>
  - <CMD: 60h> <ADDR: Row> <CMD: 60h> <ADDR: Row> <CMD: D1h>

3.2.4. Volume Reversion

When using Volume addressing, the LUNs shall support Volume reversion. Specifically, if CE_n is transitioned from high to low and a Volume Select is not the first command, then the LUN shall revert to the previously Selected, Sniff, and Deselected states (defined in Table 4-59) based on the last specified Volume address. If on-die termination is enabled when using the NV-DDR2 NV-DDR3 or NV-LPDDR4 data interface, there are additional actions described in section 4.17.

Figure 3-4 defines the Volume reversion requirements when CE_n transitions from high to low.

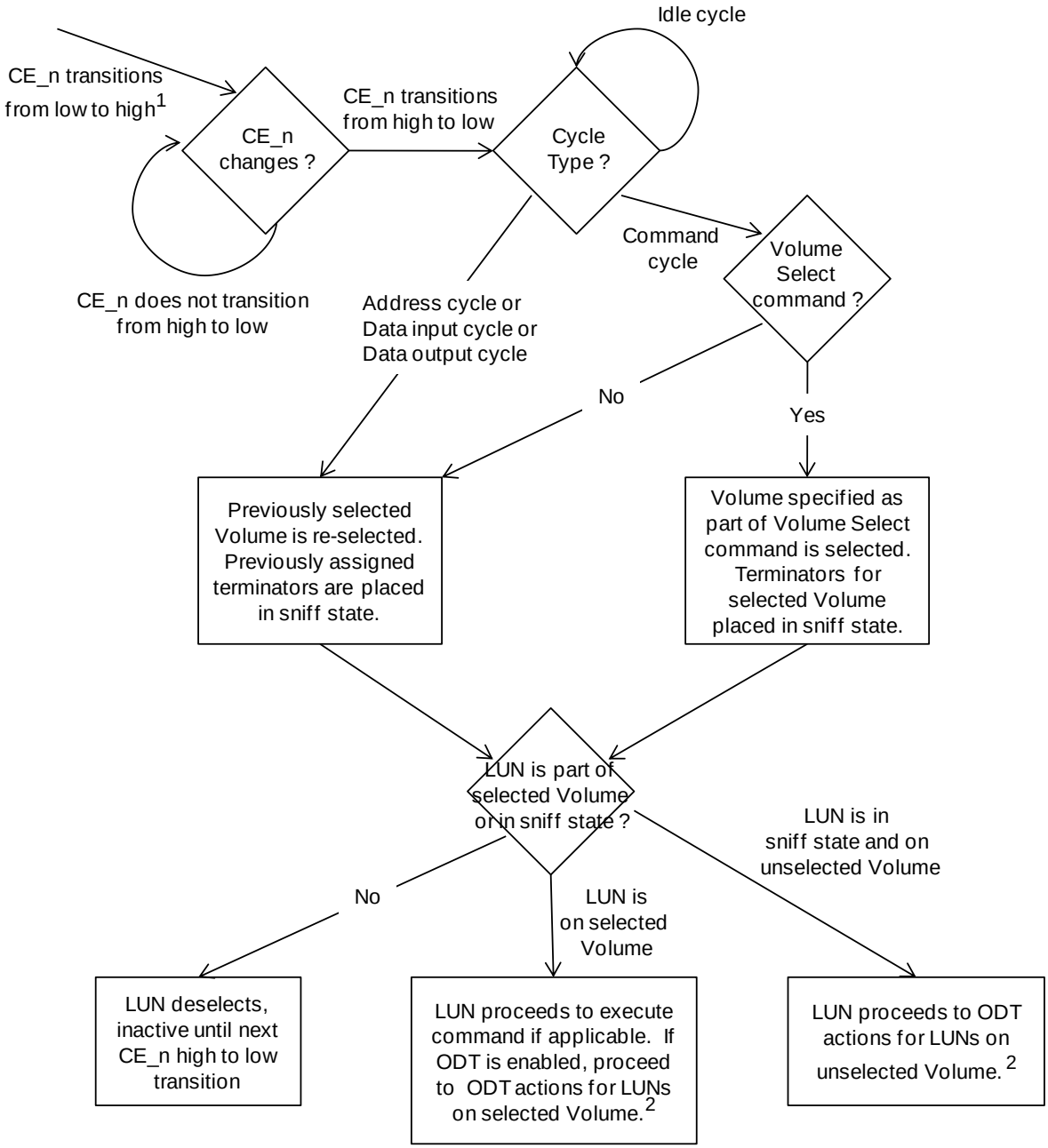


Figure 3-4 Volume Reversion Behavioral Flow

NOTE:
1. This state is entered asynchronously when CE_n transitions from low to high.
2. ODT actions for LUNs on a selected Volume are specified in Figure 4-18
3. ODT actions for LUNs on an unselected Volume are specified in Figure 4-19

3.3. Factory Defect Mapping

The Flash array is not presumed to be pristine, and a number of defects may be present that renders some blocks unusable. Block granularity is used for mapping factory defects since those defects may compromise the block erase capability.

3.3.1. Device Requirements

If a block is defective and 8-bit data access is used, the manufacturer shall mark the block as defective by setting the first byte in the defect area, as shown in Figure 3-5, of the first or last page of the defective block to a value of 00h. If a block is defective and 16-bit data access is used, the manufacturer shall mark the block as defective by setting the first word in the defect area of the first or last page of the defective block to a value of 0000h.

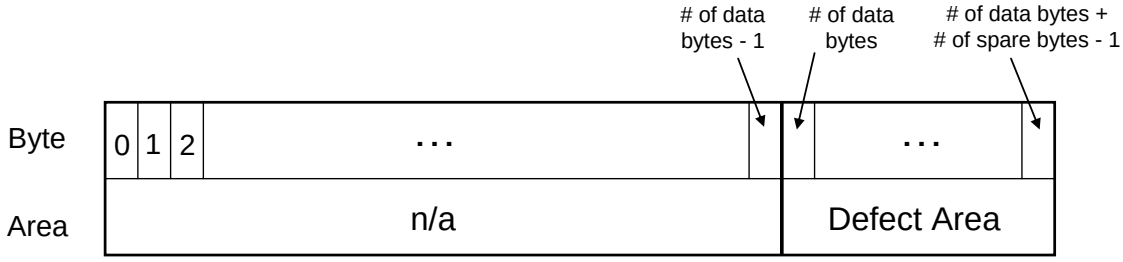


Figure 3-5 Area marked in factory defect mapping

3.3.2. Host Requirements

The host shall not erase or program blocks marked as defective by the manufacturer, and any attempt to do so yields indeterminate results.

Figure 3-6 outlines the algorithm to scan for factory mapped defects. This algorithm should be performed by the host to create the initial bad block table prior to performing any erase or programming operations on the target. The initial state of pages in non-defective blocks is vendor specific although the data at the locations of the bad block mark for non-defective blocks shall not be 00h. A defective block is indicated by a byte value equal to 00h for 8-bit access or a word value equal to 0000h for 16-bit access being present at the first byte/word location in the defect area of either the first page or last page of the block. The host shall check the first byte/word of the defect area of both the first and last past page of each block to verify the block is valid prior to any erase or program operations on that block.

NOTE: Over the lifetime use of a NAND device, the defect area of defective blocks may encounter read disturbs that cause values to change. The manufacturer defect markings may change value over the lifetime of the device and are expected to be read by the host and used to create a bad block table during initial use of the part.

```
for (i=0; i<NumLUNs; i++)
{
      for (j=0; j<BlocksPerLUN; j++)
      {
            Defective=FALSE;

            ReadPage(lun=i; block=j; page=0; DestBuff=Buff);
            if (Buff[PageSize] == 00h)  // Value checked for is 0000h for 16-bit access
                  Defective=TRUE;

            ReadPage(lun=i; block=j; page=PagesPerBlock-1; DestBuff=Buff);
            if (Buff[PageSize] == 00h)  // Value checked for is 0000h for 16-bit access
                  Defective=TRUE;

            if (Defective)
                  MarkBlockDefective(lun=i; block=j);
      }
}
```

Figure 3-6 Factory defect scanning algorithm

3.4. Extended ECC Information Reporting

The device may report extended ECC information in the extended parameter page. The required ECC correctability is closely related to other device parameters, like the number of valid blocks and the number of program/erase cycles supported. Extended ECC information allows the device to specify multiple valid methods for using the device.

Table 3-3 defines the extended ECC information block.

Byte	Definition
0	Number of bits ECC correctability
1	Codeword size
2-3	Bad blocks maximum per LUN
4-5	Block endurance
6-7	Reserved

Table 3-3 Extended ECC Information Block Definition

The definition of each field follows in the subsequent sections.

3.4.1. Byte 0: Number of bits ECC correctability

This field indicates the number of bits that the host should be able to correct per codeword. The codeword size is reported in byte 1. With this specified amount of error correction by the host, the

target shall achieve the block endurance specified in bytes 4-5. When the specified amount of error correction is applied by the host and the block endurance is followed, then the maximum number of bad blocks specified in bytes 2-3 shall not be exceeded by the device. All used bytes in the page shall be protected by host controller ECC including the spare bytes if the ECC requirement reported in byte 0 has a value greater than zero.

When this value is cleared to zero, the target shall return valid data if the ECC Information Block is valid (the Codeword size is non-zero).

3.4.2. Byte 1: Codeword size

The number of bits of ECC correctability specified in byte 0 is based on a particular ECC codeword size. The ECC codeword size is specified in this field as a power of two. The minimum value that shall be reported is 512 bytes (a value of 9).

If a value of 0 is reported then this ECC Information Block is invalid and should not be used.

3.4.3. Byte 2-3: Bad blocks maximum per LUN

This field contains the maximum number of blocks that may be defective at manufacture and over the life of the device per LUN. The maximum rating assumes that the host is following the block endurance requirements and the ECC requirements reported in this extended ECC information block.

3.4.4. Byte 4-5: Block endurance

This field indicates the maximum number of program/erase cycles per addressable page/block. This value assumes that the host is using the ECC correctability reported in byte 0.

The block endurance is reported in terms of a value and a multiplier according to the following equation: value x $10^{multiplier}$. Byte 4 comprises the value. Byte 5 comprises the multiplier. For example, a block endurance of 75,000 cycles would be reported as a value of 75 and a multiplier of 3 (75 x 10^3). The value field shall be the smallest possible; for example 100,000 shall be reported as a value of 1 and a multiplier of 5 (1 x 10^5).

3.5. Discovery and Initialization

3.5.1. Discovery without CE_n pin reduction

This section describes CE_n discovery when the CE_n pin reduction technique described in section 2.20 is not used. If CE_n pin reduction is being used, then the initialization sequence described in section 3.5.2 shall be followed.

There may be multiple chip enable (CE_n) signals on a package, one for each separately addressable target. To determine the targets that are connected, the procedure outlined in this section shall be followed for each distinct CE_n signal. CE_n signals shall be used sequentially on the device; CE0_n is always connected and CE_n signals shall be connected in a numerically increasing order. The host shall attempt to enumerate targets connected to all host CE_n signals.

The discovery process for a package that supports independent dual data buses includes additional steps to determine which data bus the target is connected to. The LGA, 100-ball BGA, and 152-ball BGA packages with 8-bit data access are the packages within ONFI that have a dual

data bus option. The BGA-316 and BGA-272 packages with 8-bit data access are the packages within ONFI that have a quad data bus option.

3.5.1.1. Single Data Bus Discovery

The CE_n to test is first pulled low by the host to enable the target if connected, while all other CE_n signals are pulled high. The host shall then issue the Reset (FFh) command to the target. Following the reset, the host should then issue a Read ID command to the target. If the ONFI signature is returned by the Read ID command with address 20h, then the corresponding target is connected. If the ONFI signature is not returned or any step in the process encountered an error/timeout, then the CE_n is not connected and no further use of that CE_n signal shall be done.

3.5.1.2. Dual/Quad Data Bus Discovery

The CE_n to test is first pulled low by the host to enable the target if connected, while all other CE_n signals are pulled high. The host shall then issue the Reset (FFh) command to the target. Following the reset, the host should then issue a Read ID command with address 20h to the target. If the ONFI signature is returned by the Read ID command, then the corresponding target is connected.

If the ONFI signature is not returned (or any step in the process encountered an error/timeout), then the second 8-bit data bus should be probed. The host shall issue the Reset (FFh) command to the target using the second 8-bit data bus. Following the reset, the host should then issue a Read ID command with address 20h to the target on the second 8-bit data bus. If the ONFI signature is returned by the Read ID command, then the corresponding target is connected and is using the second 8-bit data bus. After discovering that the target is using the second 8-bit data bus, all subsequent commands to that target shall use the second 8-bit data bus including Read Parameter Page. If the ONFI signature is not returned for the second 8-bit data bus, the discovery process described for the second 8-bit data bus should be repeated for the third and fourth 8-bit data busses.

If after this point a valid ONFI signature is not discovered or further errors were encountered, then the CE_n is not connected and no further use of that CE_n signal shall be done.

3.5.2. Discovery with CE_n pin reduction

After power-on the host may issue a Reset (FFh) to all NAND Targets in parallel on the selected Host Target, or the host may sequentially issue Reset (FFh) to each NAND Target connected to a particular Host Target. The methodology chosen depends on host requirements for maximum current draw. To reset all NAND Targets in parallel, the host issues a Reset (FFh) as the first command issued to the NAND device(s). To reset NAND Targets sequentially, the host issues a Read Status (70h) command as the first command issued to all NAND Targets on the selected Host Target.

In cases where there are multiple NAND Targets within a package, those NAND Targets share the same ENo signal. When multiple NAND Targets share an ENo signal, the host shall not stagger Set Feature commands that appoint the Volume addresses. If the Set Feature commands are not issued simultaneously then the host shall wait until Volume appointment for previous NAND Target(s) is complete before issuing the next Set Feature command to appoint the Volume address for the next NAND Target that shares the ENo signal within a package.

After issuing the Set Feature command to appoint the Volume address, the host shall not issue another command to any NAND Target on the associated Host Target (including status commands) until after the tFEAT time has elapsed. This is to ensure that the proper NAND Target responds to the next command, allowing for the proper ENo/ENi signal levels to be reflected.

The initialization sequence when using CE_n pin reduction is as follows:

1. Power is applied to the NAND device(s).
2. CE_n (Host Target) is pulled low.
3. If resetting all NAND Targets in parallel, then the host issues the Reset (FFh) command. This command is accepted by all NAND Targets connected to the CE_n (Host Target).
4. If resetting each NAND Target sequentially, then:
    a. Host issues Read Status (70h) command. Issuing Read Status (70h) prior to any other command indicates sequential Reset (FFh) of each NAND Target.
    b. Host issues Reset (FFh). This command only resets the NAND Target connected to the CE_n (Host Target) whose ENi signal is high.
5. Host issues Read Status (70h) command and waits until SR[6] is set to one.
6. Host configures the NAND Target. Read ID, Read Parameter Page, and other commands are issued as needed to configure the NAND Target.
7. Set Feature with a Feature Address of Volume Configuration is issued to appoint the Volume address for the NAND Target(s) whose ENi signal is high. The Volume address specified shall be unique amongst all NAND Targets. After the Set Features command completes, ENo is pulled high and the Volume is deselected until a Volume Select command is issued that selects the Volume. The host shall not issue another command to a NAND Target connected to the associated Host Target until after tFEAT time has elapsed.
8. For each NAND Target connected to the Host Target, steps 4-7 are repeated for the sequential initialization sequence and steps 5-7 for the parallel initialization sequence.
9. When no further NAND Targets are found connected to the Host Target, then repeat steps 2-8 for the next Host Target (i.e. host CE_n signal).
10. To complete the initialization process, a Volume Select command is issued following a CE_n transition from high to low to select the next Volume that is going to execute a command.

After Volume addresses have been appointed, the host may complete any additional initialization tasks (e.g. configure on-die termination for NV-DDR2, NV-DDR3 or NV-LPDDR4) and then proceed with normal operation.

The host CE_n signal shall be kept low for steps 2-7. If the host CE_n signal that is pulled low for steps 2-7 is brought high anytime after step 7 but before the initialization process is complete then tCS (i.e. CE_n setup time) for SDR timing mode 0 shall be used.

Figure 3-7 shows a timing diagram for a Sequential Reset initialization based on topology in Figure 2-35.

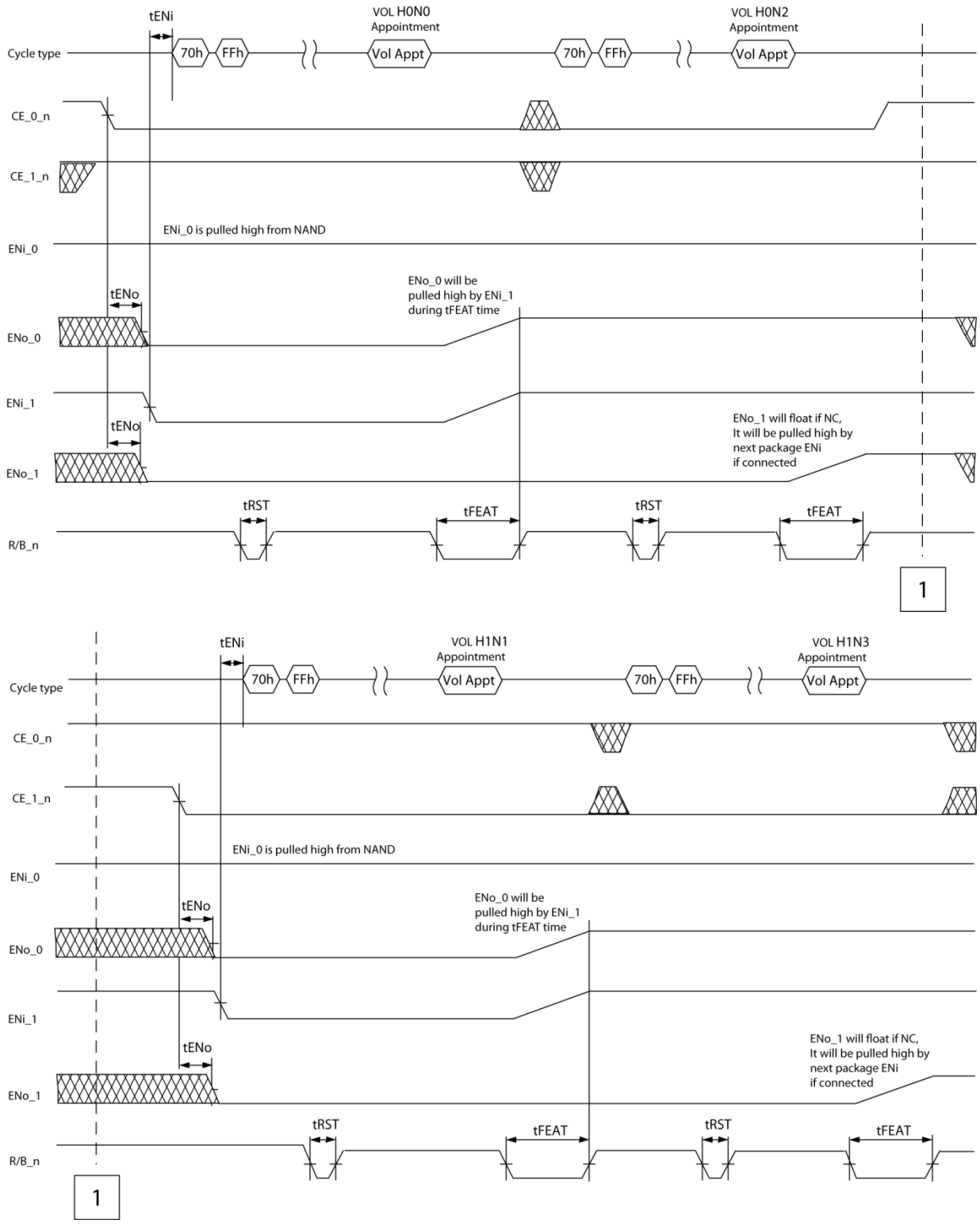


Figure 3-7 Example of Sequential Reset Initialization of Figure 2-35 Topology

3.5.3. Target Initialization

To initialize a discovered target, the following steps shall be taken. The initialization process should be followed for each connected CE_n signal, including performing the Read Parameter Page (ECh) command for each target. Each chip enable corresponds to a unique target with its own independent properties that the host shall observe and subsequently use.

The host should issue the Read Parameter Page (ECh) command. This command returns information that includes the capabilities, features, and operating parameters of the device. When the information is read from the device, the host shall check the CRC to ensure that the data was received correctly and without error prior to taking action on that data.

If the CRC of the first parameter page read is not valid (refer to section 5.7.1.42), the host should read redundant parameter page copies. The host can determine whether a redundant parameter page is present or not by checking if the first four bytes contain at least two bytes of the parameter page signature. If the parameter page signature is present, then the host should read the entirety of that redundant parameter page. The host should then check the CRC of that redundant parameter page. If the CRC is correct, the host may take action based on the contents of that redundant parameter page. If the CRC is incorrect, then the host should attempt to read the next redundant parameter page by the same procedure.

The host should continue reading redundant parameter pages until the host is able to accurately reconstruct the parameter page contents. All parameter pages returned by the Target may have invalid CRC values; however, bit-wise majority or other ECC techniques may be used to recover the contents of the parameter page. The host may use bit-wise majority or other ECC techniques to recover the contents of the parameter page from the parameter page copies present. When the host determines that a parameter page signature is not present (refer to section 5.7.1.1), then all parameter pages have been read.

The Read ID and Read Parameter Page commands only use the lower 8-bits of the data bus. The host shall not issue commands that use a word data width on x16 devices until the host determines the device supports a 16-bit data bus width in the parameter page.

After successfully retrieving the parameter page, the host has all information necessary to successfully communicate with that target. If the host has not previously mapped defective block information for this target, the host should next map out all defective blocks in the target. The host may then proceed to utilize the target, including erase and program operations.

4. Data Interface and Timing

4.1. Data Interface Type Overview

ONFI supports five different data interface types: SDR, NV-DDR, NV-DDR2, NV-DDR3 and NV-LPDDR4. The SDR data interface is the traditional NAND interface that uses RE_n to latch data read, WE_n to latch data written, and does not include a clock. The NV-DDR data interface is double data rate (DDR), includes a clock that indicates where commands and addresses should be latched, and a data strobe that indicates where data should be latched. The NV-DDR2 data interface is double data rate (DDR) and includes additional capabilities for scaling speed like on-die termination and differential signaling. The NV-DDR3 data interface includes all NV-DDR2 features but operates at VccQ=1.2V. The NV-LPDDR4 data interface uses LTT electrical signaling and operates at VccQ=1.2V.A feature comparison of the data interfaces is shown in Table 4-1.

Feature	Data Interface				
	SDR	**NV-DDR**	**NV-DDR2**	**NV-DDR3**	**NV-LPDDR4**
Protocol	Single data rate (SDR)	Double data rate (DDR)	Double data rate (DDR)	Double data rate (DDR)	Double data rate (DDR)
Maximum Speed		200 MT/s	800 MT/s	3600[1] MT/s	3600[1] MT/s
CE_n Pin Reduction support	Yes	Yes	Yes	Yes	Yes
Volume Addressing support	Yes	Yes	Yes	Yes	Yes
On-die termination support	No	No	Yes	Yes	Yes
Differential signaling	No	No	Yes, optional for DQS and/or RE_n	Yes, optional for DQS and/or RE_n	Yes, required for DQS and/or RE_n
VccQ support	3.3 V or 1.8 V	3.3 V or 1.8 V	1.8 V	1.2 V	1.2 V
External Vpp support	Yes	Yes	Yes	Yes	Yes
External VREFQ support	No	No	Yes	Yes	No
ZQ Calibration	No	No	Yes, optional	Yes, optional	Yes, required
Previous name in older ONFI specifications	Asynchronous	Source Synchronous	n/a	n/a	n/a
Input Path Topology	n/a	Matched DQS	Matched DQS	Matched DQS or Unmatched DQS[2]	Matched DQS or Unmatched DQS[2]
Differential Signaling enabled on Power-up	Disabled	Disabled	Disabled	Yes, optional[2]	Yes, optional[2]
Equalization	No	No	No	Yes, optional[2]	Yes, optional[2]
Training	No	No	No	Write/Read DQ/DCC/ Internal VrefQ WDCA (optional) Write Training Monitor (optional)	Write/Read DQ/DCC/ Internal VrefQ WDCA (optional) Write Training Monitor (optional)

				Per-pin VrefQ Adjustment (optional)	Per-pin VrefQ Adjustment (optional)

Notes:
1. The maximum timing mode a NAND device supports is vendor specific (See vendor datasheet)
2. Vendor Specific (See Vendor Datasheet)

Table 4-1 Data Interface Comparison

Feature			~200 MT/s	~400 MT/s	~800 MT/s	~1200 MT/s, ~1600 MT/s, ~1800 MT/s, ~2000 MT/s, ~2200 MT/s, ~2400 MT/s	~2800 MT/s, ~3200 MT/s, ~3600 MT/s
VccQ			1.2V				
I/O Type	Single-ended Signaling for DQS and RE [1, 2]	NAND	Supported	Not supported			
		Host	Optional				
	Differential Signaling for DQS and RE	NAND	Supported				
		Host	Optional	Required			
ZQ Calibration		NAND	Supported				
		Host	Optional		Required		
Training (DCC)		NAND	Not supported			Required	
		Host					
Training (Read)		NAND	Supported				
		Host	Optional			Required	
Training (Write)		NAND	Supported				
		Host	Optional for Matched DQS NAND, Required for Unmatched DQS NAND			Required for both Unmatched DQS and Matched DQS NAND	
Training (WDCA)		NAND	Optional				
		Host	Optional				
On Die (NAND) Termi-nation	CTT	NAND	Supported				
		Host	Optional [3]				
	LTT	NAND	Supported				
		Host	Optional [3]				

Equalization	NAND	Optional & Vendor Specific
	Host	Optional & Vendor Specific

NOTES

1) For NV-DDR3 mode, the device can be used up to 200Mbps without Differential Signals. To use high speed over 200Mbps, Differential Signals shall be used and asserted before High-speed setting.
2) For NV-LPDDR4 mode, Differential Signaling is always required, even below 200Mbps.
3) Host can enable/disable On Die (NAND) Termination.

Table 4-2 Supported Features and Operating Conditions Versus Data Rate

If VccQ = 1.8V or 3.3V on power-up, the device shall operate in SDR data interface timing mode 0. After the host determines that either the NV-DDR or NV-DDR2 data interface is supported in the parameter page, the host may select the NV-DDR or NV-DDR2 data interface and supported timing mode by using Set Features with a Feature Address of 01h. Refer to section 5.31.1.

If VccQ=1.2V on power up, the device shall operate in NV-DDR3 interface timing mode 0. After the host determines the NV-DDR3 timing modes supported in the parameter page, the host may enable the supported timing mode by transitioning CE_n high and changing the interface speed to the desired timing mode. The new timing mode is active when the host pulls CE_n low. Refer to section 5.31.1.

The NV-DDR, NV-DDR2, NV-DDR3 and NV-LPDDR4 data interfaces use a DDR protocol. Thus, an even number of bytes is always transferred. The least significant bit of the column address shall always be zero when using the DDR protocol. If the least significant bit of the column address is set to one when using the DDR protocol, then the results are indeterminate.

For devices that support >2400 data rates, the NV-DDR3 and NV-LPDDR4 interface implementations have the following options. Please see Vendor datasheets for these optional and/or vendor specific modes support

- Input Path topology: Matched DQS vs Unmatched DQS
- Differential signaling on Power-up: Vendor Specific
- Equalization: Optional and Vendor specific
- Write-Duty-Cycle-Adjustment (WDCA): Optional
- Write Training Monitor: Optional
- Per-Pin Vrefq Adjustment: Optional

4.2. Signal Function Assignment

The function of some signals is different depending on the selected data interface; those differences are described in this section.

For the NV-DDR, NV-DDR2 NV-DDR3 or NV-LPDDR4 data interfaces, the common changes in comparison to the SDR data interface are:

- The I/O bus is renamed to the DQ bus.
- A strobe signal for the DQ data bus, called DQS (DQ strobe), is added. DQS is bi-directional and is used for all data transfers. DQS is not used for command or address cycles. The latching edge of DQS is center aligned to the valid data window for data transfers from the host to the device (writes). The latching edge of DQS is aligned to the transition of the DQ bus for data transfers from the device to the host (reads). DQS should be pulled high by the host and shall be ignored by the device when operating in the SDR data interface.

For the NV-DDR data interface, the changes in comparison to the SDR data interface are:

- WE_n becomes the clock signal (CLK). CLK shall be enabled with a valid clock period whenever a command cycle, address cycle, or data cycle is occurring. CLK shall maintain the same frequency while the CE_n signal is low. Refer to section 2.9.1.
- RE_n becomes the write/read direction signal (W/R_n). This signal indicates the owner of the DQ data bus and the DQS signal. The host shall only transition W/R_n when ALE and CLE are latched to zero. Refer to section 4.20.2.6 for W/R_n requirements.

For the NV-DDR2 and NV-DDR3 data interfaces, the changes in comparison to the SDR data interface are:

- RE_n may be used single-ended or as a complementary signal pair (RE_t, RE_c).
- A strobe signal for the DQ data bus, called DQS (DQ strobe), is added. DQS may be used single-ended or as a complementary signal pair (DQS_t, DQS_c).

For the NV-LPDDR4 data interfaces, the changes in comparison to the SDR data interface are:

- RE_n must be used as a complementary signal pair (RE_t, RE_c).
- A strobe signal for the DQ data bus, called DQS (DQ strobe), is added. DQS must be used as a complementary signal pair (DQS_t, DQS_c).
- An optional data bus invertion signal for the DQ data bus, called DBI_n, is added. DBI_n designates if the DQ signals are inverted by transmitter side or not. DBI_n is regarded as DQ, such that specifications such as AC parameters and Interface training shall be applied to DBI.

Table 4-3 describes the signal functionality based on the selected data interface.

Symbol				Type	Description
SDR	**NV-DDR**	**NV-DDR2 / NV-DDR3**	**NV-LPDDR4**		
ALE	ALE	ALE	ALE	Input	Address latch enable
CE_n	CE_n	CE_n	CE_n	Input	Chip enable
CLE	CLE	CLE	CLE	Input	Command latch enable
I/O[7:0]	DQ[7:0]	DQ[7:0]	DQ[7:0]	I/O	Data inputs/outputs
—	DQS	DQS / DQS_t	DQS / DQS_t	I/O	Data strobe
—	—	DQS_c	DQS_c	I/O	Data strobe complement
RE_n	W/R_n	RE_n / RE_t	RE_n / RE_t	Input	Read enable / (Write / Read_n direction)
—	—	RE_c	RE_c	Input	Read enable complement
WE_n	CLK	WE_n	WE_n	Input	Write enable / Clock
WP_n	WP_n	WP_n	WP_n	Input	Write protect
R/B_n	R/B_n	R/B_n	R/B_n	Output	Ready / Busy_n
—	—	ZQ	ZQ	NA	ZQ calibration
—	—	—	DBI	I/O	Data Bus Inversion

Table 4-3 Signal Assignment based on Data Interface Type

4.3. Bus State

ALE and CLE are used to determine the current bus state in all data interfaces.

4.3.1. SDR

Table 4-4 describes the bus state for SDR. Note that in SDR the value 11b for ALE/CLE is undefined.

CE_n	ALE	CLE	WE_n	RE_n	SDR Bus State
1	X	X	X	X	Standby
0	0	0	1	1	Idle
0	0	1	0	1	Command cycle
0	1	0	0	1	Address cycle
0	0	0	0	1	Data input cycle
0	0	0	1	0	Data output cycle
0	1	1	X	X	Undefined

Table 4-4 Asynchronous Bus State

4.3.2. NV-DDR

Table 4-5 describes the bus state for NV-DDR operation. The value 11b for ALE/CLE is used for data transfers. The bus state lasts for an entire CLK period, starting with the rising edge of CLK. Thus, for data cycles there are two data input cycles or two data output cycles per bus state. The idle bus state is used to terminate activity on the DQ bus after a command cycle, an address cycle, or a stream of data.

The value of CE_n shall only change when the bus state is idle (i.e. ALE and CLE are both cleared to zero) and no data is being transmitted during that clock period.

CE_n	ALE	CLE	W/R_n	CLK	NV-DDR Bus State
1	X	X	X	X	Standby
0	0	0	1	Rising edge to rising edge	Idle[1]
0	0	0	0	Rising edge to rising edge	Bus Driving[1]
0	0	1	1	Rising edge to rising edge	Command cycle
0	1	0	1	Rising edge to rising edge	Address cycle
0	1	1	1	Rising edge to rising edge	Data input cycle[2]
0	1	1	0	Rising edge to rising edge	Data output cycle[2]
0	0	1	0	Rising edge to rising edge	Reserved
0	1	0	0	Rising edge to rising edge	Reserved

NOTE:
1. When W/R_n is cleared to ‘0’, the device is driving the DQ bus and DQS signal. When W/R_n is set to ‘1’ then the DQ and DQS signals are not driven by the device.
2. There are two data input/output cycles from the rising edge of CLK to the next rising edge of CLK.

Table 4-5 NV-DDR Bus State

4.3.3. NV-DDR2, NV-DDR3 and NV-LPDDR4

Table 4-6 describes the bus state for NV-DDR2, NV-DDR3 and NV-LPDDR4 operation.

CE_n	ALE	CLE	RE_n5 (RE_t)	DQS (DQS_t)	WE_n	Data Input or Output[1]	Measurement Point	Bus State
1	X	X	X	X	X	X	X	Standby
0	0	0	1	1	1	None	X	Idle
0	0	1	1	–	–	None	WE_n rising edge to rising edge	Command cycle
0	1	0	1	–	–	None	WE_n rising edge to rising edge	Address cycle
0	0	0	1	–	1	Input	DQS rising edge to rising edge	Data input cycle[2,3]
0	0	0	–	–	1	Output	RE_n rising edge to rising edge	Data output cycle[2,3,4]

NOTE:
1. The current state of the device is data input, data output, or neither based on the commands issued.
2. There are two data input/output cycles from the rising edge of DQS/RE_n to the next rising edge of DQS/RE_n.
3. ODT may be enabled as part of the data input and data output cycles.
4. At the beginning of a data output burst, DQS shall be held high for tDQSRH after RE_n transitions low to begin data output.
5. RE and DQS complementary signals are mandatory for NV-LPDDR4

Table 4-6 NV-DDR2, NV-DDR3 and NV-LPDDR4 Bus State

4.3.4. Pausing Data Input/Output and Restarting an Exited Data Input/Output Sequence

The host may pause data input or data output by entering the Idle state when using any data interface.

In the SDR data interface, pausing data input or data output is done by maintaining WE_n or RE_n at a value of one, respectively.

In the NV-DDR data interface, pausing data input or data output is done by clearing ALE and CLE both to zero. The host may continue data transfer by setting ALE and CLE both to one after the applicable tCAD time has passed.

In the NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface, pausing of data output may be done in the middle of a data output burst by pausing RE_n (RE_t/RE_c) and holding the signal(s) static high or low until the data burst is resumed. The pausing of data input may also be done in the middle of a data input burst by pausing DQS (DQS_t/DQS_c) and holding the signal(s) static high or low until the data burst is resumed. The data burst can be considered paused if DQS (DQS_t/DQS_c) or RE_n (RE_t/RE_c) is paused such that the current I/O frequency is not maintained for the data burst. WE_n shall be held high during data input and output burst pause time. ODT (if enabled) stays ON the entire pause time and warmup cycles (if enabled) are not re-issued when re-starting a data burst from pause.

Pausing in the middle of a data input or data output burst is only allowed up to the 800MT/s data rate. Above 800MT/s, for signal integrity reasons, pausing in the middle of a data input or data output burst is not allowed, and if the data burst is interrupted, the host is required to exit first the data burst prior to resuming it.
A data burst is exited when either ALE or CLE or CE_n is toggled to a 1. After a data burst has been exited, if warmup cycles are enabled, then warmup cycles are required when re-starting the data burst. Refer to section 4.15 for details on re-issuing warmup cycles when exiting and re-starting data bursts. After a data burst has been exited, ODT also may be disabled, however if needed to meet the signal integrity needs of the system, ODT must be re-enabled prior to re-starting the data burst. If the host desires to end the data burst, after exiting the data burst, a new command is issued.

The Figure 4-1 below is an example of exiting a data input burst with a CLE=1 and resuming the data input burst with a CLE=0. Warmup cycles if enabled are required to be issued when the data input burst is resumed.

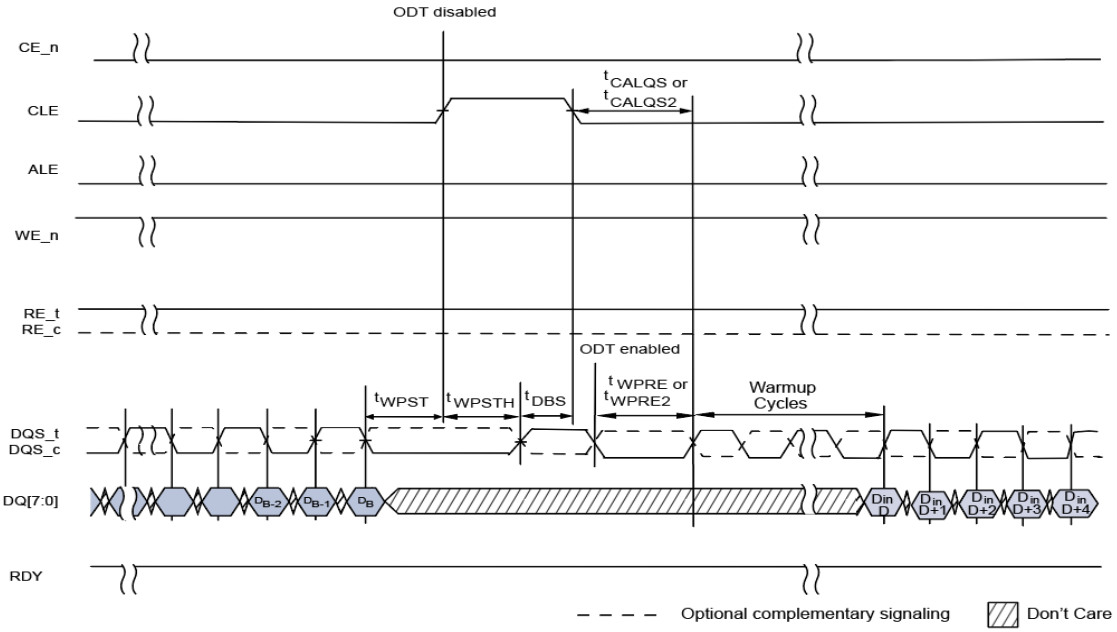


Figure 4-1 Example of Data Input Burst Exit with CLE=1 and Resume with CLE=0

The Figure 4-2 below is an example of exiting a data output burst with a CLE=1 and resuming the data output burst with a CLE=0. Warmup cycles if enabled are required to be issued when the data output burst is resumed.

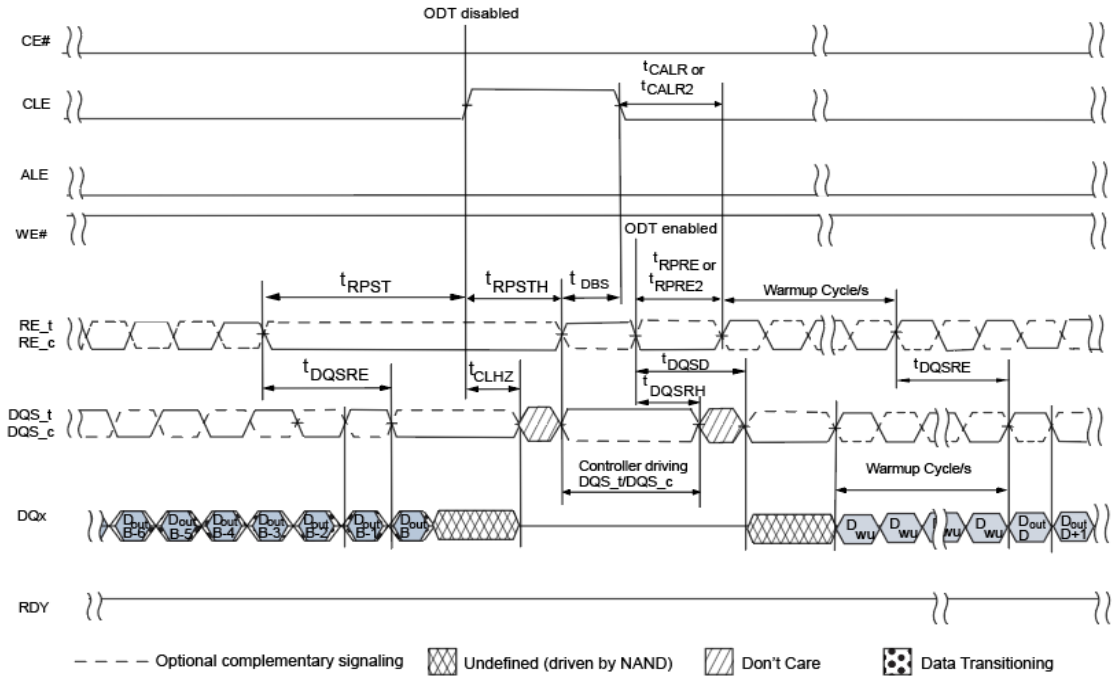


Figure 4-2 Example of Data Output Burst Exit with CLE=1 and Resume with CLE=0

As shown in Figure 4-3, for devices that support >800 MT/s, if the data input burst is exited (with a CLE or ALE or CE_n high) and CE_n is held high for >1us, in order to be able to resume the data input burst at a later time, the host may be required to issue a vendor specific command (e.g. 11h) prior to exiting the data input burst (see vendor datasheet). To restart an exited data input burst where the CE_n has been held high for >1us, a Change Write Column or Change Row Address command shall be issued (see vendor datasheet if both commands or only one of those commands are supported in resuming the data input burst).

As shown in Figure 4-4, for devices that support >800 MT/s, if the data output burst is exited (with a CLE or ALE or CE_n high) and CE_n is held high for >1uS, in order to restart an exited data output burst, the host may be required to issue a Change Read Column or Change Read Column Enhanced command (see vendor datasheet).

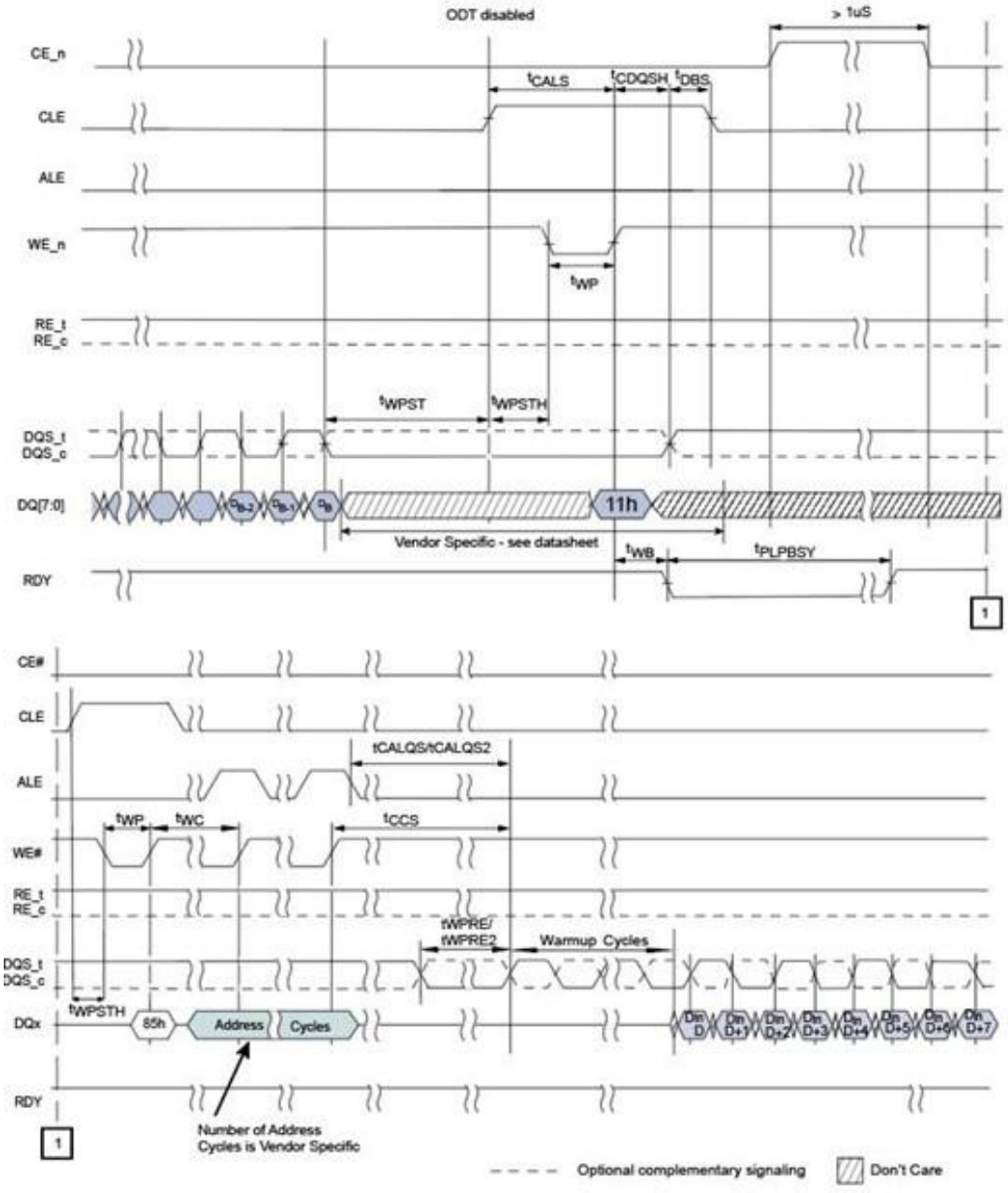


Figure 4-3 Example of Data Input Burst Exit with CE_n High > 1uS and Resume Sequence for Devices that support greater than 800 MT/s

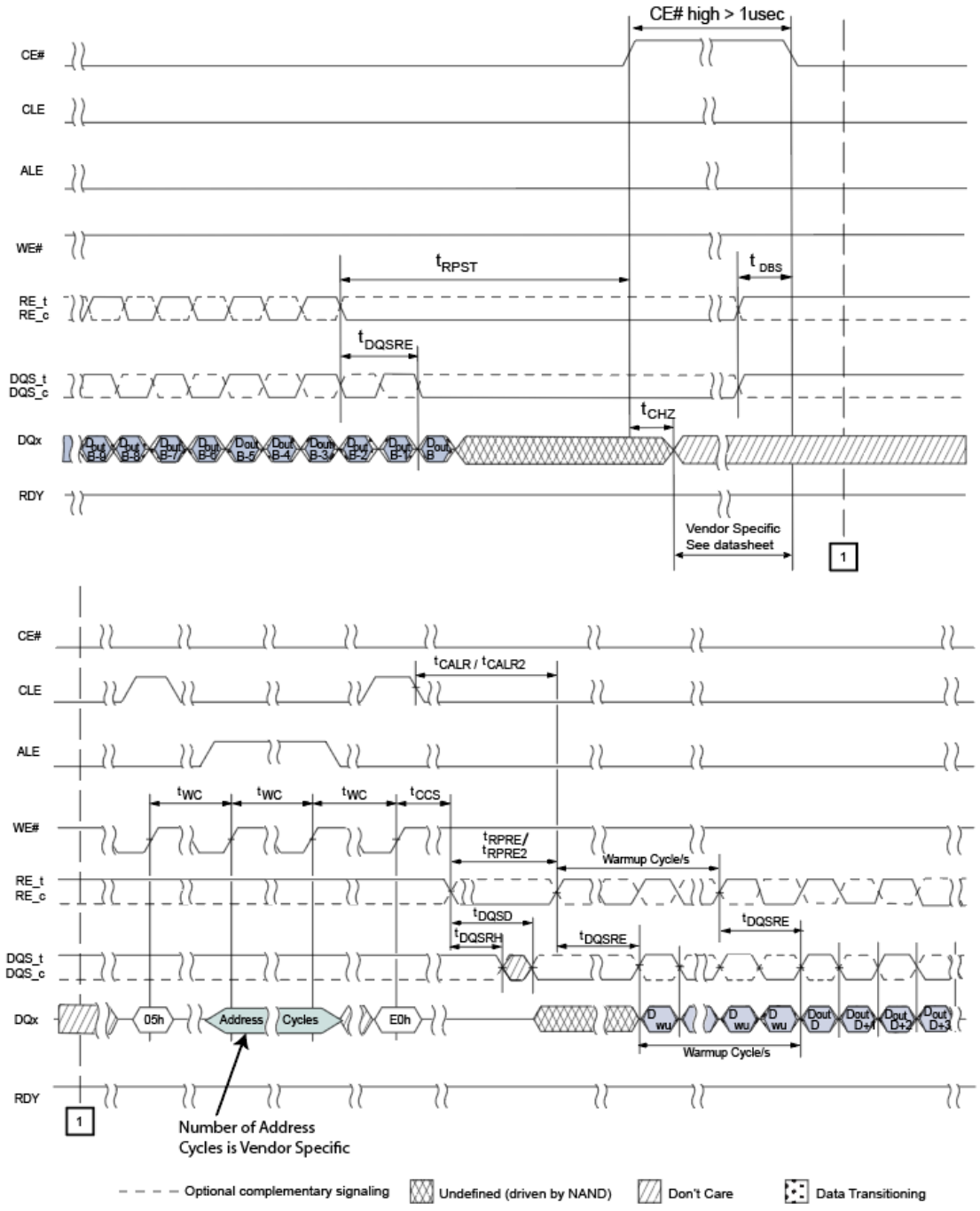


Figure 4-4 Example of Data Output Burst Exit with CE_n High > 1uS and Resume Sequence for Devices that Support greater than 800 MT/s

4.4. NV-DDR / NV-DDR2 / NV-DDR3 / NV-LPDDR4 and Repeat Bytes

The NV-DDR, NV-DDR2, NV-DDR3 and NV-LPDDR4 data interfaces use the DDR data transfer technique to achieve a high data transfer rate. However, certain configuration and settings commands are not often used and do not require a high data transfer rate. Additionally, these commands typically are not serviced by the pipeline used for data transfers.

To avoid adding unnecessary complexity and requirements to implementations for these commands, the data is transferred using single data rate. Specifically, the same data byte is repeated twice and shall conform to the timings required for the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface. The data pattern in these cases is D_0 D_0 D_1 D_1 D_2 D_2 etc. The receiver (host or device) shall only latch one copy of each data byte. Data input or data output, respectively, shall not be paused during these commands. The receiver is not required to wait for the repeated data byte before beginning internal actions.

The commands that repeat each data byte twice in the NV-DDR, NV-DDR2, NV-DDR3 and NV-LPDDR4 data interfaces are: Set Features, Read ID, Get Features, Read Status, Read Status Enhanced, and ODT Configure. SDR commands may use the highest data transfer rate supported by the device. If an ODT Configure command is not issued using SDR timing mode 0 then host shall wait 40ns prior to issuing the next command cycle.

4.5. Data Interface / Timing Mode Transitions

The following transitions between data interface are supported:

- SDR to NV-DDR
- SDR to NV-DDR2
- NV-DDR to SDR
- NV-DDR2 to SDR
- NV-DDR3 to NV-LPDDR4

Transitions from NV-DDR directly to NV-DDR2 (or vice versa) is not supported. In this case, the host should transition to the SDR data interface and then select the desired NV-DDR or NV-DDR2 data interface.

Within any data interface, transitioning between timing modes is supported.

To change the data interface to NV-DDR or NV-DDR2, or to change any timing mode, the Set Features command is used with the Timing Mode feature. The Set Features command (EFh), Feature Address, and the four parameters are entered using the previously selected timing mode in the previously selected data interface. When issuing the Set Features command, the host shall drive the DQS signal high (if supported by the interface the Set Features command is issued) during the entirety of the command (including parameter entry). After the fourth parameter, P4, is entered until the tITC time has passed the host shall not issue any commands to the device. After issuing the Set Features command and prior to transitioning CE_n high, the host shall hold signals in an Idle cycle state and DQS shall be set to one. In addition, when utilizing the NV-DDR interface the CLK rate shall only be changed when CE_n is high.

A transition from NV-DDR3 or NV-LPDDR4 to the other interfaces (SDR, NV-DDR, or NV-DDR2) is not supported. If VccQ = 1.2V then only the NV-DDR3 or NV-LPDDR4 interface is supported. See 4.5.4 for the initialization flow when using VccQ = 1.2V.

To change the Timing Mode for NV-DDR3 or NV-LPDDR4, the host should transition CE_n high and change the interface speed to the desired timing mode. The new timing mode is active when the host pulls CE_n low. When changing the NV-DDR3 or NV-LPDDR4 timing mode, prior to transitioning CE_n high, the host shall hold signals in an Idle bus state and DQS shall be set to one.

Prior to issuing any new commands to the device, the host shall transition CE_n high. The new data interface or timing mode is active when the host pulls CE_n low.

4.5.1. SDR Transition from NV-DDR or NV-DDR2

To transition from NV-DDR or NV-DDR2 to the SDR data interface, the host shall use the Reset (FFh) command using SDR timing mode 0. A device in any timing mode is required to recognize a Reset (FFh) command issued in SDR timing mode 0. After the Reset is issued, the host shall not issue any commands to the device until after the tITC time has passed. Note that after the tITC time has passed, only status commands may be issued by the host until the Reset completes. After issuing the Reset (FFh) and prior to transitioning CE_n high, the host shall hold signals in an Idle cycle state and DQS shall be set to one.

After CE_n has been pulled high and then transitioned low again, the host should issue a Set Features to select the appropriate SDR timing mode.

4.5.2. NV-DDR2 Recommendations

Prior to selecting the NV-DDR2 data interface, it is recommended that settings for the NV-DDR2 data interface be configured. Specifically:

- Set Features should be used to configure the NV-DDR2 Configuration feature.
- If on-die termination is used with a more advanced topology, the appropriate ODT Configure commands should be issued.

These actions should be completed prior to selecting the NV-DDR2 data interface. If these settings are modified when the NV-DDR2 data interface is already selected, the host should take care to ensure appropriate settings are applied in a manner that avoids signal integrity issues.

4.5.3. NV-DDR3 Recommendations

Prior to enabling the intended timing mode for the NV-DDR3 data interface, it is recommended that settings for the NV-DDR3 data interface be configured in Timing Mode 0. Specifically:

- Set Features should be used to configure the NV-DDR3 Configuration feature.
- If on-die termination is used with a more advanced topology, the appropriate ODT Configure commands should be issued.

These actions should be completed prior to enabling a NV-DDR3 Timing Mode other than Timing Mode 0.

4.5.4. NV-DDR3/NV-LPDDR4 Initialization

When VccQ = 1.2V the interface can operate in NV-DDR3 or NV-LPDDR4 mode. The host shall follow the initialization flow shown in Figure 4-5 to select between and configure NV-DDR3 or NV-LPDDR4.

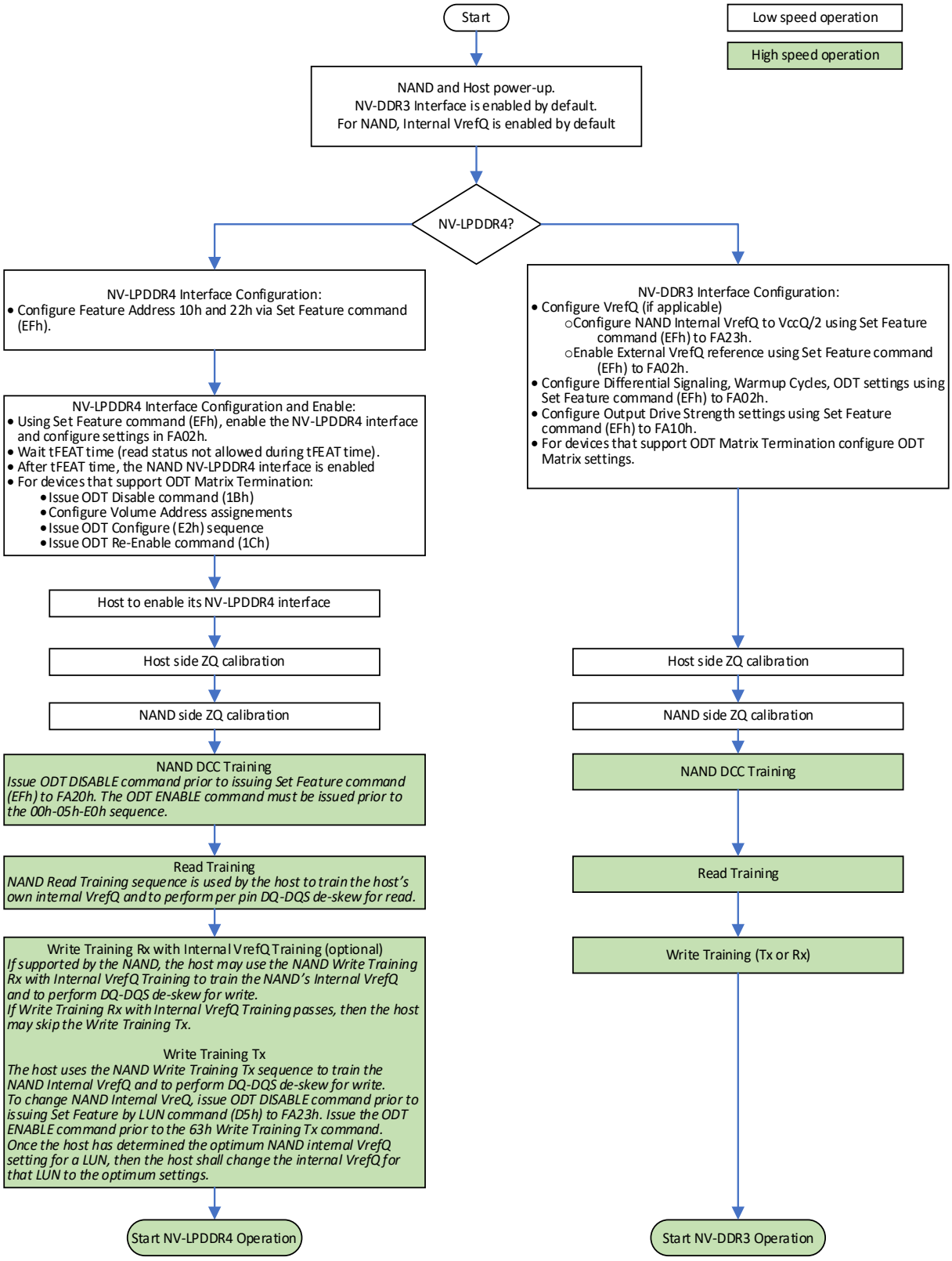

Start
Low speed operation
High speed operation
NAND and Host power-up.
NV-DDR3 Interface is enabled by default.
For NAND, Internal VrefQ is enabled by default
NV-LPDDR4?
NV-LPDDR4 Interface Configuration:
• Configure Feature Address 10h and 22h via Set Feature command (EFh).
NV-LPDDR4 Interface Configuration and Enable:
• Using Set Feature command (EFh), enable the NV-LPDDR4 interface and configure settings in FA02h.
• Wait tFEAT time (read status not allowed during tFEAT time).
• After tFEAT time, the NAND NV-LPDDR4 interface is enabled
• For devices that support ODT Matrix Termination:
• Issue ODT Disable command (1Bh)
• Configure Volume Address assignements
• Issue ODT Configure (E2h) sequence
• Issue ODT Re-Enable command (1Ch)
Host to enable its NV-LPDDR4 interface
Host side ZQ calibration
NAND side ZQ calibration
NAND DCC Training
Issue ODT DISABLE command prior to issuing Set Feature command (EFh) to FA20h. The ODT ENABLE command must be issued prior to the 00h-05h-E0h sequence.
Read Training
NAND Read Training sequence is used by the host to train the host's own internal VrefQ and to perform per pin DQ-DQS de-skew for read.
Write Training Rx with Internal VrefQ Training (optional)
If supported by the NAND, the host may use the NAND Write Training Rx with Internal VrefQ Training to train the NAND's Internal VrefQ and to perform DQ-DQS de-skew for write.
If Write Training Rx with Internal VrefQ Training passes, then the host may skip the Write Training Tx.
Write Training Tx
The host uses the NAND Write Training Tx sequence to train the NAND Internal VrefQ and to perform DQ-DQS de-skew for write.
To change NAND Internal VreQ, issue ODT DISABLE command prior to issuing Set Feature by LUN command (D5h) to FA23h. Issue the ODT ENABLE command prior to the 63h Write Training Tx command.
Once the host has determined the optimum NAND internal VrefQ setting for a LUN, then the host shall change the internal VrefQ for that LUN to the optimum settings.
Start NV-LPDDR4 Operation
NV-DDR3 Interface Configuration:
• Configure VrefQ (if applicable)
○Configure NAND Internal VrefQ to VccQ/2 using Set Feature command (EFh) to FA23h.
○Enable External VrefQ reference using Set Feature command (EFh) to FA02h.
• Configure Differential Signaling, Warmup Cycles, ODT settings using Set Feature command (EFh) to FA02h.
• Configure Output Drive Strength settings using Set Feature command (EFh) to FA10h.
• For devices that support ODT Matrix Termination configure ODT Matrix settings.
Host side ZQ calibration
NAND side ZQ calibration
NAND DCC Training
Read Training
Write Training (Tx or Rx)
Start NV-DDR3 Operation

Figure 4-5 NV-DDR3/NV-LPDDR4 Initialization Flow

4.6. Data Bus Inversion

4.6.1. DBI Purpose and Function

Data Bus Inversion (DBI) is an optional function for NAND device to reduce power consumption and power/bus noise during data input/output. A device supporting DBI shall have DBI pin to designate if the DQ signals are inverted by transmitter side or not. The DBI shall be synchronized with DQ signals. DBI is regarded as DQ, such that specifications such as AC parameters and Interface training shall be applied to DBI.

4.6.1. DBI Signal Encoding

DBI signal shall be either 0 or 1 during data input/output, where 0 indicates the DQ signals in the same cycle are not inverted and 1 indicates the DQ signals in the same cycle are inverted.
In the case where transmitter (host or NAND device) outputs DQ with DBI, the transmitter shall invert DQ signal on the pin and set DBI to 1 if the number of 1's of internal DQ signals is more than 4. Otherwise, if the number of 1's is equal to or less than 4, the transmitter shall not invert DQ signal on the pin and set DBI to 0.
DBI function shall be activated/deactivated by Set Feature.

The Table 4-7 below shows the DQ bus and DBI signal behavior during different modes of operation.

Mode of Operation	DQ[7:0] Behavior	DBI signal Behavior
Command/address	Without DBI encoding	"0"
Data Input	With DBI encoding	Encoding flag
Data Output	With DBI encoding	Encoding flag
SET Feature / GET Feature / Read ID / Read Status	Without DBI encoding	"0"
Write DQ Training (Tx side)	Without DBI encoding	9th DQ
Read DQ Training	Without DBI encoding	9th DQ (inverse mask value "0")

Table 4-7 DQ bus and DBI signal behavior

4.7. Test Conditions

4.7.1. SDR Only

The testing conditions that shall be used to verify that a device complies with a particular SDR timing mode are listed in Table 4-8 for devices that support the asynchronous data interface only and do not support driver strength settings.

Parameter	Value
Input pulse levels	0.0 V to VccQ
Input rise and fall times	5 ns
Input and output timing levels	VccQ / 2
Output load for VccQ of 3.3V	CL = 50 pF
Output load for VccQ of 1.8V	CL = 30 pF

Table 4-8 Testing Conditions for SDR Only Devices

4.7.2. Devices that Support Driver Strength Settings

The testing conditions that shall be used to verify compliance with a particular timing mode for devices that support driver strength settings are listed in Table 4-9. This includes all devices that support the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interfaces. It also includes devices that only support the SDR data interface that support driver strength settings. The test conditions are the same regardless of the number of LUNs per Target.

Parameter	NV-DDR	NV-DDR2/3, single-ended	NV-DDR2/3, differential	NV-LPDDR4
Positive input transition	VIL (DC) to VIH (AC)	VIL (DC) to VIH (AC)	VILdiff (DC) max to VIHdiff (AC) min	VIL.LTT (DC) to VIH.LTT (AC)
Negative input transition	VIH (DC) to VIL (AC)	VIH (DC) to VIL (AC)	VIHdiff (DC) min to VILdiff (AC) max	VIH.LTT (DC) to VIL.LTT (AC)
Minimum input slew rate	tIS = 1.0 V/ns	tIS = 1.0 V/ns	tIS = 2.0 V/ns	1.0 V/ns (for single-ended signals), 2.0 V/ns (for differential signals)
Input timing levels	VccQ / 2	VccQ / 2 if internal VREFQ or external VREFQ	crosspoint	crosspoint
Output timing levels	VccQ / 2	Vtt	crosspoint	crosspoint
Driver strength	Default[1]	Default[1]	Default[1]	Default[2]
Output reference load	50 Ohms to Vtt	50 Ohms to Vtt	50 Ohms to Vtt	50 Ohms to Vss

NOTE:
1. Default value for NV-DDR, NV-DDR2, and NV-DDR3 is 35 Ohms or 37.5 Ohms.
2. Default value for NV-LPDDR4 is 37.5 Ohms for the pull-down, and 50 Ohms Channel ODT setting for the pull-up

Table 4-9 Testing Conditions for Devices that Support Driver Strength Settings

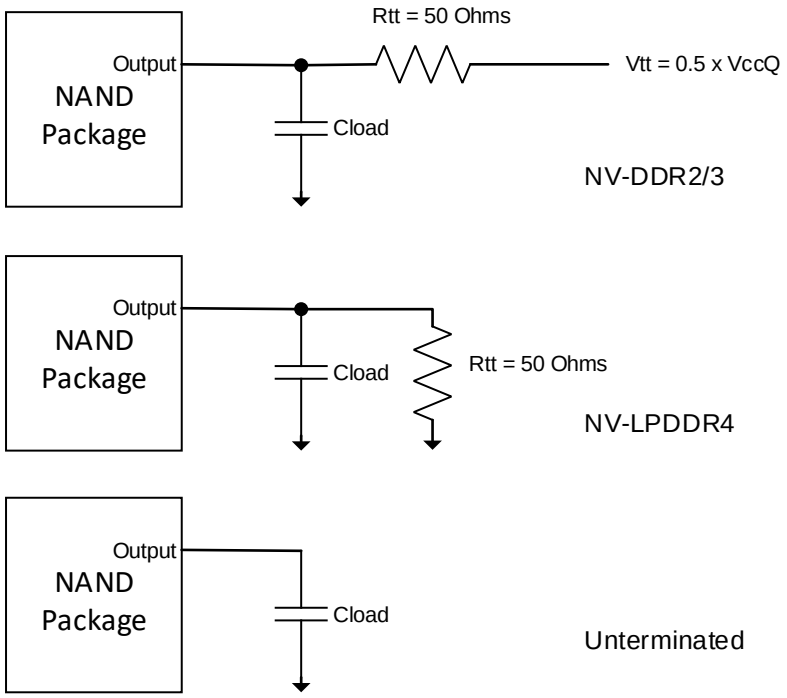


Figure 4-6 Driver Output Reference Load

See Table 4-23 Testing Conditions for Output Slew Rate for the reference capacitance load value (Cload).

4.8. ZQ Calibration

ZQ calibration is optional for the NV-DDR2 interface. ZQ calibration is optional but recommended for the NV-DDR3 interface over 400MT/s speed. ZQ calibration is required for the NV-LPDDR4 interface regardless of data rate.

ZQ Calibration is performed by issuing F9h command for ZQCL (ZQ long calibration) and D9h command for ZQCS (ZQ short calibration). ZQ Calibration is used to calibrate NAND Ron values and may also be used to calibrate ODT values as well. A longer time is required to calibrate the output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL is used to perform the initial calibration after power-up initialization sequence. The command to enable ZQCL may be issued at any time by the controller depending on the system environment. ZQCL triggers the calibration engine inside the NAND and once calibration is achieved, the calibrated values are transferred from the calibration engine to NAND IO, which updates the output driver and on-die termination values.

ZQCL is allowed a timing period of tZQCL to perform the full calibration and the transfer of values.

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as

defined by timing parameter tZQCS. One ZQCS command can effectively correct a minimum of 1.5 % (ZQ Correction) of R_{ON} and Rtt impedance error within tZQCS for all speed bins assuming the maximum sensitivities specified in Table 4-40 and Table 4-58. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the NAND is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$ZQCorrection / [(TSens\ X\ Tdriftrate) + (VSens\ X\ Vdriftrate)]$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the NAND temperature and voltage sensitivities.

For example, if TSens = 0.5% / oC, VSens = 0.2% / mV, Tdriftrate = 1 oC / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$1.5/ [(0.5\ X\ 1) + (0.2\ X\ 15)] = 0.429 = 429ms$$

No other activities, including read status, should be performed on the NAND channel (i.e. data bus) by the controller for the duration of tZQCL or tZQCS. The quiet time on the NAND channel allows accurate calibration of output driver and on-die termination values. For multi-channel packages, all channels should not have any data transfer during ZQ calibration even if the devices are not sharing a channel with the LUN performing ZQ calibration. Once NAND calibration is achieved, the NAND should disable ZQ current consumption path to reduce power. NAND array operations may not occur on the device performing the ZQCS or ZQCL operation. NAND array operations may occur on any devices that share the ZQ resistor with the device performing ZQCS or ZQCL. All devices connected to the DQ bus shall be in high impedance during the calibration procedure. The R/B# signal will be brought low by the device during calibration time, but if other devices are driving a shared R/B# low then the host is required to wait the maximum tWB+tZQCS before issuing any commands to the data bus (see Figure 5-43).

If a RESET command is issued during ZQ calibration, the state of the NAND device output driver strength and ODT is not guaranteed and the host shall re-run calibration operation. If a RESET command (FFh, FAh, FCh) is issued during ZQ long calibration (ZQCL) operation, the RESET operation is executed and the NAND device will revert to factory settings for output driver strength and ODT values (e.g. as if no ZQ calibration was performed). If a RESET command (FFh, FAh, FCh) is issued during ZQ short calibration (ZQCS) operation, the RESET operation is executed and the NAND device will return to vendor specific settings for output driver strength and ODT values. When either ZQCL or ZQCS is aborted with a RESET command, the reset time will be less than 10us (i.e. tRST < 10us).
In systems that share the ZQ resistor between NAND devices, the controller must not allow any overlap of tZQCL or tZQCS between the devices.

4.8.1. ZQ External Resistor Value, Tolerance, and Capacitive loading

In order to use the ZQ Calibration function, a RZQ = 300 Ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. The ZQ resistance is the sum of the trace resistance and the actual resistor resistance. The user should attempt to place ZQ resistor as close as possible to the NAND device to reduce the trace resistance. The resistance presented to the NAND needs to be +/-1% of 300 Ohm. The vendor may require a limit to the number of LUNs (and channels) a single RZQ resistor can be shared amongst. A single resistor can be used for each NAND device or one resistor can be shared between up to the vendor specified number of NAND devices if the ZQ calibration timings for each NAND do not overlap. The Cdie component of the ZQ signal will be less than an I/O signal. Depending on the number of die per package the total capacitance (Cpackage + Cdie) of the ZQ signal may exceed an I/O signal. For packages

with eight or more die that share a ZQ signal the total ZQ capacitance will not exceed 15% greater than the number of die times the Cdie of an I/O signal [i.e. Total ZQ capacitance < 1.15 * Cdie(I/O)].

The NV-DDR3 driver supports different Ron values. These Ron values are Ron = 25 (optional), 35 Ohms and/or 37.5 Ohms, and 50 Ohms.

Output driver impedance R_{ON} is defined by the value of the external reference resistor RZQ as follows:

$R_{ON}35$ = RZQ / 8.5 (nominal 35 Ohms ±15% with nominal RZQ = 300 Ohms)

4.9. I/O Drive Strength

The requirements in this section apply to devices that support driver strength settings.

The device may be configured with multiple driver strengths with the Set Features command. There is a 50 Ohm, 37.5 Ohm and/or 35 Ohm, 25 Ohm, and 18 Ohm setting that the device may support. The device support for the 18 Ohm, 25 Ohm, 35 Ohm and/or 37.5 Ohm settings are specified in the Parameter Page. The NV-DDR3 interface does not support the Ron = 18 Ohm value while support for Ron=25 Ohm is optional. A device that only supports the SDR data interface may support all or a subset of driver strength settings. Devices that support driver strength settings shall comply with the output driver requirements in this section.

Setting	Driver Strength	VccQ
18 Ohms	2.0x = 18 Ohms	3.3V / 1.8V without ZQ
25 Ohms	1.4x = 25 Ohms	
35 Ohms	1.0x = 35 Ohms	
50 Ohms	0.7x = 50 Ohms	
25 Ohms	RZQ/12	1.8V / 1.2V with ZQ
35 Ohms[2]	RZQ/8.5	
37.5 Ohms[1]	RZQ/8	
50 Ohms	RZQ/6	
NOTE: 1. Recommend default.		

Table 4-10 I/O Drive Strength Settings for NV-DDR, NV-DDR2, NV-DDR3

Setting	Unit
25 Ohms	RZQ/12
37.5 Ohms[1,3]	RZQ/8
42.9 Ohms	RZQ/7
50 Ohms[1,3]	RZQ/6
60 Ohms	RZQ/5
75 Ohms	RZQ/4
100 Ohms	RZQ/3
150 Ohms	RZQ/2

NOTE:
1. 37.5Ω and 50Ω Pull-Down drive strength are mandatory while the rest are vendor specific.
2. With ZQ Calibration, Pull-Down tolerance from the nominal value is ±15% (when measured at a pad voltage of VOH_nom)
3. The default value when LTT Pull-Down bit locations are in Location1 (see Feature Address 22h) is 50Ω while the default value when LTT Pull-Down bit locations are in Location2 (see Feature Address 10h) is 37.5Ω.
4. Since the default output pull-down drive strength values may be different among NAND vendors, the NAND LTT pull-down shall be configured by the host to the desired value prior to enabling the LTT interface.

Table 4-11 I/O Pull-Down Drive Strength Settings for NV-LPDDR4

Channel ODT Setting	Unit	VOH.LTT Nominal = VCCQ/3	VOH.LTT Nominal = VCCQ/2.5
25 Ohms	RZQ/12	Valid	Valid
37.5 Ohms	RZQ/8	Valid	Valid
42.9 Ohms	RZQ/7	Valid	Valid
50 Ohms[1]	RZQ/6	Valid (default)	Valid
60 Ohms	RZQ/5	Valid	Valid
75 Ohms	RZQ/4	Valid	Valid
100 Ohms	RZQ/3	Valid	Valid
150 Ohms	RZQ/2	Valid	Valid

NOTE:
1. Support for Pull-Up Setting with a Channel ODT value of 50Ω when VOHpu,nom = VccQ/3 is mandatory and shall be the default setting. Support for other values is vendor specific.

Table 4-12 Allowable I/O Pull-Up Settings (CH_ODT) for NV-LPDDR4

The pull-up and pull-down impedance mismatch requirements for the NV-DDR, NV-DDR2 and NV-DDR3 data interfaces are defined in Table 4-13. If ZQ calibration is enabled, the pull-up and pull-down impedance mismatch requirements for the NV-DDR2 and NV-DDR3 data interfaces is defined in Table 4-14. Impedance mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage. The testing conditions that shall be used to verify the impedance mismatch requirements are: VccQ = VccQ(min), VOUT = VccQ x 0.5, and T_A is across the full operating range.

I/O Drive Strength	NV-DDR Maximum	NV-DDR2/3 Maximum	Minimum	Unit
18 Ohms	6.3	3.2	0.0	Ohms
25 Ohms	8.8	4.4	0.0	Ohms
35 Ohms	12.3	6.2	0.0	Ohms
37.5 Ohms	13.3	6.64	0.0	Ohms
50 Ohms	17.5	8.8	0.0	Ohms

Table 4-13 NV-DDR, NV-DDR2 and NV-DDR3 Pull-up and Pull-down Impedance Mismatch without ZQ calibration

I/O Drive Strength	NV-DDR2/3 Maximum	Minimum	Unit
25 Ohms	3.75	0.0	Ohms
35 Ohms	5.25	0.0	Ohms
37.5 Ohms	5.62	0.0	Ohms
50 Ohms	7.5	0.0	Ohms

Table 4-14 NV-DDR2 and NV-DDR3 Pull-up and Pull-down Impedance Mismatch with ZQ calibration

4.10. Output Slew Rate

The requirements in this section apply to devices that support driver strength settings.

The output slew rate requirements that the device shall comply with are defined in Table 4-15, Table 4-16, and Table 4-17 for a single LUN per 8-bit data bus. The 18 Ohms, 25 Ohms, and 35 and/or 37.5 Ohms driver strengths output slew rate requirements are normative (if the associated driver strength is supported) and shall be supported by the device; the host may choose whether to use those settings based on topology. The testing conditions that shall be used to verify the output slew rate are listed in Table 4-23. NV-DDR3 output slew rates are only verified with ZQ calibration enabled.

Description	Output Slew Rate		Unit	Normative or Recommended
	Min	Max		
18 Ohms	1.5	10.0	V/ns	Normative
25 Ohms	1.5	9.0	V/ns	Normative
35 Ohms	1.2	7.0	V/ns	Normative
37.5 Ohms	1.2	7.0	V/ns	Normative
50 Ohms	1.0	5.5	V/ns	Recommended

Table 4-15 Output Slew Rate Requirements for 3.3V VccQ, NV-DDR only

Description	Output Slew Rate		Unit	Normative or Recommended
	Min	Max		
18 Ohms	1.0	5.5	V/ns	Normative
25 Ohms	0.85	5.0	V/ns	Normative
35 Ohms	0.75	4.0	V/ns	Normative
37.5 Ohms	0.73	4.0	V/ns	Normative
50 Ohms	0.60	4.0	V/ns	Recommended

Table 4-16 Output Slew Rate Requirements for 1.8V VccQ, NV-DDR or NV-DDR2 without ZQ calibration (single-ended)

Description	Output Slew Rate		Unit	Normative or Recommended
	Min	Max		
18 Ohms	2.0	11.0	V/ns	Normative
25 Ohms	1.7	10.0	V/ns	Normative
35 Ohms	1.5	8.0	V/ns	Normative
37.5 Ohms	1.45	8.0	V/ns	Normative
50 Ohms	1.2	8.0	V/ns	Recommended

Table 4-17 Output Slew Rate Requirements for 1.8V VccQ, NV-DDR2 without ZQ calibration (differential)

Description	Output Slew Rate		Unit	Normative or Recommended
	Min	Max		
25 Ohms	1.2	5.0	V/ns	Normative
35 Ohms	1.08	4.0	V/ns	Normative
37.5 Ohms	1.05	4.0	V/ns	Normative
50 Ohms	0.9	3.5	V/ns	Recommended

Table 4-18 Output Slew Rate Requirements for 1.8V VccQ, NV-DDR2 with ZQ calibration (single-ended)

Description	Output Slew Rate		Unit	Normative or Recommended
	Min	Max		
25 Ohms	2.4	10.0	V/ns	Normative
35 Ohms	2.16	8.0	V/ns	Normative
37.5 Ohms	2.1	8.0	V/ns	Normative
50 Ohms	1.8	7.0	V/ns	Recommended

Table 4-19 Output Slew Rate Requirements for 1.8V VccQ, NV-DDR2 (1.8V VccQ) with ZQ calibration (differential)

Description	Output Slew Rate		Unit	Normative or Recommended
	Min	Max		
25 Ohms	0.8	5.0	V/ns	Normative
35 Ohms	0.72	4.0	V/ns	Normative
37.5 Ohms	0.70	4.0	V/ns	Normative
50 Ohms	0.60	3.5	V/ns	Recommended

Table 4-20 Output Slew Rate Requirements for 1.2V VccQ, NV-DDR3 with ZQ calibration (single-ended)

Description	Output Slew Rate		Unit	Normative or Recommended
	Min	Max		
25 Ohms	1.6	10.0	V/ns	Normative
35 Ohms	1.44	8.0	V/ns	Normative
37.5 Ohms	1.4	8.0	V/ns	Normative
50 Ohms	1.2	7.0	V/ns	Recommended

Table 4-21 Output Slew Rate Requirements for 1.2V VccQ, NV-DDR3 with ZQ calibration (differential)

Description	Output Slew Rate		Unit
	Min	Max	
Single Ended	1	5.0	V/ns
Differential	2	10.0	V/ns

Table 4-22 Output Slew Rate Requirements for 1.2V VccQ, NV-LPDDR4 with ZQ calibration

The testing conditions used for output slew rate testing are specified in Table 4-23. Output slew rate is verified by design and characterization; it may not be subject to production test. The minimum slew rate is the minimum of the rising edge and the falling edge slew rate. The maximum slew rate is the maximum of the rising edge and the falling edge slew rate. Slew rates are measured under normal SSO conditions, with half of the DQ signals per data byte driving high and half of the DQ signals per data byte driving low. The output slew rate is measured per individual DQ signal. The differential parameters are used when the DQS signal is configured to operate as a differential signal. The NV-DDR2 data interface uses the same voltage levels defined in the SSTL_18 standard.

Parameter	NV-DDR	NV-DDR2/NV-DDR3	NV-LPDDR4
VOL(DC)	0.4 * VccQ	—	—
VOH(DC)	0.6 * VccQ	—	—
VOL(AC)	0.3 * VccQ	Vtt – (VccQ * 0.10)	0.2 * VOH.LTT nom
VOH(AC)	0.7 * VccQ	Vtt + (VccQ * 0.10)	0.8 * VOH.LTT nom
VOLdiff(AC)		-0.2 * VccQ	-0.6 * VOH.LTT nom
VOHdiff(AC)		0.2 * VccQ	0.6 * VOH.LTT nom
Positive output transition	VOL (DC) to VOH (AC)	VOL (AC) to VOH (AC) VOLdiff(AC) to VOHdiff(AC)	VOL (AC) to VOH (AC) VOLdiff(AC) to VOHdiff(AC)
Negative output transition	VOH (DC) to VOL (AC)	VOH (AC) to VOL (AC) VOHdiff(AC) to VOLdiff(AC)	VOH (AC) to VOL (AC) VOHdiff(AC) to VOLdiff(AC)
tRISE[1]	Time during rising edge from VOL(DC) to VOH(AC)	Time during rising edge from VOL(AC) to VOH(AC)	Time during rising edge from VOL(AC) to VOH(AC)
tFALL[1]	Time during falling edge from VOH(DC) to VOL(AC)	Time during falling edge from VOH(AC) to VOL(AC)	Time during falling edge from VOH(AC) to VOL(AC)
tRISEdiff[2]	—	Time during rising edge from VOLdiff(AC) to VOHdiff(AC)	Time during rising edge from VOLdiff(AC) to VOHdiff(AC)
tFALLdiff[2]	—	Time during falling edge from VOHdiff(AC) to VOLdiff(AC)	Time during falling edge from VOHdiff(AC) to VOLdiff(AC)
Output slew rate rising edge	[VOH(AC) – VOL(DC)] / tRISE	[VOH(AC) – VOL(AC)] / tRISE [VOHdiff(AC) – VOLdiff(AC)] / tRISEdiff	[VOH(AC) – VOL(AC)] / tRISE [VOHdiff(AC) – VOLdiff(AC)] / tRISEdiff
Output slew rate falling edge	[VOH(DC) – VOL(AC)] / tFALL	[VOH(AC) – VOL(AC)] / tFALL [VOHdiff(AC) – VOLdiff(AC)] / tFALLdiff	[VOH(AC) – VOL(AC)] / tFALL [VOHdiff(AC) – VOLdiff(AC)] / tFALLdiff
Output reference load Cload	5pF to Vss	NV-DDR2: 5pF to Vss NV-DDR3: see Note 3	2pF to Vss

NOTE:
1. Refer to Figure 4-7 and Figure 4-8.
2. Refer to Figure 4-9.
3. NV-DDR3: 5pF reference load for data rata rates up to 1600MT/s and 2pF for data rates >1600MT/s.

Table 4-23 Testing Conditions for Output Slew Rate

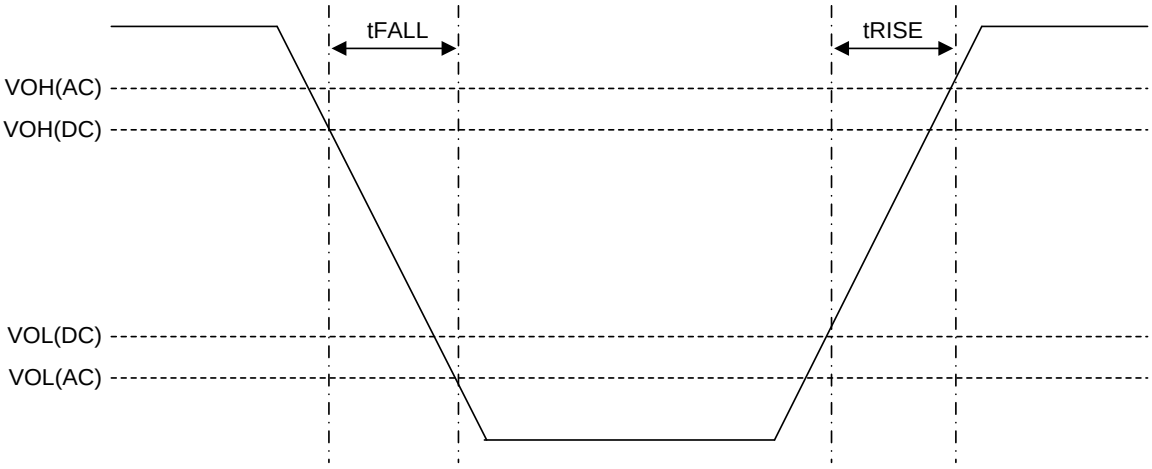


Figure 4-7 tRISE and tFALL Definition for Output Slew Rate, NV-DDR

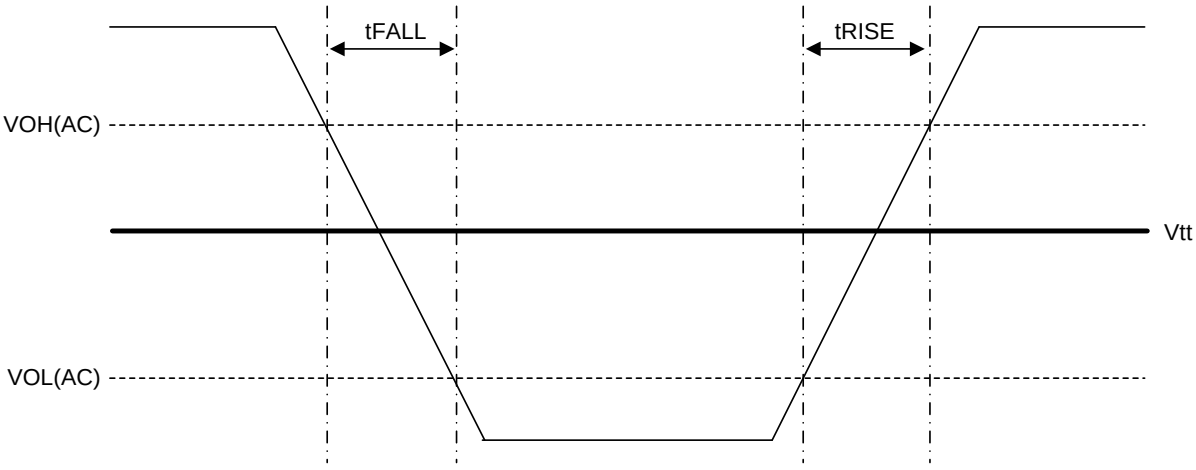


Figure 4-8 tRISE and tFALL Definition for Output Slew Rate, NV-DDR2/3, NV-LPDDR4 (single-ended)

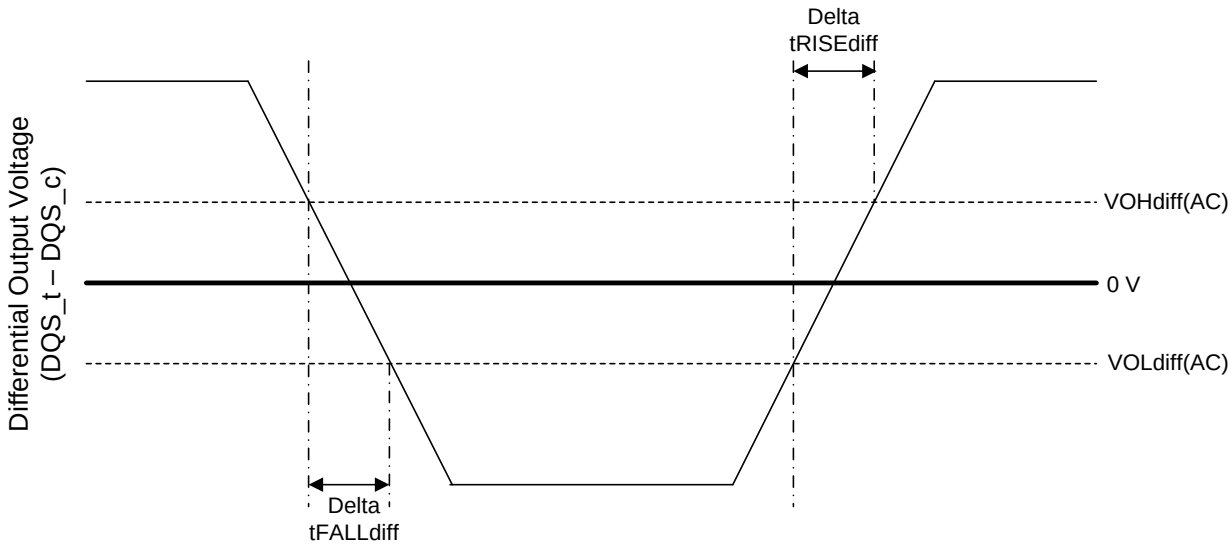


Figure 4-9 tRISEdiff and tFALLdiff Definition for Output Slew Rate, NV-DDR2/3, NV-LPDDR4 (differential)

The output slew rate matching ratio is specified in Table 4-24. The output slew rate mismatch is determined by the ratio of fast slew rate and slow slew rate. If the rising edge is faster than the falling edge, then divide the rising slew rate by the falling slew rate. If the falling is faster than the rising edge, then divide the falling slew rate by the rising slew rate. The output slew rate mismatch is verified by design and characterization; it may not be subject to production test

Parameter	Min	Max
Output Slew Rate Matching Ratio, without ZQ calibration	1.0	1.4
Output Slew Rate Matching Ratio, with ZQ calibration	1.0	1.3

Table 4-24 Output Slew Rate Matching Ratio

4.11. Capacitance

4.11.1. Legacy Capacitance Requirements

The requirements in this section apply to legacy devices that support the NV-DDR or NV-DDR2 data interfaces. For NV-DDR3 devices and NV-DDR2 devices that support speeds faster than 533 MT/s, the Package Electrical Specification and Pad Capacitance (section 4.11.3) shall be used for device capacitance requirements.

The input capacitance requirements are defined in Table 4-25. The testing conditions that shall be used to verify the input capacitance requirements are: temperature of 25 degrees Celsius, VccQ=1.2V, V_{BIAS} = VccQ/2, and a frequency of 100 MHz.

The capacitance delta values measure the pin-to-pin capacitance for all LUNs within a package, including across data buses if the package has the same number of LUNs per x8 data bus (i.e. package channel). The capacitance delta values are not measured across data buses if the

package has a different number of LUNs per x8 data bus. The capacitance delta values change based on the number of LUNs per x8 data bus.

The variance from the Typical capacitance is the maximum capacitance or minimum capacitance any pin in a signal group may have relative to the Typical value for that signal group. The variance is symmetrically offset from the Typical reported value and bounds the absolute maximum and minimum capacitance values.

All NAND Targets that share an I/O should report an equivalent Typical capacitance in order to meet the capacitance delta requirements. If NAND Targets with different Typical capacitance values share an I/O bus, then the values in these tables are not applicable and detailed topology and signal integrity analysis needs to be completed by the implementer to determine the bus speed that is achievable.

Parameter	Number of LUNs per x8 Data Bus				Unit
	1	2	4	8	
Variance from Typical	± 1.0	± 1.5	± 2.0	± 4.0	pF
Delta	1.4	1.7	2.0	4.0	pF

NOTE:
1. Typical capacitance values for pin groups CCK, CIN, and CIO are vendor specific, see the vendor component datasheet. The allowable range for Typical capacitance values is specified in Table 4-26 for CLK and input pins and Table 4-27 for I/O pins.
2. Input capacitance for CE_n and WP_n shall not exceed the higher of either the CLK or input pin maximums. However, CE_n and WP_n are not required to meet delta or variance requirements. For example, if maximum capacitance (typical capacitance plus variance from typical) for CLK is 5.0pf and maximum capacitance for the input pins is 5.5pf, the maximum capacitance for CE_n and WP_n is 5.5pf.

Table 4-25 Input Capacitance Delta and Variance

The Typical capacitance values for the NV-DDR and NV-DDR2 data interfaces shall be constrained to the ranges defined in Table 4-26 input pins and Table 4-27 for I/O pins for devices in a BGA package. The Typical capacitance value for the CLK signal when using the NV-DDR data interface shall also be constrained to the ranges defined in Table 4-26. Capacitance is shared for LUNs that share the same 8-bit data bus in the same package, thus the ranges are specific to the number of LUNs per data bus.

Parameter	Min	Typ Low	Typ High	Max	Unit
1 LUN per x8 data bus	1.5	2.5	5.4	6.4	pF
2 LUNs per x8 data bus	2.0	3.5	7.7	9.2	pF
4 LUNs per x8 data bus	3.5	5.5	12.3	14.3	pF
8 LUNs per x8 data bus	4.5	8.5	23.3	27.3	pF

Table 4-26 Input Capacitance Typical Ranges for Input Pins

Parameter	Min	Typ Low	Typ High	Max	Unit
1 LUN per x8 data bus	3.0	4.0	5.7	6.7	pF
2 LUNs per x8 data bus	5.0	6.5	8.5	10.0	pF
4 LUNs per x8 data bus	8.9	10.9	14.9	16.9	pF
8 LUNs per x8 data bus	16.7	20.7	28.7	32.7	pF

Table 4-27 Input Capacitance Typical Ranges for I/O pins

NOTE: Capacitance ranges are not defined for the TSOP package due to the varying TSOP package construction techniques and bond pad locations. For the TSOP package compared to the BGA package, the input capacitance delta values do not apply, input capacitance values for I/O pins is similar, and input capacitance values for input pins could be significantly higher. For higher speed applications, the BGA-63, BGA-100, and BGA-152 packages are recommended due to their lower and more consistent input capacitance and input capacitance delta values.

4.11.2. Capacitance Requirements (Informative)

Capacitance requirements depend on the signal type. Capacitance requirements are different for input only pins than I/O pins. Additionally, there are separate capacitance requirements for CLK (NV-DDR only), CE_n, and WP_n. The four signal groups that capacitance requirements are separately defined for are:

CLK: CLK (NV-DDR only)
Inputs: ALE, CLE, WE_n
I/Os: DQ[7:0] (I/O[7:0] or I/O[15:0]), DQS (DQS_t / DQS_c)
Other: CE_n, WP_n

The capacitance requirements for RE_n (RE_t/RE_c) and W/R_n are dependent on whether ODT is supported, as indicated in the parameter page. If ODT is supported, then RE_n (RE_t/RE_c) and W/R_n are treated as I/Os for capacitance. If ODT is not supported, then RE_n (RE_t/RE_c) and W/R_n are treated as inputs for capacitance, but RE_n (RE_t/RE_c) should be excluded from I/O Delta Capacitance Spec.

For each signal group, a typical capacitance value is defined and reported for each NAND Target within a package. The signal groups include all signal group pins in a single package even if the pins belong to separate I/O channels unless the package has a different number of LUNs per x8 data bus. If the package has a different number of LUNs per x8 data bus than the signal group pins are separated per each x8 data bus.

There are two key parameters that define how much capacitance may vary within a package. The *delta* defines the maximum pin-to-pin capacitance difference within a signal group in a single package. Specifically, the delta within a signal group is the difference between the pin with the maximum capacitance and the pin with the minimum capacitance within the signal group. The *variance* is the maximum capacitance or minimum capacitance any pin in a signal group may have relative to the typical value for that signal group. The variance is symmetrically offset from the typical reported value and bounds the absolute maximum and minimum capacitance values. The delta may be asymmetrical from the typical value; i.e. the minimum capacitance may be closer or further away from the typical value than the maximum capacitance for that signal group.

The “delta window” always falls within the “variance window”, and thus the delta is always smaller than the variance multiplied by two.

As shown in Figure 4-10, the delta window falls within the variance window. Two example delta windows are shown. The “delta low window” shows an example where the minimum capacitance value is lower compared to the typical capacitance value; the “delta high window” shows the opposite example where the maximum capacitance value is higher compared to the typical capacitance value. The delta window for a given package may fall anywhere within the variance window for the given number of LUNs per x8 data bus.

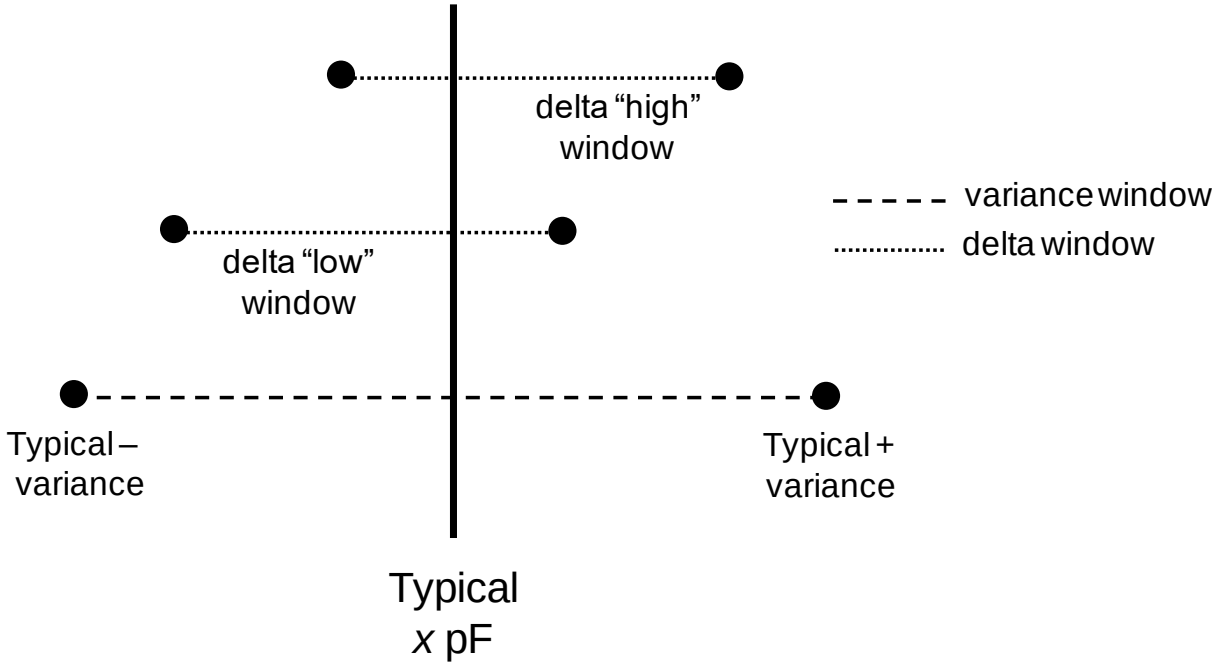


Figure 4-10 Typical, Variance, and Delta Capacitance Values

As a more concrete example, take the case of a package with two LUNs per x8 data bus. The typical capacitance for the I/O signal group may be between 6.5 pF and 8.5 pF. For this example, the typical capacitance is 8.5 pF. The variance for two LUNs per x8 data bus is 1.5 pF. Thus, all signal pins in the I/O group shall have a capacitance between 7.0 pF and 10.0 pF. The delta for two LUNs per x8 data bus is 1.7 pF. If the minimum pin capacitance for all pins in the I/O signal group on this package is 7.0 pF, then the maximum pin capacitance for all pins in the I/O signal group on this package shall be no greater than 8.7 pF. If the minimum pin capacitance for all pins in the I/O signal group on this package is 8.0 pF, then the maximum pin capacitance for all pins in the I/O signal group on this package shall be no greater than 9.7 pF.

4.11.3. Package Electrical Specifications and Pad Capacitance for Raw NAND Devices Supporting I/O Speeds Greater than 533MT/s

The requirements in this section apply to devices that support the NV-DDR3 and NV-LPDDR4 data interface and are optional for the SDR and NV-DDR interfaces. The requirements in this section are optional for the NV-DDR2 interface when the device supports I/O speeds 533 MT/s or less and required for NV-DDR2 interface when the device supports I/O speeds greater than 533 MT/s. The Parameter Page will specify if the device supports the requirements in this section (see 5.7.1.3, Parameter Page Byte 6-7, bit 15),

For NAND devices which support I/O speeds greater than 533MT/s, the DQ[7:0], DQS_t, DQS_c, RE_t, RE_c, DBI, ALE, CLE, CE_n, WE_n, WP_n, ZQ pins shall meet the requirements detailed in this section and not the Legacy Capacitance Requirements in sections 4.11.1 and 4.11.2.

See vendor datasheet for capacitance values for other pins not specified in this section.

4.11.3.1. Package Electrical Specifications for DQS_t, DQS_c, DQ[7:0], RE_t, RE_c, DBI

ZIO applies to DQ[7:0], DQS_t, DQS_c, RE_t, RE_c and DBI. TdIO RE applies to RE_t and RE_c. TdIO and TdIOMismatch applies to DQ[7:0], DQS_t, DQS_c and DBI. Mismatch and Delta values are required to be met across same data bus on given package (i.e. package channel), but not required across all channels on a given package.

Symbol	Parameter	≤400 MT/s		533 MT/s		667 MT/s		800-1200 MT/s		1333-3600 MT/s		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Z_{IO}	Input/Output Zpkg	35	90	35	90	35	90	35	90	35	90	Ohms
Td_{IO}	Input/Output Pkg Delay	-	160	-	160	-	145	-	130	-	130	ps
$Td_{IO\ RE}$	Input/Output Pkg Delay	-	160	-	160	-	145	-	130	-	130	ps
Td_{IO}Mismatch	Input/Output Pkg Delay Mismatch	-	50	-	40	-	40	-	40	-	40	ps
D $Z_{IO\ DQS}$	Delta Zpkg for DQS_t and DQS_c	-	10	-	10	-	10	-	10	-	10	Ohms
D $Td_{IO\ DQS}$	Delta Pkg Delay for DQS_t and DQS_c	-	10	-	10	-	10	-	10	-	10	ps
D $Z_{IO\ RE}$	Delta Zpkg for RE_t and RE_c	-	10	-	10	-	10	-	10	-	10	Ohms
D $Td_{IO\ RE}$	Delta Pkg Delay for RE_t and RE_c	-	10	-	10	-	10	-	10	-	10	ps

NOTE:
1. The package parasitic (L & C) are validated using package only samples. The capacitance is measured with Vcc, VccQ, Vss, VssQ shorted with all other signal pins floating. The inductance is measured with Vcc, VccQ, Vss and VssQ shorted and all other signal pins shorted at the die side (not pin).
2. Package only impedance (Z_{IO}) is calculated based on the Lpkg and Cpkg total for a given pin where: Z_{IO}(total per pin) = SQRT(Lpkg/Cpkg)
3. Package only delay (Td_{IO}) is calculated based on Lpkg and Cpkg total for a given pin where: Td_{IO}(total per pin) = SQRT(Lpkg*Cpkg)
4. Mismatch for Td_{IO} (Td_{IO}Mismatch) is value of Pkg Delay of fastest I/O minus the value of Pkg Delay for slowest I/O.
5. Delta for DQS is Absolute value of ZIO(DQS_t-ZIO(DQS_c) for impedance(Z) or absolute value of TdIO (DQS_t)-TdIO(DQS_c) for delay(Td)
6. Delta for RE is Absolute value of ZIO(RE_t-ZIO(RE_c) for impedance(Z) or absolute value of TdIO(RE_t)-TdIO(RE_c) for delay(Td)

Table 4-28 Package Electrical Specifications

4.11.3.2. Pad Capacitance Specifications for DQS_t, DQS_c, DQ[7:0], RE_t, RE_c, DBI and ZQ Pins

Symbol	Parameter	≤400 MT/s		533 – 800 MT/s		800 – 1600 MT/s		> 1600 – 3600 MT/s		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
C_{IO}	Input/Output Capacitance for DQ[7:0], DQS_t, DQS_c, RE_t, RE_c, DBI	-	2.5	-	2.5	-	2.5	-	1.6	pF
C_{ZQ}	ZQ capacitance	-	2.875	-	2.875	-	2.875	-	2	pF
D $C_{IO\ DQS}$	Delta Input/Output Capacitance DQS_t and DQS_c	0	0.2	0	0.2	0	0.2	0	0.2	pF
D $C_{IO\ RE}$	Delta Input/Output Capacitance for RE_t and RE_c	0	0.2	0	0.2	0	0.2	0	0.2	pF

NOTE:
1. These parameters are not subject to a production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with Vcc, VccQ, Vss, and VssQ applied and all other pins floating (accept the pin under test). VccQ = 1.2V, VBIAS = VccQ/2 and on-die termination off.
2. These parameters apply to monolithic die, obtained by de-embedding the package L & C parasitics.
3. Delta for DQS is the absolute value of CIO(DQS_t) - CIO(DQS_c)
4. Delta for RE is the absolute value of CIO(RE_t) - CIO(RE_c)

Table 4-29 Pad Input/Output Capacitance for DQS_t, DQS_c, DQ[7:0], RE_t, RE_c, DBI and ZQ Pins

4.11.3.3. Input Capacitance Specifications for ALE, CE_n, CLE, WE_n and WP_n Pin

The input capacitance requirements defined in Table 49.2 below are for packaged raw NAND devices. The testing conditions that shall be used to verify the input capacitance requirements are: temperature of 25 degrees Celsius, VccQ = nominal value, Vcc = nominal value, V_{IN} = 0v, and a frequency of 100 MHz. The DC_{IN} specification is for the ALE, CLE and WE_n pins only and is the maximum variation allowed for those pins as a group.

Parameter	Loading	Min	Typ	Max	Unit
C_{IN}	1 LUN per x8 data bus	-	-	6.4	pF
	2 LUNs per x8 data bus	-	-	9.2	pF
	4 LUNs per x8 data bus	-	-	14.3	pF
	8 LUNs per x8 data bus	-	-	27.3	pF
DC_{IN} [1]	1 LUN per x8 data bus	-	-	1.4	pF
	2 LUNs per x8 data bus	-	-	1.7	pF
	4 LUNs per x8 data bus	-	-	2.0	pF
	8 LUNs per x8 data bus	-	-	4.0	pF

NOTE:
1. DC_{IN} applies to ALE, CLE and WE_n pins as a group (WE_n pin may be excluded from the group)

Table 4-30 Capacitance Specifications for ALE, CE_n, CLE, WE_n and WP_n Pins

4.11.4. Electrostatic Discharge Sensitivity Characteristics

The ESD specifications below apply to NAND devices that support >2400MT/s data rates.

Parameter[1]	Symbol	Min	Max	Unit	Notes
Human Body Model (HBM)	ESD_{HBM}	1000	-	V	2
Charged-device model (CDM)	ESD_{CDM}	250	-	V	3
Note:1 State-of-the-art basic ESD control measures have to be in place when handling devices Note:2 Refer to ESDA / JEDEC Joint Standard JS-001 for measurement procedures Note:3 Refer to ESDA / JEDEC Joint Standard JS-002 for measurement procedures					

Table 4-31 Electrostatic Discharge Sensitivity Characteristics

4.12. Impedance Values

The test conditions that shall be used to verify the impedance values is specified in Table 4-32.

Condition	Temperature (TA)	VccQ (3.3V)	VccQ (1.8V)	VccQ (1.2V)	Process
Minimum Impedance	TOPER (Min) degrees Celsius	3.6V	1.95V	1.26V	Fast-fast
Nominal Impedance	25 degrees Celsius	3.3V	1.8V	1.2V	Typical
Maximum impedance	TOPER (Max) degrees Celsius	2.7V	1.7V	1.14V	Slow-slow

Table 4-32 Testing Conditions for Impedance Values

4.12.1. NV-DDR

The impedance values corresponding to several different VOUT values are defined in Table 4-33 for 3.3V VccQ and Table 4-34 for 1.8V VccQ for the NV-DDR data interface.

R_{ON} = 18 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	28.7	16.2	7.0	Ohms
	0.5 x VccQ	36.0	18.0	9.0	Ohms
	0.8 x VccQ	50.0	21.0	11.8	Ohms
R_pullup	0.2 x VccQ	50.0	21.0	11.8	Ohms
	0.5 x VccQ	36.0	18.0	9.0	Ohms
	0.8 x VccQ	28.7	14.0	7.0	Ohms
R_{ON} = 25 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	40.0	22.3	9.3	Ohms
	0.5 x VccQ	50.0	25.0	12.6	Ohms
	0.8 x VccQ	68.0	29.0	16.3	Ohms
R_pullup	0.2 x VccQ	68.0	29.0	16.3	Ohms
	0.5 x VccQ	50.0	25.0	12.6	Ohms
	0.8 x VccQ	40.0	19.0	9.3	Ohms
R_{ON} = 35 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	58.0	32.0	12.8	Ohms
	0.5 x VccQ	70.0	35.0	18.0	Ohms
	0.8 x VccQ	95.0	40.0	23.0	Ohms
R_pullup	0.2 x VccQ	95.0	40.0	23.0	Ohms
	0.5 x VccQ	70.0	35.0	18.0	Ohms
	0.8 x VccQ	58.0	32.0	12.8	Ohms
R_{ON} = 50 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	80.0	45.0	18.4	Ohms
	0.5 x VccQ	100.0	50.0	25.0	Ohms
	0.8 x VccQ	136.0	57.0	32.0	Ohms
R_pullup	0.2 x VccQ	136.0	57.0	32.0	Ohms
	0.5 x VccQ	100.0	50.0	25.0	Ohms
	0.8 x VccQ	80.0	45.0	18.4	Ohms

Table 4-33 Impedance Values for 3.3V VccQ (NV-DDR)

R_{ON} = 18 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	34.0	13.5	7.5	Ohms
	0.5 x VccQ	31.0	18.0	9.0	Ohms
	0.8 x VccQ	44.0	23.5	11.0	Ohms
R_pullup	0.2 x VccQ	44.0	23.5	11.0	Ohms
	0.5 x VccQ	31.0	18.0	9.0	Ohms
	0.8 x VccQ	34.0	13.5	7.5	Ohms
R_{ON} = 25 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	47.0	19.0	10.5	Ohms
	0.5 x VccQ	44.0	25.0	13.0	Ohms
	0.8 x VccQ	61.5	32.5	16.0	Ohms
R_pullup	0.2 x VccQ	61.5	32.5	16.0	Ohms
	0.5 x VccQ	44.0	25.0	13.0	Ohms
	0.8 x VccQ	47.0	19.0	10.5	Ohms
R_{ON} = 35 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	66.5	27.0	15.0	Ohms
	0.5 x VccQ	62.5	35.0	18.0	Ohms
	0.8 x VccQ	88.0	52.0	22.0	Ohms
R_pullup	0.2 x VccQ	88.0	52.0	22.0	Ohms
	0.5 x VccQ	62.5	35.0	18.0	Ohms
	0.8 x VccQ	66.5	27.0	15.0	Ohms
R_{ON} = 37.5 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	70.5	29.0	16.0	Ohms
	0.5 x VccQ	66.0	37.5	19.5	Ohms
	0.8 x VccQ	92.0	55.0	24.0	Ohms
R_pullup	0.2 x VccQ	92.0	55.0	24.0	Ohms
	0.5 x VccQ	66.0	37.5	19.5	Ohms
	0.8 x VccQ	70.5	29.0	16.0	Ohms
R_{ON} = 50 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	95.0	39.0	21.5	Ohms
	0.5 x VccQ	90.0	50.0	26.0	Ohms
	0.8 x VccQ	126.5	66.5	31.5	Ohms
R_pullup	0.2 x VccQ	126.5	66.5	31.5	Ohms
	0.5 x VccQ	90.0	50.0	26.0	Ohms
	0.8 x VccQ	95.0	39.0	21.5	Ohms

Table 4-34 Impedance Values for 1.8V VccQ (NV-DDR)

4.12.2. NV-DDR2

The impedance values for 1.8V VccQ for the NV-DDR2 data interface are specified in Table 4-35 (without ZQ calibration) and Table 4-36 (with ZQ calibration).

R_{ON} = 18 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	31.5	18.0	8.2	Ohms
	0.5 x VccQ	31.5	18.0	10.8	Ohms
	0.8 x VccQ	42.7	18.0	10.8	Ohms
R_pullup	0.2 x VccQ	42.7	18.0	10.8	Ohms
	0.5 x VccQ	31.5	18.0	10.8	Ohms
	0.8 x VccQ	31.5	18.0	8.2	Ohms
R_{ON} = 25 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	44.0	25.0	11.4	Ohms
	0.5 x VccQ	44.0	25.0	15.0	Ohms
	0.8 x VccQ	61.0	25.0	15.0	Ohms
R_pullup	0.2 x VccQ	61.0	25.0	15.0	Ohms
	0.5 x VccQ	44.0	25.0	15.0	Ohms
	0.8 x VccQ	44.0	25.0	11.4	Ohms
R_{ON} = 35 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	61.0	35.0	16.0	Ohms
	0.5 x VccQ	61.0	35.0	21.0	Ohms
	0.8 x VccQ	85.3	35.0	21.0	Ohms
R_pullup	0.2 x VccQ	85.3	35.0	21.0	Ohms
	0.5 x VccQ	61.0	35.0	21.0	Ohms
	0.8 x VccQ	61.0	35.0	16.0	Ohms
R_{ON} = 37.5 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	66.0	37.5	17.1	Ohms
	0.5 x VccQ	66.0	37.5	22.5	Ohms
	0.8 x VccQ	91.5	37.5	22.5	Ohms
R_pullup	0.2 x VccQ	91.5	37.5	22.5	Ohms
	0.5 x VccQ	65.5	37.5	22.5	Ohms
	0.8 x VccQ	65.5	37.5	17.1	Ohms
R_{ON} = 50 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	87.0	50.0	24.0	Ohms
	0.5 x VccQ	87.0	50.0	30.0	Ohms
	0.8 x VccQ	122.0	50.0	30.0	Ohms
R_pullup	0.2 x VccQ	122.0	50.0	30.0	Ohms
	0.5 x VccQ	87.0	50.0	30.0	Ohms
	0.8 x VccQ	87.0	50.0	24.0	Ohms

Table 4-35 Impedance Values for 1.8V VccQ (NV-DDR2) without ZQ calibration

R_{ON} = 25 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	1.15	1	0.57	RZQ/12
	0.5 x VccQ	1.15	1	0.85	RZQ/12
	0.8 x VccQ	1.47	1	0.85	RZQ/12
R_pullup	0.2 x VccQ	1.47	1	0.85	RZQ/12
	0.5 x VccQ	1.15	1	0.85	RZQ/12
	0.8 x VccQ	1.15	1	0.57	RZQ/12
R_{ON} = 35 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	1.15	1	0.57	RZQ/8.5
	0.5 x VccQ	1.15	1	0.85	RZQ/8.5
	0.8 x VccQ	1.47	1	0.85	RZQ/8.5
R_pullup	0.2 x VccQ	1.47	1	0.85	RZQ/8.5
	0.5 x VccQ	1.15	1	0.85	RZQ/8.5
	0.8 x VccQ	1.15	1	0.57	RZQ/8.5
R_{ON} = 37.5 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	1.15	1	0.57	RZQ/8
	0.5 x VccQ	1.15	1	0.85	RZQ/8
	0.8 x VccQ	1.47	1	0.85	RZQ/8
R_pullup	0.2 x VccQ	1.47	1	0.85	RZQ/8
	0.5 x VccQ	1.15	1	0.85	RZQ/8
	0.8 x VccQ	1.15	1	0.57	RZQ/8
R_{ON} = 50 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	1.15	1	0.57	RZQ/6
	0.5 x VccQ	1.15	1	0.85	RZQ/6
	0.8 x VccQ	1.47	1	0.85	RZQ/6
R_pullup	0.2 x VccQ	1.47	1	0.85	RZQ/6
	0.5 x VccQ	1.15	1	0.85	RZQ/6
	0.8 x VccQ	1.15	1	0.57	RZQ/6

Notes:
1. Tolerance limits assume RZQ of 300Ω +/- 1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
2. Refer to Output Driver Sensitivity if either the temperature or the voltage changes after calibration.
3. The minimum values are derated by 6% when the device operates between –40°C and 0°C (TC).

Table 4-36 Impedance Values for 1.8V VccQ (NV-DDR2) with ZQ calibration

4.12.3. NV-DDR3

The impedance values for 1.2V VccQ for the NV-DDR3 data interface are specified in Table 4-37 (without ZQ calibration) and Table 4-38 (with ZQ calibration).

R_{ON} = 25 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	44.0	25.0	11.4	Ohms
	0.5 x VccQ	44.0	25.0	15.0	Ohms
	0.8 x VccQ	61.0	25.0	15.0	Ohms
R_pullup	0.2 x VccQ	61.0	25.0	15.0	Ohms
	0.5 x VccQ	44.0	25.0	15.0	Ohms
	0.8 x VccQ	44.0	25.0	11.4	Ohms
R_{ON} = 35 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	61.0	35.0	16.0	Ohms
	0.5 x VccQ	61.0	35.0	21.0	Ohms
	0.8 x VccQ	85.3	35.0	21.0	Ohms
R_pullup	0.2 x VccQ	85.3	35.0	21.0	Ohms
	0.5 x VccQ	61.0	35.0	21.0	Ohms
	0.8 x VccQ	61.0	35.0	16.0	Ohms
R_{ON} = 37.5 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	65.5	37.5	17.1	Ohms
	0.5 x VccQ	65.5	37.5	22.5	Ohms
	0.8 x VccQ	91.4	37.5	22.5	Ohms
R_pullup	0.2 x VccQ	91.4	37.5	22.5	Ohms
	0.5 x VccQ	65.5	37.5	22.5	Ohms
	0.8 x VccQ	65.5	37.5	17.1	Ohms
R_{ON} = 50 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	87.0	50.0	24.0	Ohms
	0.5 x VccQ	87.0	50.0	30.0	Ohms
	0.8 x VccQ	122.0	50.0	30.0	Ohms
R_pullup	0.2 x VccQ	122.0	50.0	30.0	Ohms
	0.5 x VccQ	87.0	50.0	30.0	Ohms
	0.8 x VccQ	87.0	50.0	24.0	Ohms

Table 4-37 Impedance Values for 1.2V VccQ (NV-DDR3) without ZQ calibration

R_{ON} = 25 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	1.15	1	0.57	RZQ/12
	0.5 x VccQ	1.15	1	0.85	RZQ/12
	0.8 x VccQ	1.47	1	0.85	RZQ/12
R_pullup	0.2 x VccQ	1.47	1	0.85	RZQ/12
	0.5 x VccQ	1.15	1	0.85	RZQ/12
	0.8 x VccQ	1.15	1	0.57	RZQ/12
R_{ON} = 35 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	1.15	1	0.57	RZQ/8.5
	0.5 x VccQ	1.15	1	0.85	RZQ/8.5
	0.8 x VccQ	1.47	1	0.85	RZQ/8.5
R_pullup	0.2 x VccQ	1.47	1	0.85	RZQ/8.5
	0.5 x VccQ	1.15	1	0.85	RZQ/8.5
	0.8 x VccQ	1.15	1	0.57	RZQ/8.5
R_{ON} = 37.5 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	1.15	1	0.57	RZQ/8
	0.5 x VccQ	1.15	1	0.85	RZQ/8
	0.8 x VccQ	1.47	1	0.85	RZQ/8
R_pullup	0.2 x VccQ	1.47	1	0.85	RZQ/8
	0.5 x VccQ	1.15	1	0.85	RZQ/8
	0.8 x VccQ	1.15	1	0.57	RZQ/8
R_{ON} = 50 Ohms					
Description	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	1.15	1	0.57	RZQ/6
	0.5 x VccQ	1.15	1	0.85	RZQ/6
	0.8 x VccQ	1.47	1	0.85	RZQ/6
R_pullup	0.2 x VccQ	1.47	1	0.85	RZQ/6
	0.5 x VccQ	1.15	1	0.85	RZQ/6
	0.8 x VccQ	1.15	1	0.57	RZQ/6

Notes:

1. Tolerance limits assume RZQ of 300Ω +/- 1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
2. Refer to Output Driver Sensitivity if either the temperature or the voltage changes after calibration.
3. The minimum values are derated by 6% when the device operates between –40°C and 0°C (TC).

Table 4-38 Impedance Values for 1.2V VccQ (NV-DDR3) with ZQ calibration

4.12.1. NV-LPDDR4 Pull-Up

The VOH.LTT values for 1.2V VccQ for the NV-LPDDR4 data interface with ZQ calibration are specified in Table 4-39.

Description	VOH.LTT setting	VOH.LTT Maximum	VOH.LTT Nominal @ 1.2V VCCQ	VOH.LTT Minimum	Unit
R_pullup	VCCQ/3	1.15 * VOH.LTTnom	400	0.85 * VOH.LTTnom	mV
R_pullup	VCCQ/2.5	1.15 * VOH.LTTnom	480	0.85 * VOH.LTTnom	mV

Notes:
1. VOH.LTT,nom = VccQ/3 is mandatory and shall be the default, while VOH.LTT,nom = VccQ/2.5 is optional.
2. VOH,nom accuracy requirements are after ZQ calibration with an RZQ of 300Ω +/- 1%
3. VOH,nom accuracy requirements only apply at valid CH_ODT values
4. Refer to Output Driver Sensitivity if either the temperature or the voltage changes after calibration.

Table 4-39 VOH Values for NV-LPDDR4 with ZQ calibration

4.13. Output Driver Sensitivity

If either the temperature or the voltage changes after ZQ calibration, then the tolerance limits listed in Table 4-36 or Table 4-38 can be expected to widen according to Table 4-40 and Table 4-41.

NV-DDR2/3				
Description	**VOUT to VssQ**	**Maximum**	**Minimum**	**Unit**
R_pulldown	0.2 x VccQ	1.15 + dRONdT x ΔT + dRONdV x ΔV	0.57 - dRONdT x ΔT - dRONdV x ΔV	%
	0.5 x VccQ	1.15 + dRONdT x ΔT + dRONdV x ΔV	0.85 - dRONdT x ΔT - dRONdV x ΔV	%
	0.8 x VccQ	1.47 + dRONdT x ΔT + dRONdV x ΔV	0.85 - dRONdT x ΔT - dRONdV x ΔV	%
R_pullup	0.2 x VccQ	1.47 + dRONdT x ΔT + dRONdV x ΔV	0.85 - dRONdT x ΔT - dRONdV x ΔV	%
	0.5 x VccQ	1.15 + dRONdT x ΔT + dRONdV x ΔV	0.85 - dRONdT x ΔT - dRONdV x ΔV	%
	0.8 x VccQ	1.15 + dRONdT x ΔT + dRONdV x ΔV	0.57 - dRONdT x ΔT - dRONdV x ΔV	%
NV-LPDDR4				
Description	**VOUT to VssQ**	**Maximum**	**Minimum**	**Unit**
R_pullup	VOH.LTTnom	1.15 + dVOHdT x ΔT + dVOHdV x ΔV	0.85 - dVOHdT x ΔT - dVOHdV x ΔV	%

Table 4-40 Output Driver Sensitivity Definition

Change	Maximum	Minimum	Unit
dRONdT	0.5	0	%/°C
dRONdV	0.2	0	%/mV
dVOHdT	0.5	0	%/°C
dVOHdV	0.2	0	%/mV

Table 4-41 Output Driver Voltage and Temperature Sensitivity

4.14. Input Slew Rate Derating

4.14.1. NV-DDR

The input slew rate requirements that the device shall comply with for the NV-DDR data interface are defined in Table 4-42. The testing conditions that shall be used to verify the input slew rate are listed in Table 4-43. Derating is required for input slew rates slower than 0.5 V/ns, refer to the vendor's datasheet.

Description	Timing Modes 0-5	Unit
Input slew rate (min)	0.5	V/ns
Input slew rate (max)	4.5	V/ns

Table 4-42 Input Slew Rate Requirements

Parameter	Value
Positive input transition	VIL (DC) to VIH (AC)
Negative input transition	VIH (DC) to VIL (AC)

Table 4-43 Testing Conditions for Input Slew Rate

4.14.2. NV-DDR2/NV-DDR3

The minimum and maximum input slew rate requirements that the device shall comply with for the NV-DDR2 and NV-DDR3 data interface are defined in Table 4-44 for all timing modes. If the input slew rate falls below the minimum value, then derating shall be applied. At data rates where the Input DQ Rx Mask is applied (>1600MT/s), the input slew rate on DQ[7:0] and DBI must not fall below the minimum slew rate as specified in the Table 4-44 NV-DDR2/3 Maximum and Minimum Input Slew Rate and no derating is applied.

Description	Single Ended	Differential	Unit
Input slew rate (min)	1.0	2.0	V/ns
Input slew rate (max)	4.5	9.0	V/ns

Table 4-44 NV-DDR2/3 Maximum and Minimum Input Slew Rate

For DQ signals when used for input, the total data setup time (tDS) and data hold time (tDH) required is calculated by adding a derating value to the tDS and tDH values indicated for the timing mode. To calculate the total data setup time, tDS is incremented by the appropriate ∆set

derating value. To calculate the total data hold time, tDH is incremented by the appropriate ∆hld derating value. Table 4-45 provides the NV-DDR2 derating values when differential DQS (DQS_t/DQS_c) is used. Table 4-46 provides the NV-DDR2 derating values when single-ended DQS is used. Table 4-47 provides the NV-DDR3 derating values when differential DQS (DQS_t/DQS_c) is used. Table 4-48 provides the NV-DDR3 derating values when single-ended DQS is used. Table 4-49 provides the NV-DDR3 derating value when the input timing is measured as a Tsu+Thd window.

The setup nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREFQ(DC) and the first crossing of VIH(AC) min. The setup nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREFQ(DC) and the first crossing of VIL(AC) max. If the actual signal is always earlier than the nominal slew rate line between the shaded 'VREFQ(DC) to AC region', then the derating value uses the nominal slew rate shown in Figure 4-12. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREFQ(DC) to AC region', then the derating value uses the slew rate of a tangent line to the actual signal from the AC level to the DC level shown in Figure 4-13.

The hold nominal slew rate for a rising signal is defined as the slew rate between the first crossing of VIL(DC) max and the first crossing of VREFQ(DC). The hold nominal slew rate for a falling signal is defined as the slew rate between the first crossing of VIH(DC) min and the first crossing of VREFQ(DC). If the actual signal is always later than the nominal slew rate line between shaded 'DC to VREFQ(DC) region', then the derating value uses the nominal slew rate shown in Figure 4-14. If the actual signal is earlier than the nominal slew rate line anywhere between the shaded 'DC to VREFQ(DC) region', then the derating value uses the slew rate of a tangent line to the actual signal from the DC level to the VREFQ(DC) level shown in Figure 4-15.

If the tangent line is used for derating, the setup and hold values shall be derated from where the tangent line crosses VREFQ(DC), not the actual signal (refer to Figure 4-13 and Figure 4-15).

The input differential DQS slew rate measurement is defined in Figure 4-11

For slew rates not explicitly listed in Table 4-45, Table 4-46, Table 4-47, and Table 4-48 the derating values should be obtained by linear interpolation. These values are typically not subject to production test; the values are verified by design and characterization.

Shaded areas indicate input slew rate combinations not supported.

DQ V/ns	DQS_t/DQS_c Slew Rate Derating VIH/L(AC) = 250 mV, VIH/L(DC) = 125 mV																							
	12		6		4		3		2		1.8		1.6		1.4		1.2		1		0.8		0.6	
	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld
6	-26	-26	-21	-21	-16	-16																		
3	-26	-26	-21	-21	-16	-16	-10	-10																
2			-21	-21	-16	-16	-10	-10	0	0														
1.5					-16	-16	-10	-10	0	0	7	7												
1					-16	-16	-10	-10	0	0	7	7	16	16										
0.9							3	3	14	14	21	21	30	30	41	41								
0.8									31	31	38	38	47	47	58	58	73	73						
0.7											61	61	69	69	80	80	95	95	116	116				
0.6													99	99	110	110	125	125	146	146	176	176		
0.5															152	152	167	167	188	188	218	218	269	269
0.4																	229	229	250	250	282	282	333	333
0.3																			355	355	385	385	436	436

Table 4-45 NV-DDR2 Input Slew Rate Derating Values for DQ and differential DQS

Shaded areas indicate input slew rate combinations not supported.

DQ V/ns	DQS Slew Rate Derating VIH/L(AC) = 250 mV, VIH/L(DC) = 125 mV																							
	6		5		3		2		1.5		1		0.9		0.8		0.7		0.6		0.5		0.4		0.3	
	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld
6	0	0	0	0																						
5	0	0	0	0	0	0																				
4			0	0	0	0	0	0																		
3			0	0	0	0	0	0	0	0																
2					0	0	0	0	0	0	0	0														
1.5					0	0	0	0	0	0	0	0	14	14												
1							0	0	0	0	0	0	14	14	31	31										
0.9									14	14	14	14	28	28	45	45	67	67								
0.8											31	31	45	45	63	63	85	85	115	115						
0.7													67	67	85	85	107	107	137	137	179	179				
0.6															115	115	137	137	167	167	208	208	271	271		
0.5																	179	179	208	208	250	250	313	313	418	418
0.4																			271	271	313	313	375	375	480	480
0.3																					418	418	480	480	594	594

Table 4-46 NV-DDR2 Input Slew Rate Derating Values for DQ and single-ended DQS

Shaded areas indicate input slew rate combinations not supported. Slew rates below 0.4V/ns are not supported 1066/1200 MT/s operation. Slew rates below 1.0V/ns are not supported for >1200MT/s operation.

DQ V/ns	DQS_t/DQS_c Slew Rate Derating VIH/L(AC) = 150 mV, VIH/L(DC) = 100 mV																							
	12		6		4		3		2		1.8		1.6		1.4		1.2		1		0.8		0.6	
	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld
6	–63	–31	–33	–17	-25	-13																		
3	–63	–31	–33	–17	–25	–13	-17	-8																
2			–33	–17	–25	–13	–17	–8	0	0														
1.5					–25	–13	–17	–8	0	0	6	6												
1					–25	–13	–17	–8	0	0	6	6	13	13										
0.9							–6	3	11	11	17	17	24	24	33	33								
0.8									25	25	31	31	38	38	46	46	58	58						
0.7											48	48	55	55	64	64	76	76	93	93				
0.6													79	79	88	88	100	100	117	117	142	142		
0.5															121	121	133	133	150	150	175	175	217	217
0.4																	183	183	200	200	225	225	267	267
0.3																			283	283	308	308	350	350

Table 4-47 NV-DDR3 Input Slew Rate Derating Values for DQ and differential DQS

Shaded areas indicate input slew rate combinations not supported. Slew rates below 0.4V/ns are not supported for 1066/1200 MT/s operation. Slew rates below 1.0V/ns are not supported for >1200MT/s operation.

DQ V/ns	DQS Slew Rate Derating VIH/L(AC) = 150 mV, VIH/L(DC) = 100 mV																									
	6		5		3		2		1.5		1		0.9		0.8		0.7		0.6		0.5		0.4		0.3	
	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld
6	0	0	0	0	0	0																				
5	0	0	0	0	0	0	0	0																		
3	0	0	0	0	0	0	0	0	0	0																
2			0	0	0	0	0	0	0	0	0	0														
1.5					0	0	0	0	0	0	0	0	11	11												
1							0	0	0	0	0	0	11	11	25	25										
0.9									11	11	11	11	22	22	36	36	54	54								
0.8											25	25	36	36	50	50	68	68	92	92						
0.7													54	54	68	68	86	86	110	110	143	143				
0.6															92	92	110	110	133	133	167	167	217	217		
0.5																	143	143	167	167	200	200	250	250	333	333
0.4																			217	217	250	250	300	300	383	383
0.3																					333	333	383	383	467	467

Table 4-48 NV-DDR3 Input Slew Rate Derating Values for DQ and single-ended DQS

DQ Slew Rate	∆ Setup + Hold
≥1.0 V/ns	0 ps
0.9 V/ns	22 ps
0.8 V/ns	50 ps
0.7 V/ns	86 ps
0.6 V/ns	133 ps
0.5V/ns	200 ps
0.4 V/ns	300 ps

Table 4-49 NV-DDR3 Input Slew Rate Derating Values for DQ Window

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (DQS_t – DQS_c)	VILdiff(DC)	VIHdiff(DC)	[VIHdiff(DC) – VILdiff(DC)] / Delta tRISEdiff
Differential input slew rate for falling edge (DQS_t – DQS_c)	VIHdiff(DC)	VILdiff(DC)	[VIHdiff(DC) – VILdiff(DC)] / Delta tFALLdiff
NOTE: The differential signal must be linear between these thresholds.			

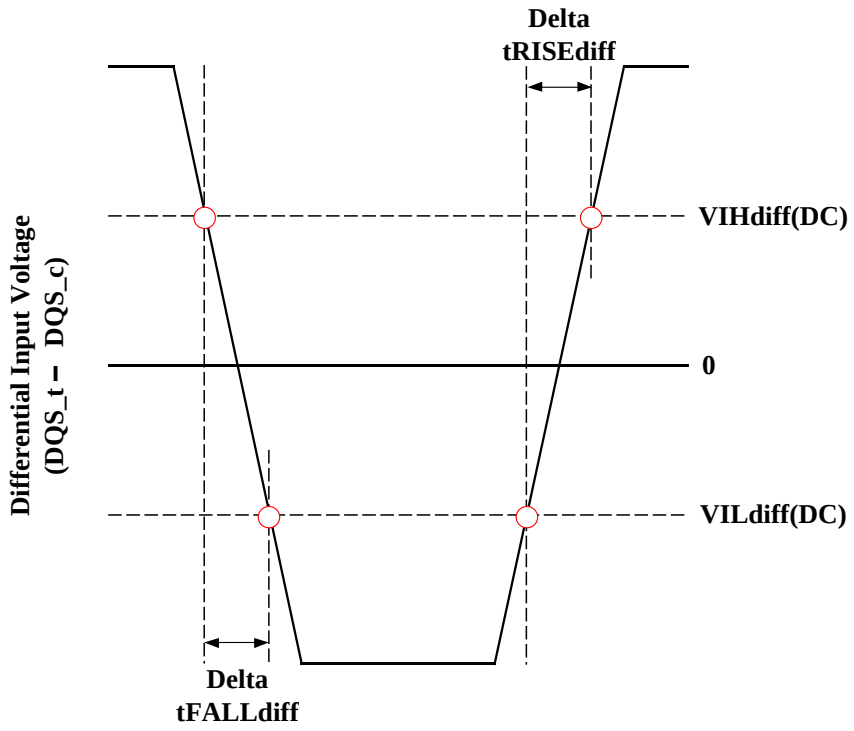


Figure 4-11 Differential Input Slew Rate Definition for DQS_t, DQS_c

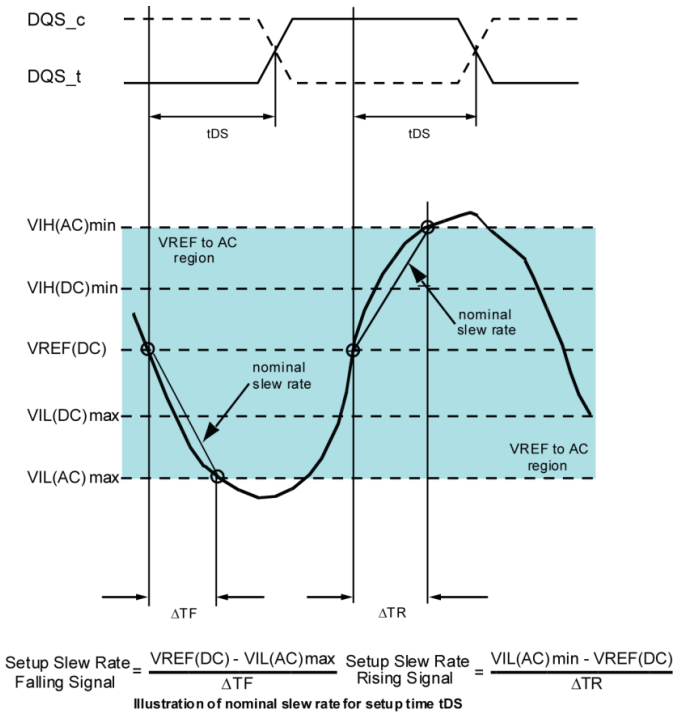


Figure 4-12 Nominal Slew Rate for Data Setup Time (tDS)

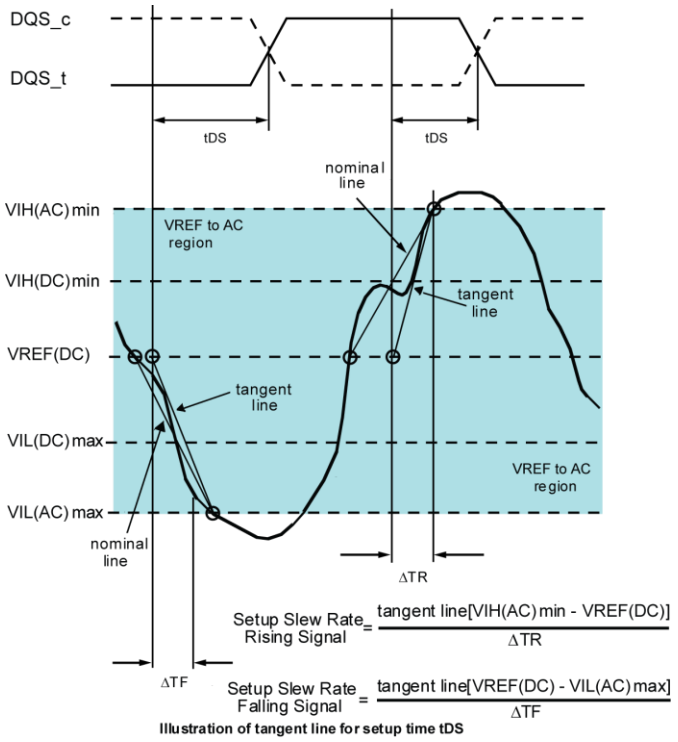


Figure 4-13 Tangent Line for Data Setup Time (tDS)

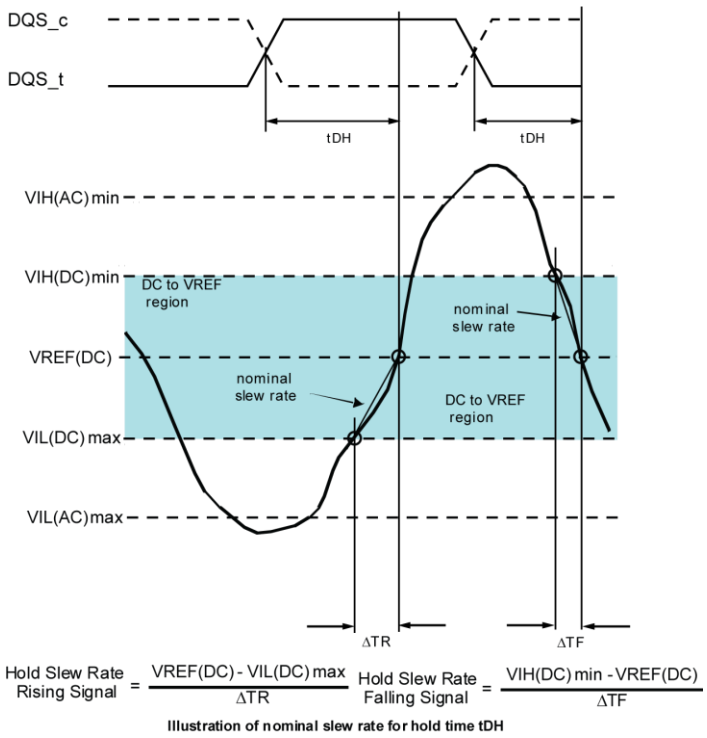


Figure 4-14 Nominal Slew Rate for Data Hold Time (tDH)

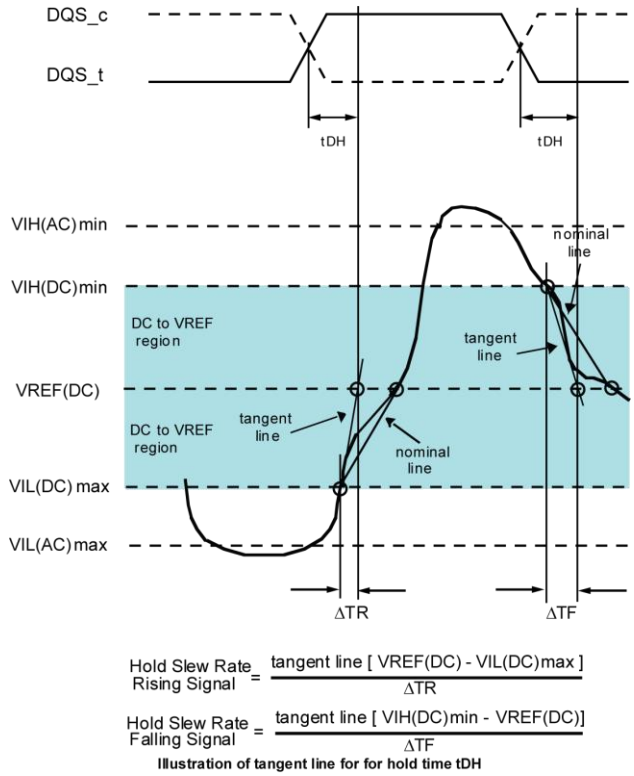


Figure 4-15 Tangent Line for Data Hold Time (tDH)

4.14.3. NV-LPDDR4

For the NV-LPDDR4 interface, the input slew rate on DQ[7:0] and DBI must not fall below the minimum slew rate as specified in the Table 4-50 NV-LPDDR4 Maximum and Minimum Input Slew Rate and no derating is applied.

Description	Single Ended	Differential	Unit
Input slew rate (min)	1.0	2.0	V/ns
Input slew rate (max)	4.5	9.0	V/ns

Notes:
1. Input Slew Rate = (Vcent_DQ – VIL.LTT(DC)) / ΔTF and (VIH.LTT(DC) – Vcent_DQ) / ΔTR

Table 4-50 NV-LPDDR4 Maximum and Minimum Input Slew Rate

4.15. Differential Signaling (NV-DDR2/NV-DDR3/NV-LPDDR4)

An enabler for higher speed operation is differential signaling for the RE_n and DQS signals. For the NV-DDR2/NV-DDR3 interfaces, complementary RE_n and complementary DQS signal may be optionally used to create differential signal pairs (RE_t/RE_c and DQS_t/DQS_c). When using differential signaling, RE_n is referred to as RE_t and DQS is referred to as DQS_t, i.e., the “true” versions of the signals. Differential signaling may be used to improve signal integrity through enhanced noise immunity. Differential signaling is supported for the NV-DDR2, NV-DDR3 and NV-LPDDR4 data interfaces only. For the NV-LPDDR4 interface, differential signaling for both RE_n and DQS signals are required and must be enabled prior to enabling the interface.

A device may support differential RE_n and/or differential DQS signaling. The support for differential RE_n and/or DQS is reported in the parameter page. By default, differential signaling is disabled. The host may configure the device to use differential signaling using the NV-DDR2/NV-DDR3/NV-LPDDR4 Configuration feature, refer to section 5.31.2. Complementary RE_n (i.e., RE_c) and complementary DQS (i.e., DQS_c) signals are individually configured/enabled.

Differential signaling is active when the selected data interface is NV-DDR2, NV-DDR3 or NV-LPDDR4 and differential signaling is enabled in the NV-DDR2/NV-DDR3/NV-LPDDR4 Configuration feature. For devices that support the NV-DDR2 interface, prior to enabling the NV-DDR2 interface it is recommended that the NV-DDR2/NV-DDR3/NV-LPDDR4 Configuration feature be configured using the SDR data interface. For NV-DDR2, NV-DDR3 interfaces, after changing the state of the differential signaling setting in the NV-DDR2/NV-DDR3/NV-LPDDR4 Configuration feature, the host shall transition CE_n high before issuing subsequent commands to avoid any signal integrity issues.

In NV-DDR2, if there is a Reset (FFh) operation, differential signaling is disabled. In NV-DDR3 and NV-LPDDR4 however, differential signaling settings are retained across a Rest (FFh) operation. Synchronous Reset (FCh) and Reset LUN (FAh) have no effect on differential signaling.

The differential AC input parameters are specified in Table 4-51. VIX(AC) indicates the voltage at which differential input signals shall cross. The typical value of VIX(AC) is expected to be 0.5 x VccQ of the transmitting device. VIX(AC) is expected to track variations in VccQ.

		Timing Mode 0-12		Timing Mode 13-19		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
AC differential input cross-point voltage relative to VccQ / 2	VIX(AC)	NV-DDR2: 0.50 x VccQ - 175	NV-DDR2: 0.50 x VccQ + 175			mV
		NV-DDR3: 0.50 x VccQ – 120	NV-DDR3: 0.50 x VccQ + 120	NV-DDR3: 0.50 x VccQ – 80	NV-DDR3: 0.50 x VccQ + 80	
AC differential input cross-point voltage relative to VREFQ	VIX(AC)	NV-LPDDR4: VREFQ – 64	NV-LPDDR4: VREFQ + 64	NV-LPDDR4: VREFQ – 64	NV-LPDDR4: VREFQ + 64	mV

Table 4-51 Differential AC Input Parameters

4.16. Warmup Cycles (NV-DDR2/NV-DDR3/NV-LPDDR4)

In order to support higher speed operation, warmup cycles for data output and data input may be provided. Warmup cycles are supported for the NV-DDR2, NV-DDR3 and NV-LPDDR4 data interfaces only.

Warmup cycles for data output provide extra RE_n and corresponding DQS transitions at the beginning of a data output burst. These extra RE_n/DQS transitions do not have any data associated with them. The number of extra cycles is configured via the NV-DDR2/NV-DDR3/NV-LPDDR4 Configuration feature address, refer to section 5.31.2. The number of cycles specified includes a full data output cycle (both rising and falling edge for RE_n and DQS).

Warmup cycles for data input provide extra DQS transitions at the beginning of a data input burst. These extra DQS transitions do not have any data associated with them. The number of extra cycles is configured via the NV-DDR2/NV-DDR3/NV-LPDDR4 Configuration feature address, refer to section 5.31.2. The number of cycles specified includes a full data input cycle (both rising and falling edge for DQS).

Warmup cycles are optional for both data output and data input, and if used, do not need to be configured to the same value. Warmup cycles apply to all commands, including SDR commands (refer to section 4.4). The warmup cycles shall be initiated at the start of each data burst when warmup cycles are enabled for that data transfer type. If the host pauses and then resumes a data transfer without exiting and re-entering the data burst, then the host shall not issue additional warmup cycles. Exiting and re-entering the data burst shall be performed by bringing ALE, CLE or CE_n high without latching with WE_n. In the case of not re-issuing warmup cycles, the host should take care to avoid signal integrity issues due to pausing the data transfer and resuming without warmup cycles.

Warmup cycles are active when the selected data interface is NV-DDR2, NV-DDR3 or NV-LPDDR4 and warmup cycles are enabled in the NV-DDR2/NV-DDR3/NV-LPDDR4 Configuration feature. For NV-DDR2, it is recommended that the NV-DDR2/NV-DDR3/NV-LPDDR4 Configuration feature be configured using the SDR data interface. If warmup cycles are enabled while the NV-DDR2, NV-DDR3 or NV-LPDDR4 interface is active, then warmup cycles shall be used for all subsequent commands after the Set Features is complete.

Figure 4-16 shows an example of warmup cycles for data output, where the number of warmup cycles is two. As illustrated, the first byte of data is transmitted to the host as part of the third rising transition of DQS.

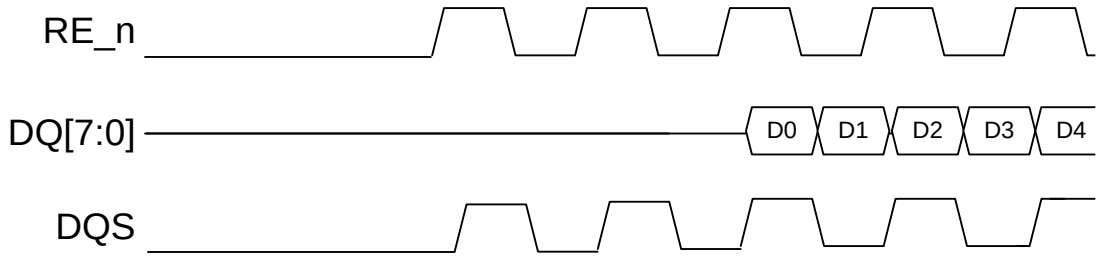


Figure 4-16 Warmup Cycles for Data Output

4.17. On-die Termination (NV-DDR2/NV-DDR3/NV-LPDDR4)

On-die termination (ODT) may be required at higher speeds depending on system topology. This section describes the mechanism for on-die termination on the DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c signals. On-die termination is an optional capability that may be employed to meet higher speeds in particular topologies. If power needs to be optimized in a particular condition, then on-die termination may be disabled, and the topology may potentially need to be run at a slower speed. On-die termination is supported for the NV-DDR2, NV-DDR3 and NV-LPDDR4 data interfaces only.

On-die termination settings are configured during initialization. The host may configure on-die termination in a self-termination only configuration, or it may configure a more flexible on-die termination scheme utilizing matrix termination, which enables a mixture of Target and non-Target termination to be specified.

For the more flexible ODT configuration, referred to as matrix termination, the host configures a matrix that defines the LUN(s) that terminate for a particular Volume. This matrix is configured using the ODT Configure command defined in section 5.25. For the simple configuration of self-termination only ODT, no ODT matrix configuration is required.

ODT is enabled and disabled based on the type of cycle (on for data input and output cycles, off for command, and address cycles). On-die termination applies for data input and output cycles for all commands.

When on-die termination is enabled via the NV-DDR2/NV-DDR3/NV-LPDDR4 Configuration feature address, the default is self-termination only. To use matrix termination for non-Target termination or termination topologies that use multiple terminators, the Volume address mechanism shall be used and the on-die termination configuration matrix shall be specified using the ODT Configure command. If using matrix termination, the ODT Configure command shall be issued to at least one LUN on all NAND Targets. As part of the ODT Configure command, Rtt settings may be specified on a per LUN basis with individual values for:

- RE_n Rtt,
- DQ[7:0] and DQS for data output Rtt, and
- DQ[7:0] and DQS for data input Rtt

On-die termination is disabled when ALE, CLE or CE_n transitions from low to high.

The on-die termination DC electrical characteristics are specified in Table 4-52 (NV-DDR2 without ZQ calibration), Table 4-53 (NV-DDR3 without ZQ calibration) and Table 4-54 (NV-DDR2/3 with ZQ calibration). RttEff1, RttEff2, RttEff3, RttEff4, and RttEff5 are determined by separately applying VIH(AC) and VIL(AC) to the ball being tested, and then measuring current I(VIH[AC]) and I(VIL[AC]), respectively. The equation is:

RttEff = (VIH[AC] – VIL[AC]) / {I(VIH[AC]) – I(VIL[AC]}

The measurement voltage (VM) is at the tested ball with no load. The deviation of VM with respect to VccQ / 2 is defined as:

$\Delta VM = \{(2 \times VM)/VccQ - 1\} \times 100$

Parameter	Symbol	Min	Nom	Max	Unit	Optional or Mandatory
Rtt effective Impedance value for 30 Ohms setting	RttEff1	19.5	30	40.5	Ohms	Optional
Rtt effective impedance value for 50 Ohms setting	RttEff2	32.5	50	67.5	Ohms	Mandatory
Rtt effective impedance value for 75 Ohms setting	RttEff3	48.7	75	101.3	Ohms	Mandatory
Rtt effective impedance value for 100 Ohms setting	RttEff4	65	100	135	Ohms	Optional[1]
Rtt effective impedance value for 150 Ohms setting	RttEff5	97.5	150	202.5	Ohms	Mandatory
Deviation of VM with respect to VccQ/2	ΔVM	-7	-	7	%	Mandatory

NOTE:
1. Devices that support 37.5 Ohms and not 35 Ohms do not support Rtt = 100 Ohms.

Table 4-52 On-die Termination DC Electrical Characteristics, NV-DDR2 without ZQ calibration

Parameter	Symbol	Min	Nom	Max	Unit	Optional or Mandatory
Rtt effective Impedance value for 50 Ohms setting	RttEff1	32.5	50	80	Ohms	Mandatory
Rtt effective impedance value for 75 Ohms setting	RttEff2	48.5	75	120	Ohms	Mandatory
Rtt effective impedance value for 100 Ohms setting	RttEff3	65	100	160	Ohms	Optional[1]
Rtt effective impedance value for 150 Ohms setting	RttEff4	97.5	150	240	Ohms	Mandatory
Deviation of VM with respect to VccQ/2	ΔVM	-7	-	7	%	

NOTE:
1. Devices that support 37.5 Ohms and not 35 Ohms do not support Rtt = 100 Ohms.

Table 4-53 On-die Termination DC Electrical Characteristics, NV-DDR3 without ZQ calibration

Parameter	Symbol	Min	Nom	Max	Unit
Rtt effective Impedance value	RttEff	See Table 4-55			
Deviation of VM with respect to VccQ/2	ΔVM	7	-	7	%

Table 4-54 On-die Termination DC Electrical Characteristics, NV-DDR2 and NV-DDR3 with ZQ calibration

	Rtt = 50 Ohms					
Rtt	**Resistor**	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
50 Ohm (optional)	R_pulldown[5]	0.2 x VccQ	1.15	1.0	0.57	RZQ/3
		0.5 x VccQ	1.15	1.0	0.85	RZQ/3
		0.8 x VccQ	1.47	1.0	0.85	RZQ/3
	R_pullup[5]	0.2 x VccQ	1.47	1.0	0.85	RZQ/3
		0.5 x VccQ	1.15	1.0	0.85	RZQ/3
		0.8 x VccQ	1.15	1.0	0.57	RZQ/3
50 Ohm (required)		VIL(AC) to VIH (AC)	1.67	1.0	0.85	RZQ/6
	Rtt = 75 Ohms					
Rtt	**Description**	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
75 Ohm (optional)	R_pulldown[5]	0.2 x VccQ	1.15	1.0	0.57	RZQ/2
		0.5 x VccQ	1.15	1.0	0.85	RZQ/2
		0.8 x VccQ	1.47	1.0	0.85	RZQ/2
	R_pullup[5]	0.2 x VccQ	1.47	1.0	0.85	RZQ/2
		0.5 x VccQ	1.15	1.0	0.85	RZQ/2
		0.8 x VccQ	1.15	1.0	0.57	RZQ/2
75 Ohm (required)		VIL(AC) to VIH (AC)	1.67	1.0	0.85	RZQ/4
	Rtt = 100 Ohms[4]					
Rtt	**Description**	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
100 Ohm (optional)	R_pulldown[5]	0.2 x VccQ	1.15	1.0	0.57	RZQ/1.5
		0.5 x VccQ	1.15	1.0	0.85	RZQ/1.5
		0.8 x VccQ	1.47	1.0	0.85	RZQ/1.5
	R_pullup[5]	0.2 x VccQ	1.47	1.0	0.85	RZQ/1.5
		0.5 x VccQ	1.15	1.0	0.85	RZQ/1.5
		0.8 x VccQ	1.15	1.0	0.57	RZQ/1.5
100 Ohm (required)		VIL(AC) to VIH (AC)	1.67	1.0	0.85	RZQ/3
	Rtt = 150 Ohms					
Rtt	**Description**	**VOUT to VssQ**	**Maximum**	**Nominal**	**Minimum**	**Unit**
150 Ohm (optional)	R_pulldown[5]	0.2 x VccQ	1.15	1.0	0.57	RZQ/1
		0.5 x VccQ	1.15	1.0	0.85	RZQ/1
		0.8 x VccQ	1.47	1.0	0.85	RZQ/1
	R_pullup[5]	0.2 x VccQ	1.47	1.0	0.85	RZQ/1
		0.5 x VccQ	1.15	1.0	0.85	RZQ/1
		0.8 x VccQ	1.15	1.0	0.57	RZQ/1
150 Ohm (required)		VIL(AC) to VIH (AC)	1.67	1.0	0.85	RZQ/2

NOTE:
1. Tolerance limits assume RZQ of 300Ω +/- 1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
2. Refer to ODT Sensitivity if either the temperature or the voltage changes after calibration.
3. The minimum values are derated by 6% when the device operates between –40°C and 0°C (TC).
4. Devices that support 37.5 Ohms and not 35 Ohms do not support Rtt = 100 Ohms.
5. The Rtt R_pulldown and R_pullup specifications are not specification requirements but can be used as design guidelines. The Rtt Maximum, Nominal and Minimum specifications though for a VOUT to VssQ between VIL(AC) to VIH(AC), are specification requirements.

Table 4-55 Rtt effective impedances, NV-DDR2 and NV-DDR3 with ZQ calibration

Rtt	VOUT to VssQ	Maximum	Nominal	Minimum	Unit
25 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/12
	0.33 x VccQ	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
37.5 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/8
	0.33 x VccQ	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
42.9 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/7
	0.33 x VccQ	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
50 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/6
	0.33 x VccQ	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
60 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/5
	0.33 x VccQ	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
75 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/4
	0.33 x VccQ	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
100 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/3
	0.33 x VccQ	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
150 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/2
	0.33 x VccQ	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
300 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/1
	0.33 x VccQ	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	

NOTE:
1. Tolerance limits assume RZQ of 300Ω +/- 1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
2. Refer to ODT Sensitivity if either the temperature or the voltage changes after calibration.
3. The minimum values are derated by 6% when the device operates between –40°C and 0°C (TC).

Table 4-56 Rtt effective impedances, NV-LPDDR4 with ZQ calibration

4.17.1. ODT Sensitivity

If either the temperature or the voltage changes after ZQ calibration, then the ODT tolerance limits listed in Table 4-55 can be expected to widen according to Table 4-57 and Table 4-58. ODT sensitivity specifications are not tested in production but are simulated and characterized.

Description	Maximum	Minimum	Unit
Rtt for NV-DDR2/3	1.67 + dRTTdT x ΔT + dRTTdV x ΔV	0.85 - dRTTdT x ΔT - dRTTdV x ΔV	RZQ/(2,3,4,6)[1] RZQ/(2,4,6)[2]
Rtt for NV-LVDDR4	1.15 + dRTTdT x ΔT + dRTTdV x ΔV	0.85 - dRTTdT x ΔT - dRTTdV x ΔV	RZQ/n

NOTE:
1. If device supports 35 Ohms.
2. If device supports 37.5 Ohms and not 35 Ohms.
3. NV-LPDDR4 interface Rtt Maximum and Minimum specifications in this table are referenced at 0.33 x VccQ. The ODT Voltage and Temperature Sensitivity specs dRTTdT and dRTTdV are also referenced at 0.33 x VccQ.

Table 4-57 ODT Sensitivity Definition

Change	Maximum	Minimum	Unit
dRTTdT	0.5	0	%/°C
dRTTdV	0.2	0	%/mV

Table 4-58 ODT Voltage and Temperature Sensitivity

4.17.2. Self-termination ODT

When self-termination is enabled, the LUN that is executing the command provides on-die termination.

Figure 4-17 defines self-termination only ODT enable and disable requirements for the LUN that is the executing the command when self-termination ODT is enabled. Self-termination ODT is enabled using Set Features with the NV-DDR2/NV-DDR3 Configuration feature. If the ODT Configure command is issued to a LUN on a Target, then the ODT mechanism used for that Target changes to matrix termination (refer to section 4.17.3).

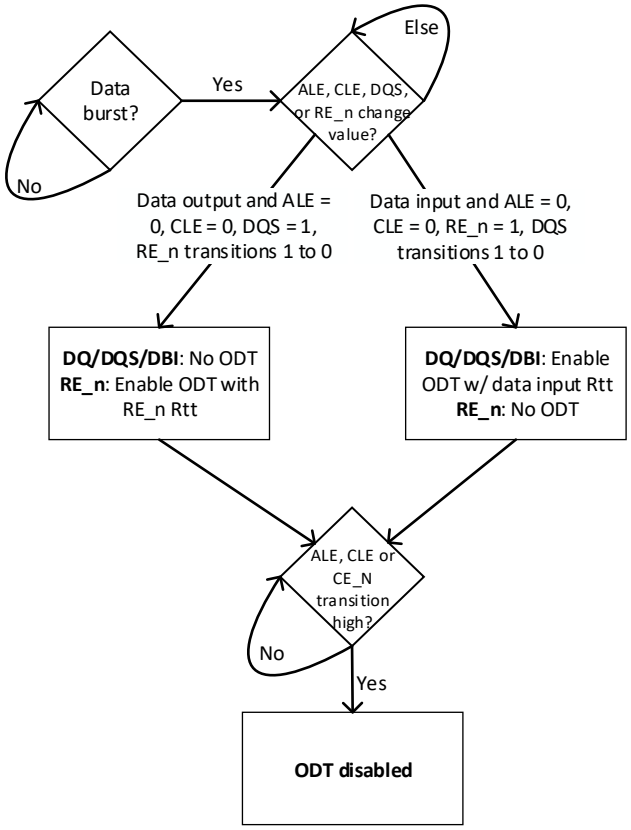


Figure 4-17 Self-termination only ODT Behavioral Flow

4.17.3. Matrix Termination

A LUN that is configured to act as a terminator using the configuration matrix (that is specified with the ODT Configure command) may be located on the same Volume as the Volume it is

terminating for (Target termination) or a separate Volume (non-Target termination). Based on the ODT configuration and the Volume a command is addressed to, LUNs enter different states which determine their ODT behavior; those states are listed in Table 4-59.

LUN is on Selected Volume ?	Terminator for Selected Volume ?	LUN State	ODT Actions Defined
Yes	na	Selected	Figure 4-18
No	Yes	Sniff	Figure 4-19
No	No	Deselected	No ODT actions

Table 4-59 LUN State for Matrix Termination

The LUN that a command is addressed to for execution may provide termination. Other LUNs on the selected Volume that are not responsible for execution of the command may also provide termination. Figure 4-18 defines the ODT actions required for LUNs of each of these types on the selected Volume. LUNs on the selected Volume remain in an active state, and thus are aware of state information like whether there is a data burst currently and the type of cycle; these LUNs do not rely only on ALE, CLE, DQS and RE_n signals.

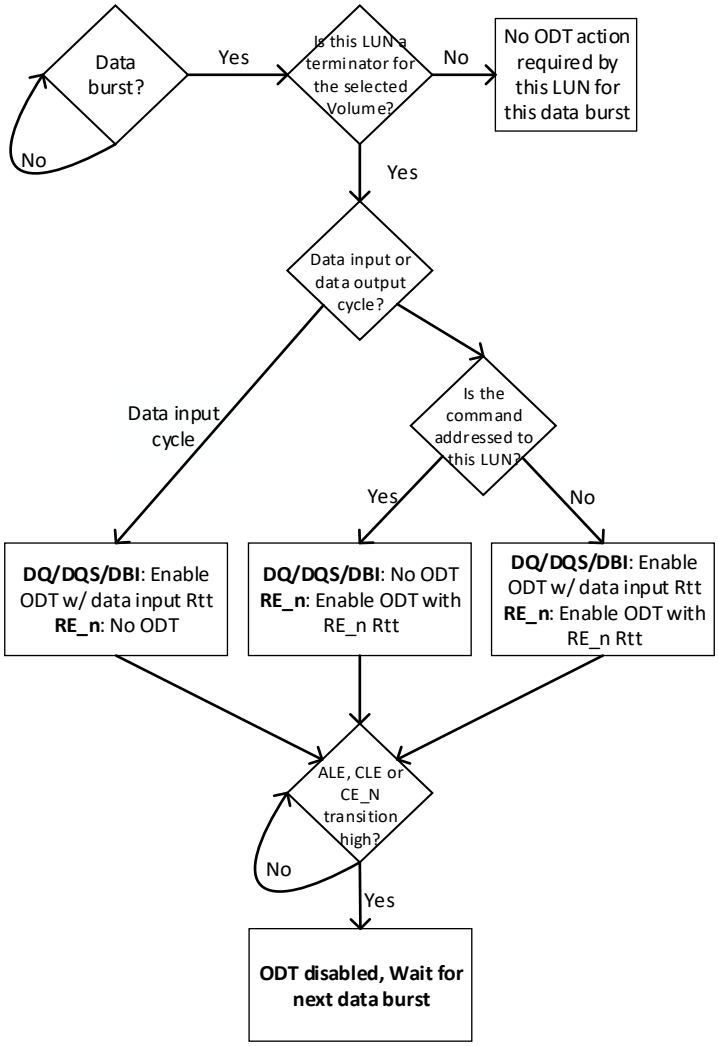


Figure 4-18 ODT Actions for LUNs on Selected Volume

The ODT configuration matrix also offers the flexibility of having LUNs on an unselected Volume provide termination for the selected Volume. When a LUN is placed in the Sniff state, it checks the ALE, CLE, DQS and RE_n signals to determine when to enable or disable ODT. Figure 4-19 defines the ODT actions for LUNs in the Sniff state on an unselected Volume.

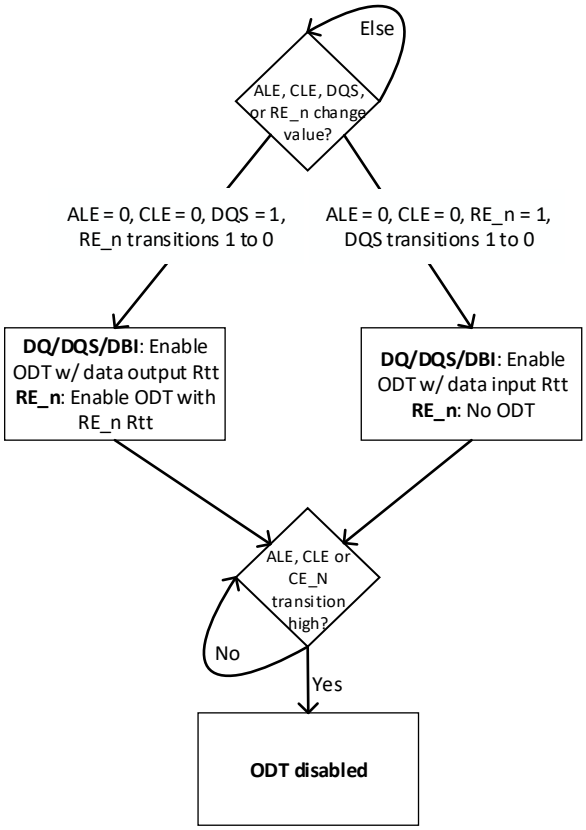


Figure 4-19 ODT Actions for LUNs in Sniff State on Unselected Volume

4.17.3.1. Matrix Termination Examples (Informative)

This section describes two examples of on-die termination configurations using matrix termination. In both examples, each Volume consists of two LUNs, referred to as H0N*n*-LUN0 and H0N*n*-LUN1. The following Volume addresses were appointed at initialization.

Volume	Appointed Volume Address
H0N0	0
H0N1	1
H0N2	2
H0N3	3

Table 4-60 Matrix Termination Example: Appointed Volume Addresses

For optimal signal integrity and power consumption, the host may configure termination in a variety of ways. The host may configure a LUN to self terminate, perform non-Target termination for another Volume, or not perform any termination function. Using matrix termination, the termination Rtt values may be set differently for each LUN configured as a terminator, including the ability to specify different settings for data output operation and data input operation. The first

example shows that a controller may configure the ODT matrix to perform stronger non-Target ODT for data output operations and weaker Target ODT for data input operations.

Refer to the ODT Configure Definition section on page 303 for definition of the ODT Configuration Matrix bits (i.e. M0, M1, Rtt1, Rtt2) used in the Matrix Termination examples in this section.

LUN	M0	M1	Rtt1	Rtt2	Notes
H0N0-LUN0	0Ch	00h	40h	00h	Terminates for Volumes 2 and 3 (non-Target) for data output with an Rtt value of 50 Ohms for DQ[7:0]/DQS.
H0N0-LUN1	01h	00h	02h	03h	Terminates for Volume 0 (Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE_n (RE_t/RE_c).
H0N1-LUN0	02h	00h	02h	03h	Terminates for Volume 1 (Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE_n (RE_t/RE_c).
H0N1-LUN1	00h	00h	00h	00h	Does not act as a terminator.
H0N2-LUN0	00h	00h	00h	00h	Does not act as a terminator.
H0N2-LUN1	04h	00h	02h	03h	Terminates for Volume 2 (Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE_n (RE_t/RE_c).
H0N3-LUN0	08h	00h	02h	03h	Terminates for Volume 3 (Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE_n (RE_t/RE_c).
H0N3-LUN1	03h	00h	40h	00h	Terminates for Volumes 0 and 1 (non-Target) for data output with an Rtt value 50 Ohms for DQ[7:0]/DQS.

Table 4-61 Matrix Termination Example 1

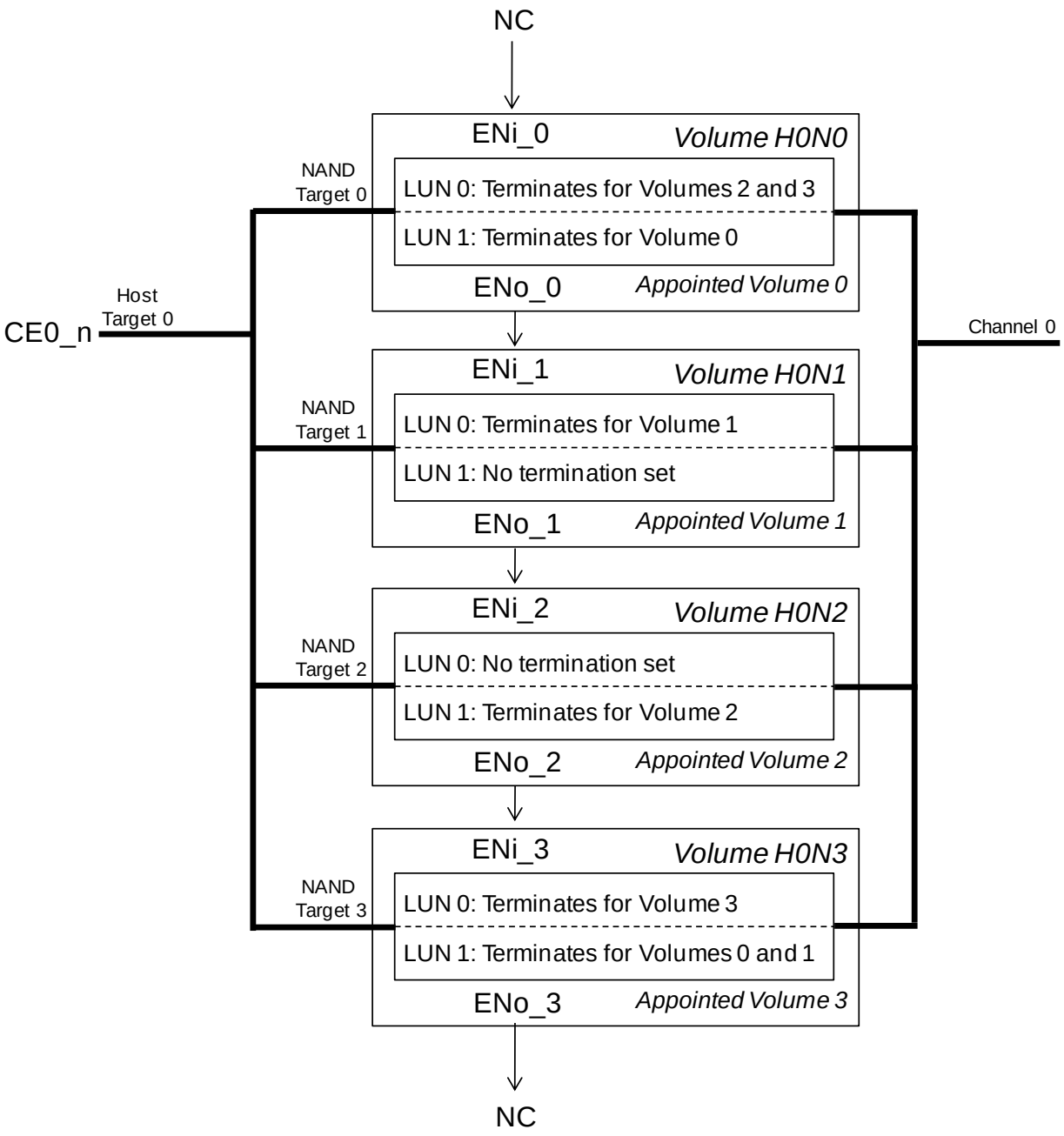


Figure 4-20 Example: Non-Target ODT for Data Output, Target ODT for Data Input

The second example uses parallel non-Target termination to achieve a stronger effective Rtt value for both data output and data input operations. For data output, two 50 Ohm terminators are used in parallel to achieve an effective 25 Ohms non-Target termination value. For data input, two 100 Ohm terminators are used in parallel to achieve an effective 50 Ohms non-Target termination value. This type of ODT matrix allows for stronger termination than may be available through a single device. It also allows for intermediate Rtt values with the use of different Rtt values for parallel LUNs. For example, if one terminator was configured for 75 Ohms and another terminator was configured for 100 Ohms for the same Volume then an effective Rtt value of 43 Ohms is achieved. In this example, parallel termination is used for data input and data output for

DQ[7:0]/DQS, however, RE_n (RE_t/RE_c) is non-Target terminated with 100 Ohms using a single LUN.

LUN	M0	M1	Rtt1	Rtt2	Notes
H0N0-LUN0	0Ch	00h	42h	00h	Terminates for Volumes 2 and 3 (non-Target) for data output with an Rtt value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 2 and 3 (non-Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS.
H0N0-LUN1	0Ch	00h	42h	01h	Terminates for Volumes 2 and 3 (non-Target) for data output with an Rtt value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 2 and 3 (non-Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS. Terminates for Volumes 2 and 3 (non-Target) with an Rtt value of 150 Ohms for RE_n (RE_t/RE_c).
H0N1-LUN0	00h	00h	00h	00h	Does not act as a terminator.
H0N1-LUN1	00h	00h	00h	00h	Does not act as a terminator.
H0N2-LUN0	00h	00h	00h	00h	Does not act as a terminator.
H0N2-LUN1	00h	00h	00h	00h	Does not act as a terminator.
H0N3-LUN0	03h	00h	42h	01h	Terminates for Volumes 0 and 1 (non-Target) for data output with an Rtt value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) with an Rtt value of 150 Ohms for RE_n (RE_t/RE_c).
H0N3-LUN1	03h	00h	42h	00h	Terminates for Volumes 0 and 1 (non-Target) for data output with an Rtt value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS.

Table 4-62 Matrix Termination Example 2

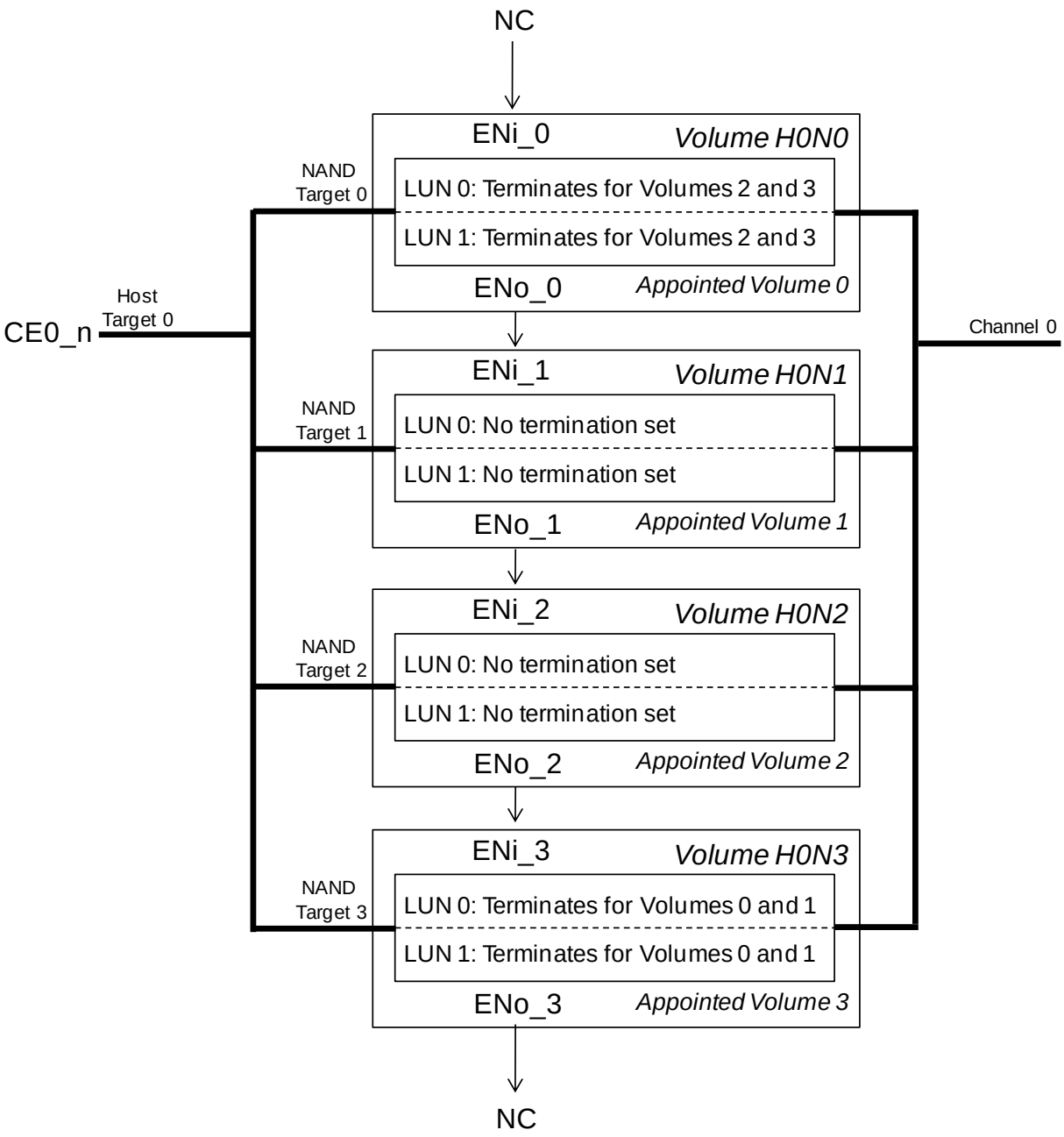


Figure 4-21 Example: Parallel Non-Target ODT

4.18. Timing Parameters

The behavior of the device when the required minimum and maximum times are not adhered to is undefined. Note that the host needs to account for channel effects in meeting the specified timings with the device.

4.18.1. General Parameters

This section describes timing parameters that apply regardless of the data interface type being used.

For execution of the first Read Parameter Page command, prior to complete initialization, a tR value of 200 microseconds and tCCS value of 500 ns shall be used. For page reads, including execution of additional Read Parameter Page commands after initialization is complete, the value for tR and tCCS is vendor specific, see the vendor component datasheet.

There are three maximums listed for tRST in the SDR, NV-DDR, NV-DDR2, NV-DDR3 and NV-LPDDR4 data interfaces. The target is allowed a longer maximum reset time when a program or erase operation is in progress. The maximums correspond to:

1. The target is performing a page read (00h-address-30h) operation. For all other operations where the target is not performing an erase, program or page read (00-address-30h) operation, refer to the vendor datasheet.
2. The target is performing a program operation.
3. The target is performing an erase operation.

Table 4-63 defines timing parameters that have common definitions across the SDR, NV-DDR, NV-DDR2, NV-DDR3 and NV-LPDDR4 interfaces.

Parameter	Description
tADL[2]	Address cycle to data loading time
tCCS[2 6]	Change Column setup time, is vendor specific, see the vendor component datasheet
tCEH	CE_n high hold time
tCH	CE_n hold time
tCS	CE_n setup time
tDH	Data hold time
tDS	Data setup time
tFEAT[1]	Busy time for Set Features and Get Features
tITC[1]	Interface and Timing Mode Change time
tRR	Ready to data output cycle (data only)
tRST	Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n.
tWB[3,4]	(WE_n high or CLK rising edge) to SR[6] low
tWHR[2]	Command, address, or data input cycle to data output cycle
tWHRT[5]	Address cycle to data output for training
tWTRN[5]	Ready-busy time during write RX training
tWW	WP_n transition to command cycle

NOTE:
1. Measured from the falling edge of SR[6] to the rising edge of SR[6].
2. tADL is used for Program operations. tWHR is used for Read ID, Read Status, and Read Status Enhanced commands. tCCS is used for commands that modify the column address and thus impact the data pipeline; these commands include Change Read Column and Change Write Column.
3. For Set Features when using NV-DDR2 or NV-DDR3, tWB starts on the rising edge of DQS for parameter P4.
4. Commands (including Read Status / Read Status Enhanced) shall not be issued until after tWB is complete.
5. tWHRT, tWTRN is used only for training commands.
6. For the NV-DDR2, NV-DDR3 and NV-LPDDR4 interfaces, during data input sequences which require tCCS, tCCS is referenced from WE# high to:
    a. The first byte (DQS_t rising edge) input when warmup cycles are disabled
    b. The first byte (DQS_t rising edge) of the first input warmup cycle when warmup cycles are enabled
7. For the NV-DDR2, NV-DDR3 and NV-LPDDR4 interfaces, during data output sequences which require tCCS, tCCS is referenced from WE# high to the RE_t falling edge marking the start of the read pre-amble (tRPRE/tRPRE2).

Table 4-63 General Timing Parameters

Table 4-64 defines the array timing parameters. The array timing parameter values are statically defined in Table 4-65. Please see vendor datasheet for these parameter timings
.

Parameter	Description
tBERS[1]	Block erase time
tCCS	Change Column setup time
tPLEBSY[1]	Busy time for multi-plane erase operation
tPLPBSY[1]	Busy time for multi-plane program operation
tPLRBSY[1]	Busy time for multi-plane read operation
tPCBSY	Program cache busy time
tPROG[1]	Page program time
tR[1]	Page read time
tRCBSY[1]	Read cache busy time

NOTE:
1. Measured from the falling edge of SR[6] to the rising edge of SR[6].
2. For the NV-DDR2, NV-DDR3 and NV-LPDDR4 interfaces, during data input sequences which require tCCS, tCCS is referenced from WE# high to:
    a. The first byte (DQS_t rising edge) input when warmup cycles are disabled
    b. The first byte (DQS_t rising edge) of the first input warmup cycle when warmup cycles are enabled
3. For the NV-DDR2, NV-DDR3 and NV-LPDDR4 interfaces, during data output sequences which require tCCS, tCCS is referenced from WE# high to the RE_t falling edge marking the start of the read pre-amble (tRPRE/tRPRE2).

Table 4-64 Array Timing Parameter Descriptions

There are “short” busy times associated with cache operations (tRCBSY, tPCBSY) and multi-plane operations (tPLEBSY, tPLPBSY, and tPLRBSY). Typical and maximum times for these busy times are listed in Table 4-65.

Parameter	Typical	Maximum
tPLEBSY	500 ns	tBERS
tPLPBSY	500 ns	tPROG
tPLRBSY	500 ns	tR
tPCBSY	3 µs	tPROG
tRCBSY	3 µs	tR

NOTE:
1. Typical times for tPCBSY and tRCBSY are the recommended interval at which the host should consider polling status. Device busy time may be longer than the typical value.

Table 4-65 Cache and Multi-plane Short Busy Times

The CE_n pin reduction mechanism may be used with any data interface. However, if VccQ = 3.3V or 1.8V, the configuration for CE_n pin reduction shall be done using the SDR data interface. If VccQ=1.2V, the configuration for CE_n pin reduction shall be done using the NV-DDR3 data interface. The timings for enumeration signals utilized in the daisy chain between packages and as part of Volume Addressing are listed in Table 4-66.

Parameter	Description	Minimum	Maximum
tVDLY	Delay prior to issuing the next command after a new Volume is selected using the Volume Select command.	50 ns	-
tCEVDLY	Delay prior to bringing CE_n high after a new Volume is selected using the Volume Select command.	50 ns	-
tENi	ENi low until any issued command is ignored (ENo driving low from previous package in daisy chain)	-	15 ns
tENo	CE_n low until ENo low	-	50 ns

Table 4-66 CE_n Pin Reduction Enumeration and Volume Addressing Times

Parameter	Description	Maximum
tZQCL	Normal operation Long calibration time	1us
tZQCS	Normal operation Short calibration time	0.4us
NOTE: Increased tZQCL and tZQCS values beyond minimum specified value may result when greater than 8 LUNs share a ZQ resistor		

Table 4-67 ZQ Calibration Timing parameters

4.18.2. SDR

Table 4-68 defines the descriptions of all timing parameters used in the SDR data interface. Table 4-72 and Table 4-73 define the requirements for timing modes 0, 1, 2, 3, 4, and 5. Timing mode 0 shall always be supported and the device operates in this mode at power-on. A host shall only begin use of a more advanced timing mode after determining that the device supports that timing mode in the parameter page.

The host shall use EDO data output cycle timings, as defined in section 4.20.1.5, when running with a tRC value less than 30 ns.

Parameter	Description
tALH	ALE hold time
tALS	ALE setup time
tAR	ALE to RE_n delay
tCEA	CE_n access time
tCHZ[1]	CE_n high to output hi-Z
tCLH	CLE hold time
tCLR	CLE to RE_n delay
tCLS	CLE setup time
tCOH	CE_n high to output hold
tCR	CE_n to RE_n low
tCR2	CE_n to RE_n low after CE_n has been high for greater than 1us
tCS3	CE_n setup time for data input after CE_n has been high for greater than 1us
tIR[1]	Output hi-Z to RE_n low
tRC	RE_n cycle time
tREA	RE_n access time
tREH	RE_n high hold time
tRHOH	RE_n high to output hold
tRHW	RE_n high to WE_n low
tRHZ[1]	RE_n high to output hi-Z
tRLOH	RE_n low to output hold
tRP	RE_n pulse width
tWC	WE_n cycle time
tWH	WE_n high hold time
tWP	WE_n pulse width
NOTE: 1. Refer to Appendix E for measurement technique.	

Table 4-68 SDR Timing Parameter Descriptions

4.18.3. NV-DDR

All NV-DDR data interface timing parameters are referenced to the rising edge of CLK or the latching edge of DQS. Note that R/B_n and WP_n are always asynchronous signals.

For parameters measured in clocks (e.g. tDSH), the parameter is measured starting from a latching edge of CLK or DQS, respectively.

Parameter	Description
tAC	Access window of DQ[7:0] from CLK
tCADf, tCADs	Command, Address, Data delay (command to command, address to address, command to address, address to command, command/address to start of data)
tCAH	Command/address DQ hold time
tCALH	W/R_n, CLE and ALE hold time
tCALS	W/R_n, CLE and ALE setup time
tCAS	Command/address DQ setup time
tCK(avg)[1]	Average clock cycle time, also known as tCK
tCK(abs)	Absolute clock period, measured from rising edge to the next consecutive rising edge
tCKH(abs) [2]	Clock cycle high
tCKL(abs) [2]	Clock cycle low
tCKWR	Data output end to W/R_n high
tCS3	CE_n setup time for data input and data output after CE_n has been high for greater than 1us
tDPZ	Data input pause setup time
tDQSCK	Access window of DQS from CLK
tDQSD[3]	W/R_n low to DQS/DQ driven by device
tDQSH	DQS input high pulse width
tDQSHZ[3]	W/R_n high to DQS/DQ tri-state by device
tDQSL	DQS input low pulse width
tDQSQ	DQS-DQ skew, DQS to last DQ valid, per access
tDQSS	Data input to first DQS latching transition
tDSC	DQS cycle time
tDSH	DQS falling edge to CLK rising – hold time
tDSS	DQS falling edge to CLK rising – setup time
tDVW	Output data valid window
tHP	Half-clock period
tJIT(per)	The deviation of a given tCK(abs) from tCK(avg)
tQH	DQ-DQS hold, DQS to first DQ to go non-valid, per access
tQHS	Data hold skew factor
tRHW	Data output cycle to command, address, or data input cycle
tWPRE	DQS write preamble
tWPST	DQS write postamble
tWRCK	W/R_n low to data output cycle

NOTE:
1. tCK(avg) is the average clock period over any consecutive 200 cycle window.
2. tCKH(abs) and tCKL(abs) include static offset and duty cycle jitter.
3. Refer to Appendix E for measurement technique.

Table 4-69 NV-DDR Timing Parameter Descriptions

4.18.4. NV-DDR2/NV-DDR3

Table 4-70 defines the timing parameters for the NV-DDR2 and NV-DDR3 data interface.

Parameter	Description
dQSQ/dT	Change in tDQSQ versus temperature for a LUN. Computed by the dividing delta in tDQSQ by the operating temperature range of the device for a LUN. Spec is guaranteed by design and characterization and not tested in production.
dQSQ/dV	Change in tDQSQ versus VccQ for a LUN. Computed by dividing the delta in tDQSQ by the operating VccQ range of the device for a LUN. Spec is guaranteed by design and characterization and not tested in production.
tAC	Access window of DQ[7:0] from RE_n (RE_t/RE_c crosspoint)
tCAH	Command/address DQ hold time
tCALH	CLE and ALE hold time
tCALS	CLE and ALE setup time during command and address cycles
tCALQS [2]	CLE and ALE setup time to DQS_t or DQS_t/DQS_c cross-point when ODT is disabled
tCALQS2 [2]	CLE and ALE setup time to DQS_t or DQS_t/DQS_c cross-point when ODT is enabled
tCALR [2]	CLE and ALE setup time to RE_n or RE_t/RE_c cross-point when ODT is disabled
tCALR2 [2]	CLE and ALE setup time to RE_n or RE_t/RE_c cross-point when ODT is enabled
tCAS	Command/address DQ setup time
tCHZ[1]	CE_n high to output Hi-Z
tCLHZ[1]	CLE high to output Hi-Z
tCLR	CLE to (RE_n low or RE_t/RE_c crosspoint)
tCR	CE_n to (RE_n low or RE_t/RE_c crosspoint)
tCR2	CE_n to (RE_n low or RE_t/RE_c crosspoint) after CE_n has been high for greater than 1us
tCS1	CE_n setup time for data burst with ODT disabled
tCS2	CE_n setup time with DQS/DQ[7:0] ODT enabled
tCD	CE_n setup time to DQS (DQS_t) low after CE_n has been high for greater than 1us
tCSD	ALE, CLE, WE_n hold time from CE_n high
tCDQSS	DQS setup time for data input start
tCDQSH	DQS hold time for data input burst end
tDBS	DQS (DQS_t) high and RE_n (RE_t) high setup to ALE, CLE and CE_n low during data burst
tDH_relaxed	Data DQ hold time relaxed timing
tDH_tight	Data DQ hold time tight timing
tDIPW	DQ input pulse width at Vcent_DQ (pin_mid) or VrefQ
tDIVW1	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) or VrefQ
tDIVW2	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) ± vDIVW_total/2
tDQ2DQ	Maximum allowable skew between DQ signals at the NAND ball for a single LUN.
tDQDQ	Worst case DQ-to-DQ variation for a LUN during data output cycles.
tDQS2DQ	Maximum allowable skew between DQS and DQ at the NAND ball for a single LUN.
tDQSD	(RE_n low or RE_t/RE_c crosspoint) to DQS/DQ driven by device
tDQSH (abs)	Absolute DQS high level width
tDQSH (avg)	Average DQS high level width
tDQSL (abs)	Absolute DQS low level width
tDQSL (avg)	Average DQS low level width
tDQSQ	DQS-DQ skew, DQS to last DQ valid, per access
tDQSRE	Access window of DQS from RE_n (RE_t/RE_c)
tDQSRH	DQS hold time after (RE_n low or RE_t/RE_c crosspoint)
tDS_relaxed	Data DQ setup time relaxed timing
tDS_tight	Data DQ setup time tight timing
tDSC(avg)	Average DQS cycle time
tDSC(abs)	Absolute write cycle period, measured from rising edge to the next consecutive rising edge
tDVWd	Output data valid window per device (across all IO pins)
tDVWp	Output data valid window per IO pin
tJITper	The deviation of a given tRC(abs)/tDSC(abs) from tRC(avg)/tDSC(avg)
tJITcc	Cycle-to-cycle jitter
tQH	DQ-DQS hold, DQS to first DQ to go non-valid, per access
tQSH	DQS output high time (if differential, DQS_t is high)
tQSL	DQS output low time (if differential, DQS_t is low)
tRC(avg)	Average read cycle time, also known as tRC
tRC(abs)	Absolute read cycle period, measured from rising edge to the next consecutive rising edge

tREH(abs)	Absolute RE_n/RE_t high level width
tREH(avg)	Average RE_n/RE_t high level width
tRHW	Data output cycle to command or address cycle (RE_t high to WE_n high)
tRP(abs)	Absolute RE_n/RE_t low level width
tRP(avg)	Average RE_n/RE_t low level width
tRPRE [2]	Read preamble
tRPRE2 [2]	Read preamble with ODT enabled
tRPST	Read postamble
tRPSTH	Read postamble hold time
tWC	Write cycle time
tWH	WE_n high pulse width
tWP	WE_n low pulse width
tWPRE [2]	DQS write preamble
tWPRE2 [2]	DQS write preamble when ODT enabled
tWPST	DQS write postamble
tWPSTH	DQS write postamble hold time

NOTE:
1. Refer to Appendix E for measurement technique.
2. Devices that support >1600MT/s may require tCALR2, tCALQS2, tRPRE2 and tWPRE2 to be met even when ODT is disabled. See Vendor Datasheet.

Table 4-70 NV-DDR2/NV-DDR3 Timing Parameter Descriptions

4.18.5. NV-LPDDR4

Table 4-71 defines the timing parameters for the NV-LPDDR4 data interface.

Parameter	Description
dQSQ/dT	Change in tDQSQ versus temperature for a LUN. Computed by the dividing delta in tDQSQ by the operating temperature range of the device for a LUN. Spec is guaranteed by design and characterization and not tested in production.
dQSQ/dV	Change in tDQSQ versus VccQ for a LUN. Computed by dividing the delta in tDQSQ by the operating VccQ range of the device for a LUN. Spec is guaranteed by design and characterization and not tested in production.
tAC	Access window of DQ[7:0] from RE_n (RE_t/RE_c crosspoint)
tCAH	Command/address DQ hold time
tCALH	CLE and ALE hold time
tCALS	CLE and ALE setup time during command and address cycles
tCALQS2	CLE and ALE setup time to DQS_t or DQS_t/DQS_c cross-point
tCALR2	CLE and ALE setup time to RE_n or RE_t/RE_c cross-point
tCAS	Command/address DQ setup time
tCHZ[1]	CE_n high to output Hi-Z
tCLHZ[1]	CLE high to output Hi-Z
tCLR	CLE to (RE_n low or RE_t/RE_c crosspoint)
tCR	CE_n to (RE_n low or RE_t/RE_c crosspoint)
tCR2	CE_n to (RE_n low or RE_t/RE_c crosspoint) after CE_n has been high for greater than 1us
tCS1	CE_n setup time for data burst with ODT disabled
tCS2	CE_n setup time with DQS/DQ[7:0] ODT enabled
tCD	CE_n setup time to DQS (DQS_t) low after CE_n has been high for greater than 1us
tCSD	ALE, CLE, WE_n hold time from CE_n high
tCDQSS	DQS setup time for data input start
tCDQSH	DQS hold time for data input burst end
tDBS	DQS (DQS_t) high and RE_n (RE_t) high setup to ALE, CLE and CE_n low during data burst
tDH_relaxed	Data DQ hold time relaxed timing
tDH_tight	Data DQ hold time tight timing
tDIPW	DQ input pulse width at Vcent_DQ (pin_mid) or VrefQ
tDIVW1	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid)
tDIVW2	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) ± vDIVW_total/2
tDQ2DQ	Maximum allowable skew between DQ signals at the NAND ball for a single LUN.
tDQDQ	Worst case DQ-to-DQ variation for a LUN during data output cycles.
tDQS2DQ	Maximum allowable skew between DQS and DQ at the NAND ball for a single LUN.
tDQSD	(RE_n low or RE_t/RE_c crosspoint) to DQS/DQ driven by device
tDQSH (abs)	Absolute DQS high level width
tDQSH (avg)	Average DQS high level width
tDQSL (abs)	Absolute DQS low level width
tDQSL (avg)	Average DQS low level width
tDQSQ	DQS-DQ skew, DQS to last DQ valid, per access
tDQSRE	Access window of DQS from RE_n (RE_t/RE_c)
tDQSRH	DQS hold time after (RE_n low or RE_t/RE_c crosspoint)
tDS_relaxed	Data DQ setup time relaxed timing
tDS_tight	Data DQ setup time tight timing
tDSC(avg)	Average DQS cycle time
tDSC(abs)	Absolute write cycle period, measured from rising edge to the next consecutive rising edge
tDVWd	Output data valid window per device (across all IO pins)
tDVWp	Output data valid window per IO pin
tJITper	The deviation of a given tRC(abs)/tDSC(abs) from tRC(avg)/tDSC(avg)
tJITcc	Cycle-to-cycle jitter
tODTOFF	ODT Disable command to next command timing
tODTON	ODT Enable command to next command timing
tQH	DQ-DQS hold, DQS to first DQ to go non-valid, per access
tQSH	DQS output high time (if differential, DQS_t is high)
tQSL	DQS output low time (if differential, DQS_t is low)
tRC(avg)	Average read cycle time, also known as tRC
tRC(abs)	Absolute read cycle period, measured from rising edge to the next consecutive rising edge
tREH(abs)	Absolute RE_n/RE_t high level width
tREH(avg)	Average RE_n/RE_t high level width
tRHW	Data output cycle to command or address cycle (RE_t high to WE_n high)
tRP(abs)	Absolute RE_n/RE_t low level width

tRP(avg)	Average RE_n/RE_t low level width
tRPRE2	Read preamble
tRPST	Read postamble
tRPSTH	Read postamble hold time
tWC	Write cycle time
tWH	WE_n high pulse width
tWP	WE_n low pulse width
tWPRE2	DQS write preamble
tWPST	DQS write postamble
tWPSTH	DQS write postamble hold time
NOTE: 1. Refer to Appendix E for measurement technique.	

Table 4-71 NV-LPDDR4 Timing Parameter Descriptions

4.18.6. NV-DDR3/NV-LPDDR4 DQ Rx Mask Specification

The DQ input receiver (Rx) mask defines the area that the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal. The mask is a receiver property and is not the valid data-eye. The DQ Rx mask for voltage and timing is shown in the Figure 4-22 below and is applied per individual DQ pin. The DQ Rx mask is evaluated at the die pads.

The minimum DQ AC input pulse amplitude (pk-pk) is given by the VIHL_AC specification. The DQ only input pulse amplitude must meet or exceed VIHL_AC at least one time over the total UI, except when no transitions are occurring for that UI. VIHL_AC is centered around Vcent_DQ (pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ (pin_mid). For NV-DDR3 interface, Vcent_DQ (pin_mid) is replaced by VrefQ as the center reference level in the case where External VrefQ is used or Internal VrefQ when Vref training is used. There are no timing requirements above or below VIHL_AC levels.

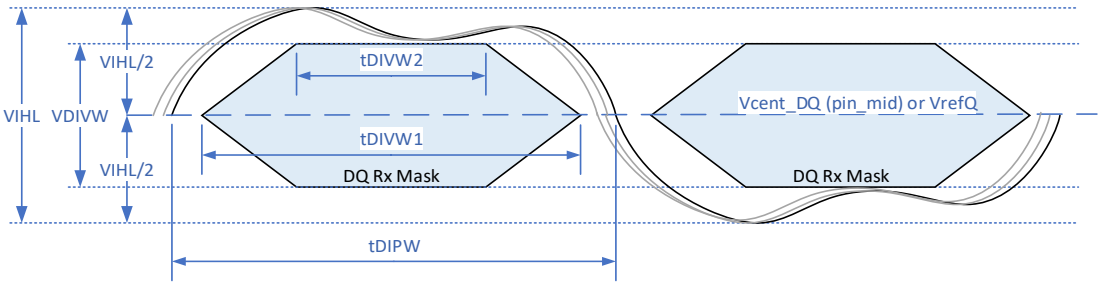


Figure 4-22 NV-DDR3/NV-LPDDR4 DQ Rx Mask and VIHL Definition

Vcent_DQ (pin_mid) is defined as the midpoint between the highest Vcent_DQ voltage level and the lowest Vcent_DQ voltage level across all DQ pins for a given NAND die.
Each Vcent_DQ is defined by the center (ie. widest opening) of the cumulative data input eye as depicted in the figure below.

Since the DQ Rx mask is centered around Vcent_DQ (pin_mid), any pin-to-pin Vcent_DQ variation must be accounted for in the DQ Rx Mask.

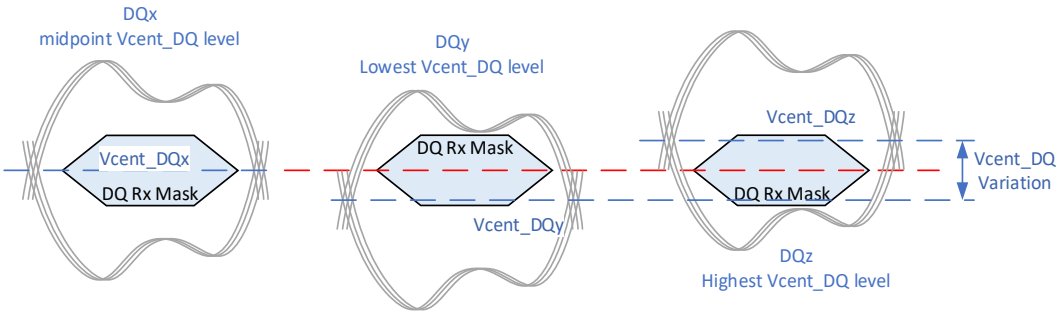


Figure 4-23 NV-DDR3/NV-LPDDR4 Vcent_DQ (pin_mid) Definition

4.19. Timing Modes

4.19.1. SDR

Parameter	Mode 0		Mode 1		Mode 2		Unit
	100		50		35		ns
	Min	Max	Min	Max	Min	Max	
tADL	400	—	400	—	400	—	ns
tALH	20	—	10	—	10	—	ns
tALS	50	—	25	—	15	—	ns
tAR	25	—	10	—	10	—	ns
tCEA	—	100	—	45	—	30	ns
tCEH	20	—	20	—	20	—	ns
tCH	20	—	10	—	10	—	ns
tCHZ	—	100	—	50	—	50	ns
tCLH	20	—	10	—	10	—	ns
tCLR	20	—	10	—	10	—	ns
tCLS	50	—	25	—	15	—	ns
tCOH	0	—	15	—	15	—	ns
tCR	10	—	10	—	10	—	ns
tCR2	100	—	100	—	100	—	ns
tCR2 (Read ID) [2]	150	—	150	—	150	—	ns
tCS3	100	—	100	—	100	—	ns
tCS	70	—	35	—	25	—	ns
tDH	20	—	10	—	5	—	ns
tDS	40	—	20	—	15	—	ns
tFEAT	—	1	—	1	—	1	µs
tIR	10	—	0	—	0	—	ns
tITC	—	1	—	1	—	1	µs
tRC	100	—	50	—	35	—	ns
tREA	—	40	—	30	—	25	ns
tREH	30	—	15	—	15	—	ns
tRHOH	0	—	15	—	15	—	ns
tRHW	200	—	100	—	100	—	ns
tRHZ	—	200	—	100	—	100	ns
tRLOH	0	—	0	—	0	—	ns
tRP	50	—	25	—	17	—	ns
tRR	40	—	20	—	20	—	ns
tRST	—	5000	—	15/30/ 500	—	15/30/ 500	µs
tWB	—	200	—	100	—	100	ns
tWC	100	—	45	—	35	—	ns
tWH	30	—	15	—	15	—	ns
tWHR	120	—	80	—	80	—	ns
tWP	50	—	25	—	17	—	ns
tWW	100	—	100	—	100	—	ns

NOTE:
1. To easily support EDO capable devices, tCHZ and tRHZ maximums are higher in modes 1, 2, and 3 than typically necessary for a non-EDO capable device.
2. tCR2(min) is 150ns for Read ID sequence only. For all other command sequences tCR2(min) requirement is 100ns.

Table 4-72 SDR Timing Modes 0, 1, and 2

Parameter	Mode 3		Mode 4 (EDO capable)		Mode 5 (EDO capable)		Unit
	30		25		20		ns
	Min	Max	Min	Max	Min	Max	
tADL	400	—	400	—	400	—	ns
tALH	5	—	5	—	5	—	ns
tALS	10	—	10	—	10	—	ns
tAR	10	—	10	—	10	—	ns
tCEA	—	25	—	25	—	25	ns
tCEH	20	—	20	—	20	—	ns
tCH	5	—	5	—	5	—	ns
tCHZ	—	50	—	30	—	30	ns
tCLH	5	—	5	—	5	—	ns
tCLR	10	—	10	—	10	—	ns
tCLS	10	—	10	—	10	—	ns
tCOH	15	—	15	—	15	—	ns
tCR	10	—	10	—	10	—	ns
tCR2	100	—	100	—	100	—	ns
tCR2 (Read ID) [2]	150	—	150	—	150	—	ns
tCS3	100	—	100	—	100	—	ns
tCS	25	—	20	—	15	—	ns
tDH	5	—	5	—	5	—	ns
tDS	10	—	10	—	7	—	ns
tFEAT	—	1	—	1	—	1	µs
tIR	0	—	0	—	0	—	ns
tITC	—	1	—	1	—	1	µs
tRC	30	—	25	—	20	—	ns
tREA	—	20	—	20	—	16	ns
tREH	10	—	10	—	7	—	ns
tRHOH	15	—	15	—	15	—	ns
tRHW	100	—	100	—	100	—	ns
tRHZ	—	100	—	100	—	100	ns
tRLOH	0	—	5	—	5	—	ns
tRP	15	—	12	—	10	—	ns
tRR	20	—	20	—	20	—	ns
tRST	—	10/30/500	—	15/30/500	—	15/30/500	µs
tWB	—	100	—	100	—	100	ns
tWC	30	—	25	—	20	—	ns
tWH	10	—	10	—	7	—	ns
tWHR	80	—	80	—	80	—	ns
tWP	15	—	12	—	10	—	ns
tWW	100	—	100	—	100	—	ns

NOTE:
1. To easily support EDO capable devices, tCHZ and tRHZ maximums are higher in modes 1, 2, and 3 than typically necessary for a non-EDO capable device.
2. tCR2(min) is 150ns for Read ID sequence only. For all other command sequences tCR2(min) requirement is 100ns.

Table 4-73 SDR Timing Modes 3, 4, and 5

4.19.2. NV-DDR

Table 4-74 describes the standard NV-DDR data interface timing modes. The host is not required to have a clock period that exactly matches any of the clock periods listed for the standard timing modes. The host shall meet the setup and hold times for the timing mode selected. If the host selects timing mode *n* using Set Features, then its clock period shall be faster than the clock period of timing mode *n-1* and slower than or equal to the clock period of timing mode **n**. For example, if the host selects timing mode 2, then the following equation shall hold:

30 ns > host clock period ≥ 20 ns

Timing parameters that indicate a latency requirement before a data input, data output, address, or command cycle shall be satisfied to the rising clock edge after the latency in nanoseconds has elapsed. To calculate the first edge where the associated transition may be made, it is calculated as follows:

= RoundUp{[tParam + tCK] / tCK}

The timing modes shall meet the testing conditions defined in Table 4-9.

Parameter	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit
	50		30		20		15		12		10		ns
	20		~33		50		~66		~83		100		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tAC	3	25	3	25	3	25	3	25	3	25	3	25	ns
tADL	400	—	400	—	400	—	400	—	400	—	400	—	ns
tCADf	25	—	25	—	25	—	25	—	25	—	25	—	ns
tCADs	45	—	45	—	45	—	45	—	45	—	45	—	ns
tCAH	10	—	5	—	4	—	3	—	2.5	—	2	—	ns
tCALH	10	—	5	—	4	—	3	—	2.5	—	2	—	ns
tCALS	10	—	5	—	4	—	3	—	2.5	—	2	—	ns
tCAS	10	—	5	—	4	—	3	—	2.5	—	2	—	ns
tCEH	20	—	20	—	20	—	20	—	20	—	20	—	ns
tCH	10	—	5	—	4	—	3	—	2.5	—	2	—	ns
tCK(avg) or tCK	50	—	30	—	20	—	15	—	12	—	10	—	ns
tCK(abs)	Minimum: tCK(avg) + tJIT(per) min Maximum: tCK(avg) + tJIT(per) max												ns
tCKH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK
tCKL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK
tCKWR	Minimum: RoundUp{[tDQSCK(max) + tCK] / tCK} Maximum: —												tCK
tCS3	75	—	75	—	75	—	75	—	75	—	75	—	ns
tCS	35	—	25	—	15	—	15	—	15	—	15	—	ns
tDH	5	—	2.5	—	1.7	—	1.3	—	1.1	—	0.9	—	ns
tDPZ	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	tDSC
tDQSCK	3	25	3	25	3	25	3	25	3	25	3	25	ns
tDQSD	0	18	0	18	0	18	0	18	0	18	0	18	ns
tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK or tDSC[4]
tDQSHZ	—	20	—	20	—	20	—	20	—	20	—	20	ns
tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK or tDSC[4]
tDQSQ	—	5	—	2.5	—	1.7	—	1.3	—	1.0	—	0.85	ns
tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK
tDS	5	—	3	—	2	—	1.5	—	1.1	—	0.9	—	ns
tDSC	50	—	30	—	20	—	15	—	12	—	10	—	ns
tDSH	0.2	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	—	tCK

tDSS	0.2	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	—	tCK
tDVW	tDVW = tQH – tDQSQ												ns
tFEAT	—	1	—	1	—	1	—	1	—	1	—	1	µs
tHP	tHP = min(tCKL, tCKH)												ns
tITC	—	1	—	1	—	1	—	1	—	1	—	1	µs
tJIT(per)	-0.7	0.7	-0.7	0.7	-0.7	0.7	-0.6	0.6	-0.6	0.6	-0.5	0.5	ns
tQH	tQH = tHP – tQHS												ns
tQHS	—	6	—	3	—	2	—	1.5	—	1.2	—	1.0	ns
tRHW	100	—	100	—	100	—	100	—	100	—	100	—	ns
tRR	20	—	20	—	20	—	20	—	20	—	20	—	ns
tRST	—	15/30/ 500	—	15/30/ 500	—	15/30/ 500	—	15/30/ 500	—	15/30/ 500	—	15/30/ 500	µs
tWB	—	100	—	100	—	100	—	100	—	100	—	100	ns
tWHR	80	—	80	—	80	—	80	—	80	—	80	—	ns
tWPRE	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	tCK
tWPST	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	tCK
tWRCK	20	—	20	—	20	—	20	—	20	—	20	—	ns
tWW	100	—	100	—	100	—	100	—	100	—	100	—	ns

NOTE:
1. tDQSHZ is not referenced to a specific voltage level, but specifies when the device output is no longer driving.
2. tCK(avg) is the average clock period over any consecutive 200 cycle window.
3. tCKH(abs) and tCKL(abs) include static offset and duty cycle jitter.
4. tDQSL and tDQSH are relative to tCK when CLK is running. If CLK is stopped during data input, then tDQSL and tDQSH are relative to tDSC.

Table 4-74 NV-DDR Timing Modes

4.19.3. NV-DDR2/NV-DDR3

Table 4-75, Table 4-76, Table 4-77, Table 4-78, Table 4-79 define the standard NV-DDR2 and NV-DDR3 data interface timing modes. The host is not required to have a period that exactly matches the tDSC or tRC values listed for the standard timing modes. The host shall meet the setup and hold times for the timing mode selected. If the host selects timing mode *n* using Set Features, then its tDSC and tRC values shall be faster than the tDSC and tRC values of timing mode *n-1* and slower than or equal to the tDSC and tRC values of timing mode *n*.

The timing modes shall meet the testing conditions defined in Table 4-9. For speeds faster than 200 MT/s, the timing parameters are verified using the 35 Ohm or 37.5 Ohm drive strength, differential signaling for both RE_n (RE_t/RE_c) and DQS (DQS_t/DQS_c) signals, and external VREFQ. For speeds faster than 533 MT/s, the timing parameters are verified with ZQ calibration performed. For speeds faster than 200 MT/s, implementations may use alternate drive strength settings, single-ended signaling, and/or internal VREFQ; verification of timing parameters in these cases is left to the implementer.

Based on the wide range of NAND applications and associated topologies NAND devices can support different tDS and tDH values and still achieve the same data input frequency. To support the diverse usage of NAND devices the NV-DDR2 and NV-DDR3 interfaces support two tDS and tDH values for each of the timing modes 4-12. These are specified as tDS_tight, tDH_tight, tDS_relaxed and tDH_relaxed shown in Table 4-77 .

For data rates >800 MT/s, the tDS+tDH (with training) spec was added. The tDS+tDH (with training) spec is the width of the keep out area for each DQ pin at the NAND ball. The tDS+tDH (with training) spec defines the area that the input signal must not encroach for the NAND input receiver to successfully capture a valid input signal. The tDS+tDH (with training) spec shall only be utilized by systems with controllers capable of per-DQ timing adjustment capability against DQS during Write Training Tx or Write Training Rx. For data rates >1600MT/s, the tDS+tDH (with training) spec no longer applies and the DQ Rx mask requirements outlined in the 4.18.6 NV-DDR3/NV-LPDDR4 DQ Rx Mask Specification section apply.

The following requirements apply to the timing parameter values:

1. tCHZ and tCLHZ are not referenced to a specific voltage level but specify when the device output is no longer driving.
2. The parameters tRC(avg) and tDSC(avg) are the average over any 200 consecutive periods and tRC(avg)/tDSC(avg) min are the smallest rates allowed, with the exception of a deviation due to tJITper.
3. Input jitter is allowed provided it does not exceed values specified.
4. tREH(avg) and RP(avg) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter, Input clock jitter is allowed provided it does not exceed values specified.
5. The period jitter (tJITper) is the maximum deviation in the tRC or tDSC period from the average or nominal tRC or tDSC over any 200 consecutive periods. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter (tJITcc) is the amount the clock period can deviate from one cycle to the next.
7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed tJITper. As long as the absolute minimum half period tRP(abs), tREH(abs), tDQSH or tDQSL is not less than 43 percent of the average cycle (tRP(abs) and tREH(abs) not less than 45 percent of the average cycle for ≥800 MTs with no training).
8. When the device is operated with input RE_n (RE_t/RE_c) jitter, tQSL, tQSH, and tQH need to be derated by the actual input duty cycle jitter beyond 0.45 * tRC(avg) but not exceeding 0.43 * tRC(avg) for less than 800 MT/s operation. Output deratings are relative to the device input RE_n pulse that generated the DQS pulse. For operation above 800 MT/s, even with input RE jitter, tREH(abs) and tRP(abs) should not go lower than 0.43 * tRC(avg).”

9. Minimizing the amount of duty cycle jitter to more than 45% of the average cycle provides a larger tQH, which in turn provides a larger data valid window. The device shall provide a minimum of 0.5% of larger data valid window for each 1% improvement in duty cycle jitter. For example, if the host provides a tREH(abs) of 0.49 * tRC(avg) then the device shall provide at least a tQH of 0.39 * tRC(avg).
10. For data rates where the DQ Rx Mask is not applicable (ie. ≤ 1600MT/s), the tDS and tDH times or tDS+tDH times listed are based on an input slew rate of 1 V/ns. If the input slew rate is not 1 V/ns, then the derating methodology shall be used for data rates ≤1200MT/s. The tDS+tDH (with training) spec shall only be utilized by systems that employ per-DQ timing adjustment capability against DQS during Write Training Tx or Write Training Rx. For data rates where DQ Rx Mask is applicable (>1600MT/s), the input slew rate must not fall below the minimum slew rate as specified in the Table 4-44 NV-DDR2/3 Maximum and Minimum Input Slew Rate and no derating is applied.
11. The parameter tDIPW is defined as the pulse width of the input signal between the first crossing of VREFQ(DC) and the consecutive crossing of VREFQ(DC).
12. For data rates up to 1200MT/s, parameters tDQSQ and tQH are used to calculate overall tDVWd (tDVWd = tQH - tDQSQ). tDVWd is the data valid window per device per UI and is derived from [tQH – tDQSQ] of each UI on a pin per device. Since data eye training to optimize strobe placement is expected at high I/O speeds (≥533 MT/s), tDQSQ and tQH may borrow time from each other without changing tDVWd. For example, if there exists X ps of margin on tDQSQ then tQH can be provided with an additional X ps without changing the value of tDVWd. When timing margin is borrowed from tDQSQ to provide additional timing for tQH, the same amount of timing margin can be used for additional timing for tQSL/tQSH. For data rates >1200MT/s, the tDVWp spec shall be used instead for the NAND output valid window. NAND devices may require that DCC training be done to be able to meet tDVWp (per pin valid window) requirements for >800 MT/s data rates. In order for a system to take advantage of the wider tDVWp (per pin valid window) data-eye opening versus tDVWd (overall valid window), the system must employ the ability to de-skew each individual DQ pin against DQS with Read DQ Training.
13. For greater than 800MTs, warmup cycle(s) are required for both data input and output.
14. Both tDQS2DQ and tDQ2DQ are parameters used only when Write DQ training is supported. TDQS2DQ is the maximum allowable skew between DQS and DQ at the NAND package ball, while TDQ2DQ is the maximum allowable skew between DQ signals on a single LUN at the NAND package ball. The controller should be capable of compensating for the maximum amount of TDQS2DQ and TDQ2DQ skew during write training. The optional Write Training (RX side) mode though is not required to compensate for the maximum TDQS2DQ and TDQ2DQ amount of skew. Even with tDQS2DQ and tDQ2DQ, tDIPW still needs to be met.

Constant Timing Parameter Values			
	Min	Max	Unit
tADL	400	—	ns
tAR	10	—	ns
tCAH	5	—	ns
tCAS	5	—	ns
tCALH	5	—	ns
tCALS	15	—	ns
tCEH	20	—	ns
tCH	5	—	ns
tCS	20	—	ns
tCS1	30	—	ns
tCS2	40	—	ns
tCSD	10	—	ns
tCHZ	—	30	ns
tCLHZ	—	30	ns
tCLR	10	—	ns
tCR	10	—	ns
tCR2	100	—	ns
tCR2 (Read ID) [1]	150	—	ns
tDBS	5	—	ns
tRHW	100	—	ns
tWC	25	—	ns
tWH	11	—	ns
tWP	11	—	ns
tWHR	80	—	ns
tWHRT	400	—	ns
tWTRN	—	200	µs
tWW	100	—	ns
tFEAT	—	1	µs
tITC	—	1	µs
tRST	—	18/30/500	µs
tRR	20	—	ns
tWB	—	100	ns

NOTE:
1. tCR2(min) is 150ns for Read ID sequence only. For all other command sequences tCR2(min) requirement is 100ns.

Table 4-75 NV-DDR2 / NV-DDR3 Timing Parameter Values: Command and Address

Timing Mode Specific Values (Modes 0-3)									
	Mode 0		Mode 1		Mode 2		Mode 3		Unit
	30		25		15		12		ns
	~ 33		40		~ 66		~ 83		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper (DQS)	-2.4	2.4	-2.0	2.0	-1.2	1.2	-1.0	1.0	ns
tJITper (RE_n)	-1.8	1.8	-1.5	1.5	-0.9	0.9	-0.75	0.75	ns
tJITcc (DQS)	—	4.8	—	4.0	—	2.4	—	2.0	ns
tJITcc (RE_n)	—	3.6	—	3.0	—	1.8	—	1.5	ns
Timing Mode Specific Values (Modes 4-7)									
	Mode 4		**Mode 5**		**Mode 6**		**Mode 7**		**Unit**
	10		7.5		6		5		ns
	100		~133		~166		200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper(DQS)	-0.80	0.80	-0.60	0.60	-0.48	0.48	-0.40	0.40	ns
tJITper(RE_n)	-0.60	0.60	-0.45	0.45	-0.36	0.36	-0.30	0.30	ns
tJITcc(DQS)	—	1.6	—	1.2	—	0.96	—	0.8	ns
tJITcc(RE_n)	—	1.2	—	0.9	—	0.72	—	0.6	ns
Timing Mode Specific Values (Modes 8-11)									
	Mode 8		**Mode 9**		**Mode 10**		**Mode 11**		**Unit**
	3.75		3		2.5		1.875		ns
	~267		~333		400		~533		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper(DQS)	-0.30	0.30	-0.24	0.24	-0.2	0.2	-0.094	0.094	ns
tJITper(RE_n)	-0.225	0.225	-0.18	0.18	-0.15	0.15	-0.094	0.094	ns
tJITcc(DQS)	—	0.6	—	0.48	—	0.4	—	0.188	ns
tJITcc(RE_n)	—	0.45	—	0.36	—	0.3	—	0.188	ns
Timing Mode Specific Values (Mode 12-15)									
	Mode 12		**Mode 13**		**Mode 14**		**Mode 15**		**Unit**
	1.667		1.5		1.364		1.25		ns
	600		~667		~733		800		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper(DQS)	-0.083	0.083	-0.078	0.078	-0.075	0.075	-0.070	0.070	ns
tJITper(RE_n)	-0.083	0.083	-0.078	0.078	-0.075	0.075	-0.070	0.070	ns
tJITcc(DQS)	—	0.167	—	0.156	—	0.150	—	0.140	ns
tJITcc(RE_n)	—	0.167	—	0.156	—	0.150	—	0.140	ns
Timing Mode Specific Values (Mode 16-19)									
	Mode 16		**Mode 17**		**Mode 18**		**Mode 19**		**Unit**
	1.111		1		0.909		0.833		ns
	900		1000		1100		1200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper(DQS)	-0.062	0.062	-0.056	0.056	-0.051	0.051	-0.047	0.047	ns
tJITper(RE_n)	-0.062	0.062	-0.056	0.056	-0.051	0.051	-0.047	0.047	ns
tJITcc(DQS)	—	0.124	—	0.112	—	0.102	—	0.094	ns
tJITcc(RE_n)	—	0.124	—	0.112	—	0.102	—	0.094	ns
Timing Mode Specific Values (Mode 20-22)									
	Mode 20		**Mode 21**		**Mode 22**				**Unit**
	0.714		0.625		0.555				ns
	1400		1600		1800				MHz
	Min	Max	Min	Max	Min	Max			
tJITper(DQS)	-0.032	0.032	-0.028	0.028	-0.025	0.025			ns
tJITper(RE_n)	-0.032	0.032	-0.028	0.028	-0.025	0.025			ns
tJITcc(DQS)	—	0.064	—	0.056	—	0.050			ns
tJITcc(RE_n)	—	0.064	—	0.056	—	0.050			ns

Table 4-76 NV-DDR2 / NV-DDR3 Timing Parameter Values: Jitter

Constant Timing Parameter Values									
	Min				Max				Unit
tCALQS	15				—				ns
tCALQS2	25				—				ns
tCDQSS	30				—				ns
tCDQSH	100				—				ns
tCD	100				—				ns
tDSC(abs)	tDSC(avg) + tJITper(DQS) min				tDSC(avg) + tJITper(DQS) max				ns
tWPRE2	25				—				ns
tWPST	6.5				—				ns
tWPSTH	25				—				ns
Timing Mode Specific Values (Modes 0-3)									
	Mode 0		**Mode 1**		**Mode 2**		**Mode 3**		**Unit**
	30		25		15		12		ns
	~ 33		40		~ 66		~ 83		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDH (no training)	4	—	3.3	—	2.0	—	1.1	—	ns
tDS (no training)	4	—	3.3	—	2.0	—	1.1	—	ns
tDIPW	0.31	—	0.31	—	0.31	—	0.31	—	tDSC(avg)
tDQS2DQ (training)	NA	NA	NA	NA	NA	NA	NA	NA	ns
tDQ2DQ (training)	—	NA	—	NA	—	NA	—	NA	ns
tDQSH (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSL (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSH (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDQSL (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDSC(avg) or tDSC	30	—	25	—	15	—	12	—	ns
Timing Mode Specific Values (Modes 4-7)									
	Mode 4		**Mode 5**		**Mode 6**		**Mode 7**		**Unit**
	10		7.5		6		5		ns
	100		~133		~166		200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDH_tight (no training)	0.7	—	0.5	—	0.4	—	0.35	—	ns
tDS_tight (no training)	0.7	—	0.5	—	0.4	—	0.35	—	ns
tDH_relaxed	0.9	—	0.75	—	0.55	—	0.40	—	ns
tDS_relaxed	0.9	—	0.75	—	0.55	—	0.40	—	ns
tDS+tDH (with training)	NA	—	NA	—	NA	—	NA	—	ns
tDIPW	0.31	—	0.31	—	0.31	—	0.31	—	tDSC (avg)
tDQS2DQ (training)	NA	NA	NA	NA	NA	NA	NA	NA	ns
tDQ2DQ (training)	—	NA	—	NA	—	NA	—	NA	ns
tDQSH (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSL (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSH (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDQSL (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDSC(avg) or tDSC	10	—	7.5	—	6	—	5	—	ns
Timing Mode Specific Values (Modes 8-11)									
	Mode 8		**Mode 9**		**Mode 10**		**Mode 11**		**Unit**
	3.75		3		2.5		1.875		ns
	~267		~333		400		~533		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDH_tight (no training)	0.3	—	0.24	—	0.2	—	0.190	—	ns
tDS_tight (no training)	0.3	—	0.24	—	0.2	—	0.190	—	ns
tDH_relaxed (no training)	0.35	—	0.31	—	0.26	—	0.25	—	ns
tDS_relaxed (no training)	0.35	—	0.31	—	0.26	—	0.25	—	ns
tDS+tDH (with training)	NA	—	NA	—	NA	—	0.300	—	ns
tDIPW	0.31	—	0.31	—	0.31	—	0.33	—	tDSC(avg)
tDQS2DQ (training)	NA	NA	NA	NA	NA	NA	-0.200	0.200	ns
tDQ2DQ (training)	—	NA	—	NA	—	NA	—	0.100	ns

tDQSH (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSL (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSH (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDQSL (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDSC(avg) or tDSC	3.75	—	3	—	2.5	—	1.875	—	ns
Timing Mode Specific Values (Mode 12-15)									
	Mode 12		**Mode 13**		**Mode 14**		**Mode 15**		**Unit**
	1.667		1.5		1.364		1.25		ns
	600		~667		~733		800		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDH_tight (no training)	0.175	—	—	—	—	—	—	—	ns
tDS_tight (no training)	0.175	—	—	—	—	—	—	—	ns
tDH_relaxed (no training)	0.23	—	—	—	—	—	—	—	ns
tDS_relaxed (no training)	0.23	—	—	—	—	—	—	—	ns
tDS+tDH (with training)	0.266	—	0.266	—	0.266	—	0.266	—	ns
tDIPW	0.33	—	0.33	—	0.33	—	0.33	—	tDSC(avg)
tDQS2DQ (training)	-0.200	0.200	-0.200	0.200	-0.200	0.200	-0.200	0.200	ns
tDQ2DQ (training)	—	0.100	—	0.100	—	0.100	—	0.100	ns
tDQSH (abs)	0.45	—	0.448	—	0.445	—	0.444	—	tDSC(avg)
tDQSL (abs)	0.45	—	0.448	—	0.445	—	0.444	—	tDSC(avg)
tDQSH (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDQSL (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDSC(avg) or tDSC	1.667	—	1.5	—	1.364	—	1.25	—	ns
Timing Mode Specific Values (Mode 16-19)									
	Mode 16		**Mode 17**		**Mode 18**		**Mode 19**		**Unit**
	1.111		1		0.909		0.833		ns
	900		1000		1100		1200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDH_tight (no training)	—	—	—	—	—	—	—	—	ns
tDS_tight (no training)	—	—	—	—	—	—	—	—	ns
tDH_relaxed (no training)	—	—	—	—	—	—	—	—	ns
tDS_relaxed (no training)	—	—	—	—	—	—	—	—	ns
tDS+tDH (with training)	—	—	—	—	—	—	—	—	ns
tDIVW1	—	0.48	—	0.48	—	0.48	—	0.48	UI
tDIVW2	—	0.30	—	0.30	—	0.30	—	0.30	UI
tDIPW	0.33	—	0.33	—	0.33	—	0.33	—	tDSC(avg)
tDQS2DQ (training)	-0.200	0.200	-0.200	0.200	-0.200	0.200	-0.200	0.200	ns
tDQ2DQ (training)	—	0.100	—	0.100	—	0.100	—	0.100	ns
tDQSH (abs)	0.444	—	0.444	—	0.444	—	0.444	—	tDSC(avg)
tDQSL (abs)	0.444	—	0.444	—	0.444	—	0.444	—	tDSC(avg)
tDQSH (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDQSL (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDSC(avg) or tDSC	1.111	—	1	—	0.909	—	0.833	—	ns
Timing Mode Specific Values (Mode 20-22)									
	Mode 20		**Mode 21**		**Mode 22**				**Unit**
	0.714		0.625		0.555				ns
	1400		1600		1800				MHz
	Min	Max	Min	Max	Min	Max			
tDH_tight (no training)	—	—	—	—	—	—			ns
tDS_tight (no training)	—	—	—	—	—	—			ns
tDH_relaxed (no training)	—	—	—	—	—	—			ns
tDS_relaxed (no training)	—	—	—	—	—	—			ns
tDS+tDH (with training)	—	—	—	—	—	—			ns
tDIVW1	—	0.48	—	0.48	—	0.48			UI
tDIVW2	—	0.30	—	0.30	—	0.30			UI
tDIPW	0.33	—	0.33	—	0.33	—			tDSC(avg)
tDQS2DQ (training)	-0.200	0.200	-0.200	0.200	-0.200	0.200			ns
tDQ2DQ (training)	—	0.100	—	0.100	—	0.100			ns

tDQSH (abs)	0.455	0.545	0.455	0.545	0.455	0.545			tDSC(avg)
tDQSL (abs)	0.455	0.545	0.455	0.545	0.455	0.545			tDSC(avg)
tDQSH (avg)	0.475	0.525	0.475	0.525	0.475	0.525			tDSC(avg)
tDQSL (avg)	0.475	0.525	0.475	0.525	0.475	0.525			tDSC(avg)
tDSC(avg) or tDSC	0.714	—	0.625	—	0.555	—			ns
NOTE: 1. Unit Interval (UI) is 0.5*tDSC(avg).									

Table 4-77 NV-DDR2 / NV-DDR3 Timing Parameter Values: Data Input

The Controller DQ RX Mask specifications in the Table 4-76 below are applicable to controllers that support the data rates listed in the tables below for NV-DDR3 mode. These specifications do not apply to NAND component

Timing Mode Specific Values (Mode 16-19)									
	Mode 16		**Mode 17**		**Mode 18**		**Mode 19**		**Unit**
	1.111		1		0.909		0.833		ns
	900		1000		1100		1200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDIVW1	—	0.40	—	0.40	—	0.40	—	0.40	UI
tDIVW2	—	0.25	—	0.25	—	0.25	—	0.25	UI
tDIPW	0.25	—	0.25	—	0.25	—	0.25	—	tDSC(avg)
Timing Mode Specific Values (Mode 20-22)									
	Mode 20		**Mode 21**		**Mode 22**				**Unit**
	0.714		0.625		0.555				ns
	1400		1600		1800				MHz
	Min	Max	Min	Max	Min	Max			
tDIVW1	—	0.40	—	0.40	—	0.40			UI
tDIVW2	—	0.25	—	0.25	—	0.25			UI
tDIPW	0.25	—	0.25	—	0.25	—			tDSC(avg)

NOTE:

1. Unit Interval (UI) is 0.5*tDSC(avg).
2. Vcent_DQ (pin_mid) shall be replaced by VrefQ in the case where External VrefQ is used or Internal VrefQ without Vref training is used.
3. At 1600Mbps, use of Rx mask specifications is optional, see vendor datasheet whether Rx mask specifications are supported by the device at that data rate.
4. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment

Table 4-78 Controller NV-DDR3 Timing Parameter Values: Data Input

	Min				Max				Unit
dQSQ/dT	-0.5				0.5				ps/ºC
dQSQ/dV	-0.35				0.35				ps/mv
tDQSD	5				18				ns
tCALR	15				—				ns
tCALR2	25				—				ns
tDVWd (device)	tDVWd = tQH – tDQSQ (TM0-TM12)								ns
tQH	0.37 (TM0-TM12)				—				tRC(avg)
tQSH	0.37				—				tRC(avg)
tQSL	0.37				—				tRC(avg)
tRC(abs)	tRC(avg) + tJITper(RE_n) min				tRC(avg) + tJITper(RE_n) max				ns
tRPRE2	25				—				ns
tRPST	tDQSRE + 0.5*tRC				—				ns
tRPSTH	15				—				ns
tDQSRH	3				5				ns
Timing Mode Specific Values (Modes 0-3)									
	Mode 0		**Mode 1**		**Mode 2**		**Mode 3**		**Unit**
	30		25		15		12		ns
	~ 33		40		~ 66		~ 83		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	—	2.5	—	2.0	—	1.4	—	1.0	ns
tDQDQ	—	—	—	—	—	—	—	—	ns
tRC(avg) or tRC	30	—	25	—	15	—	12	—	ns
tREH/tRP(abs) (no training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH/tRP(avg) (no training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tREH(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tRP(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tRP(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tDVWp (per pin)	NA	—	NA	—	NA	—	NA	—	ns
tAC	2	25	2	25	2	25	2	25	ns
tDQSRE	2	25	2	25	2	25	2	25	ns
Timing Mode Specific Values (Modes 4-7)									
	Mode 4		**Mode 5**		**Mode 6**		**Mode 7**		**Unit**
	10		7.5		6		5		ns
	100		~133		~166		200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	—	0.8	—	0.6	—	0.5	—	0.4	ns
tDQDQ	—	—	—	—	—	—	—	—	ns
tRC(avg) or tRC	10	—	7.5	—	6	—	5	—	ns
tREH/tRP(abs) (no training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH/tRP(avg) (no training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tREH(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tRP(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tRP(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tDVWp (per pin)	NA	—	NA	—	NA	—	NA	—	ns
tAC	2	25	2	25	2	25	2	25	ns
tDQSRE	2	25	2	25	2	25	2	25	ns
Timing Mode Specific Values (Modes 8-11)									
	Mode 8		**Mode 9**		**Mode 10**		**Mode 11**		**Unit**
	3.75		3		2.5		1.875		ns
	~267		~333		400		~533		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	—	0.350	—	0.3	—	0.25	—	0.188	ns
tDQDQ	—	—	—	—	—	—	—	—	ns

tRC(avg) or tRC	3.75	—	3	—	2.5	—	1.875	—	ns
tREH/tRP(abs) (no training)	0.43	—	0.43	—	0.43	—	0.45	—	tRC(avg)
tREH/tRP(avg) (no training)	0.45	0.55	0.45	0.55	0.45	0.55	0.47	0.53	tRC(avg)
tREH(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tRP(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tRP(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tDVWp (per pin)	NA	—	NA	—	NA	—	0.535	—	ns
tAC	2	25	2	25	2	25	2	25	ns
tDQSRE	2	25	2	25	2	25	2	25	ns
Timing Mode Specific Values (Mode 12-15)									
	Mode 12		**Mode 13**		**Mode 14**		**Mode 15**		**Unit**
	1.667		1.5		1.364		1.25		ns
	600		~667		~733		800		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	—	0.167	-0.250	0.250	-0.250	0.250	-0.250	0.250	ns
tDQDQ	—	—	—	0.200	—	0.200	—	0.200	ns
tRC(avg) or tRC	1.667	—	1.5	—	1.364	—	1.25	—	ns
tREH/tRP(abs) (no training)	0.45	—	—	—	—	—	—	—	tRC(avg)
tREH/tRP(avg) (no training)	0.47	0.53	—	—	—	—	—	—	tRC(avg)
tREH(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tRP(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tRP(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tDVWp (per pin)	0.475	—	0.428	—	0.389	—	0.356	—	ns
tAC	2	25	2	25	2	25	2	25	ns
tDQSRE	2	25	2	25	2	25	2	25	ns
Timing Mode Specific Values (Mode 16-19)									
	Mode 16		**Mode 17**		**Mode 18**		**Mode 19**		**Unit**
	1.111		1		0.909		0.833		ns
	900		1000		1100		1200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	-0.250	0.250	-0.250	0.250	-0.250	0.250	-0.250	0.250	ns
tDQDQ	—	0.200	—	0.200	—	0.200	—	0.200	ns
tRC(avg) or tRC	1.111	—	1	—	0.909	—	0.833	—	ns
tREH/tRP(abs) (no training)	—	—	—	—	—	—	—	—	tRC(avg)
tREH/tRP(avg) (no training)	—	—	—	—	—	—	—	—	tRC(avg)
tREH(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tRP(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tRP(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tDVWp (per pin)	0.317	—	0.285	—	0.259	—	0.237	—	ns
tAC	2	25	2	25	2	25	2	25	ns
tDQSRE	2	25	2	25	2	25	2	25	ns
Timing Mode Specific Values (Mode 20-22)									
	Mode 20		**Mode 21**		**Mode 22**				**Unit**
	0.714		0.625		0.555				ns
	1400		1600		1800				MHz
	Min	Max	Min	Max	Min	Max			
tDQSQ	-0.250	0.250	-0.250	0.250	-0.250	0.250			ns
tDQDQ	—	0.200	—	0.200	—	0.200			ns
tRC(avg) or tRC	1.111	—	1	—	0.909	—			ns
tREH/tRP(abs) (no training)	—	—	—	—	—	—			tRC(avg)
tREH/tRP(avg) (no training)	—	—	—	—	—	—			tRC(avg)
tREH(abs) (with training)	0.455	0.545	0.455	0.545	0.455	0.545			tRC(avg)
tRP(abs) (with training)	0.455	0.545	0.455	0.545	0.455	0.545			tRC(avg)
tREH(avg) (with training)	0.475	0.525	0.475	0.525	0.475	0.525			tRC(avg)
tRP(avg) (with training)	0.475	0.525	0.475	0.525	0.475	0.525			tRC(avg)

tDVWp (per pin)	0.203	—	0.178	—	0.158	—			ns
tAC	1.5	25	1.5	25	1.5	25			ns
tDQSRE	1.5	25	1.5	25	1.5	25			Ns

Table 4-79 NV-DDR2 / NV-DDR3 Timing Parameter Values: Data Output

4.19.4. NV-LPDDR4

Table 4-80, Table 4-81, Table 4-82 and Table 4-84 define the standard NV-LPDDR4 data interface timing modes. The host is not required to have a period that exactly matches the tDSC or tRC values listed for the standard timing modes. The host shall meet the setup and hold times and DQ Rx Mask requirements for the timing mode selected. If the host selects timing mode *n* using Set Features, then its tDSC and tRC values shall be faster than the tDSC and tRC values of timing mode *n-1* and slower than or equal to the tDSC and tRC values of timing mode *n*. The timing modes shall meet the testing conditions defined in Table 4-9. The timing parameters when VOH,nom = VccQ/3 are verified using 50 Ohms CH_ODT settings for the pull-up and 37.5 Ohm drive strength for the pull-down. In addition, ZQ Calibration must have been run, differential signaling for both RE_n (RE_t/RE_c) and DQS (DQS_t/DQS_c) signals must have been enabled, and internal VrefQ on the controller must have been trained with Read DQ Training and internal VrefQ on the NAND must have been trained with Write DQ Training. For data rates >800MT/s DCC training must have been run and warmup cycles enabled.

The DQ, DBI, RE and DQS input signals must satisfy the requirements given in the DC and Operating Conditions for VccQ of 1.2V (NV-LPDDR4), measured on VccQ rail table (Table 2-16)**,** as well as minimum input slew rate requirements outlined in Table 4-50 NV-LPDDR4 Maximum and Minimum Input Slew Rate. For DQ and DBI signals they must also satisfy the DQ Rx Mask requirements outlined in section 4.18.6 NV-DDR3/NV-LPDDR4 DQ Rx Mask Specification.

The following requirements apply to the timing parameter values:

1. tCHZ and tCLHZ are not referenced to a specific voltage level but specify when the device output is no longer driving.
2. The parameters tRC(avg) and tDSC(avg) are the average over any 200 consecutive periods and tRC(avg)/tDSC(avg) min are the smallest rates allowed, with the exception of a deviation due to tJITper.
3. Input jitter is allowed provided it does not exceed values specified.
4. tREH(avg) and RP(avg) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter, Input clock jitter is allowed provided it does not exceed values specified.
5. The period jitter (tJITper) is the maximum deviation in the tRC or tDSC period from the average or nominal tRC or tDSC over any 200 consecutive periods. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter (tJITcc) is the amount the clock period can deviate from one cycle to the next.
7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed tJITper. As long as the absolute minimum half period tRP(abs), tREH(abs), tDQSH or tDQSL is not less than 43 percent of the average cycle (tRP(abs) and tREH(abs) not less than 45 percent of the average cycle for ≥800 MTs with no training).
8. When the device is operated with input RE_n (RE_t/RE_c) jitter, tQSL, tQSH, and tQH need to be derated by the actual input duty cycle jitter beyond 0.45 * tRC(avg) but not exceeding 0.43 * tRC(avg) for less than 800 MT/s operation. Output deratings are relative to the device input RE_n pulse that generated the DQS pulse. For operation above 800 MT/s, even with input RE jitter, tREH(abs) and tRP(abs) should not go lower than 0.43 * tRC(avg)."
9. Minimizing the amount of duty cycle jitter to more than 45% of the average cycle provides a larger tQH, which in turn provides a larger data valid window. The device shall provide a

minimum of 0.5% of larger data valid window for each 1% improvement in duty cycle jitter. For example, if the host provides a tREH(abs) of 0.49 * tRC(avg) then the device shall provide at least a tQH of 0.39 * tRC(avg).

10. The parameter tDIPW is defined as the pulse width of the input signal between the first crossing of Vcent_DQ (pin_mid) and the consecutive crossing of Vcent_DQ (pin_mid).
11. For data rates up to 1200MT/s, parameters tDQSQ and tQH are used to calculate overall tDVWd (tDVWd = tQH - tDQSQ). tDVWd is the data valid window per device per UI and is derived from [tQH – tDQSQ] of each UI on a pin per device. Since data eye training to optimize strobe placement is expected at high I/O speeds (≥533 MT/s), tDQSQ and tQH may borrow time from each other without changing tDVWd. For example, if there exists X ps of margin on tDQSQ then tQH can be provided with an additional X ps without changing the value of tDVWd. When timing margin is borrowed from tDQSQ to provide additional timing for tQH, the same amount of timing margin can be used for additional timing for tQSL/tQSH. For data rates >1200MT/s, the tDVWp spec shall be used instead for the NAND output valid window. NAND devices may require that DCC training be done to be able to meet tDVWp (per pin valid window) requirements for >800 MT/s data rates. In order for a system to take advantage of the wider tDVWp (per pin valid window) data-eye opening versus tDVWd (overall valid window), the system must employ the ability to de-skew each individual DQ pin against DQS with Read Training.
12. For greater than 800MTs, warmup cycle(s) are required for both data input and output.
13. Both tDQS2DQ and tDQ2DQ are parameters used only when Write DQ training is supported. TDQS2DQ is the maximum allowable skew between DQS and DQ at the NAND package ball, while TDQ2DQ is the maximum allowable skew between DQ signals on a single LUN at the NAND package ball. The controller should be capable of compensating for the maximum amount of TDQS2DQ and TDQ2DQ skew during write training. The optional Write Training (RX side) mode though is not required to compensate for the maximum TDQS2DQ and TDQ2DQ amount of skew. Even with tDQS2DQ and tDQ2DQ, tDIPW still needs to be met.

Constant Timing Parameter Values			
	Min	Max	Unit
tADL	400	400	ns
tAR	10	—	ns
tCAH	5	—	ns
tCAS	5	—	ns
tCALH	5	—	ns
tCALS	15	—	ns
tCEH	20	—	ns
tCH	5	—	ns
tCS	20	—	ns
tCS1	30	—	ns
tCS2	40	—	ns
tCSD	10	—	ns
tCHZ	—	30	ns
tCLHZ	—	30	ns
tCLR	10	—	ns
tCR	10	—	ns
tCR2	100	—	ns
tCR2 (Read ID) [1]	150	—	ns
tDBS	5	—	ns
tRHW	100	—	ns
tWC	25	—	ns
tWH	11	—	ns
tWP	11	—	ns
tWHR	80	—	ns
tWHRT	400	—	ns
tWTRN	—	200	µs
tWW	100	—	ns
tFEAT	—	1	µs
tITC	—	1	µs
tRST	—	18/30/500	µs
tRR	20	—	ns
tWB	—	100	ns

NOTE:
1. tCR2(min) is 150ns for Read ID sequence only. For all other command sequences tCR2(min) requirement is 100ns.

Table 4-80 NV-LPDDR4 Timing Parameter Values: Command and Address

Timing Mode Specific Values (Modes 0-3)									
	Mode 0		Mode 1		Mode 2		Mode 3		Unit
	30		25		15		12		ns
	~ 33		40		~ 66		~ 83		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper (DQS)	-2.4	2.4	-2.0	2.0	-1.2	1.2	-1.0	1.0	ns
tJITper (RE_n)	-1.8	1.8	-1.5	1.5	-0.9	0.9	-0.75	0.75	ns
tJITcc (DQS)	—	4.8	—	4.0	—	2.4	—	2.0	ns
tJITcc (RE_n)	—	3.6	—	3.0	—	1.8	—	1.5	ns
Timing Mode Specific Values (Modes 4-7)									
	Mode 4		**Mode 5**		**Mode 6**		**Mode 7**		**Unit**
	10		7.5		6		5		ns
	100		~133		~166		200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper(DQS)	-0.80	0.80	-0.60	0.60	-0.48	0.48	-0.40	0.40	ns
tJITper(RE_n)	-0.60	0.60	-0.45	0.45	-0.36	0.36	-0.30	0.30	ns
tJITcc(DQS)	—	1.6	—	1.2	—	0.96	—	0.8	ns
tJITcc(RE_n)	—	1.2	—	0.9	—	0.72	—	0.6	ns
Timing Mode Specific Values (Modes 8-11)									
	Mode 8		**Mode 9**		**Mode 10**		**Mode 11**		**Unit**
	3.75		3		2.5		1.875		ns
	~267		~333		400		~533		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper(DQS)	-0.30	0.30	-0.24	0.24	-0.2	0.2	-0.094	0.094	ns
tJITper(RE_n)	-0.225	0.225	-0.18	0.18	-0.15	0.15	-0.094	0.094	ns
tJITcc(DQS)	—	0.6	—	0.48	—	0.4	—	0.188	ns
tJITcc(RE_n)	—	0.45	—	0.36	—	0.3	—	0.188	ns
Timing Mode Specific Values (Mode 12-15)									
	Mode 12		**Mode 13**		**Mode 14**		**Mode 15**		**Unit**
	1.667		1.5		1.364		1.25		ns
	600		~667		~733		800		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper(DQS)	-0.083	0.083	-0.078	0.078	-0.075	0.075	-0.070	0.070	ns
tJITper(RE_n)	-0.083	0.083	-0.078	0.078	-0.075	0.075	-0.070	0.070	ns
tJITcc(DQS)	—	0.167	—	0.156	—	0.150	—	0.140	ns
tJITcc(RE_n)	—	0.167	—	0.156	—	0.150	—	0.140	ns
Timing Mode Specific Values (Mode 16-19)									
	Mode 16		**Mode 17**		**Mode 18**		**Mode 19**		**Unit**
	1.111		1		0.909		0.833		ns
	900		1000		1100		1200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper(DQS)	-0.062	0.062	-0.056	0.056	-0.051	0.051	-0.047	0.047	ns
tJITper(RE_n)	-0.062	0.062	-0.056	0.056	-0.051	0.051	-0.047	0.047	ns
tJITcc(DQS)	—	0.124	—	0.112	—	0.102	—	0.094	ns
tJITcc(RE_n)	—	0.124	—	0.112	—	0.102	—	0.094	ns
Timing Mode Specific Values (Mode 20-22)									
	Mode 20		**Mode 21**		**Mode 22**				**Unit**
	0.714		0.625		0.555				ns
	1400		1600		1800				MHz
	Min	Max	Min	Max	Min	Max			
tJITper(DQS)	-0.032	0.032	-0.028	0.028	-0.025	0.025			ns
tJITper(RE_n)	-0.032	0.032	-0.028	0.028	-0.025	0.025			ns
tJITcc(DQS)	—	0.064	—	0.056	—	0.050			ns
tJITcc(RE_n)	—	0.064	—	0.056	—	0.050			ns

Table 4-81 NV-LPDDR4 Timing Parameter Values: Jitter

Constant Timing Parameter Values									
	Min				Max				Unit
tCALQS2	25				—				ns
tCDQSS	30				—				ns
tCDQSH	100				—				ns
tCD	100				—				ns
tDSC(abs)	tDSC(avg) + tJITper(DQS) min				tDSC(avg) + tJITper(DQS) max				ns
tWPRE2	25				—				ns
tWPST	6.5				—				ns
tWPSTH	25				—				ns
Timing Mode Specific Values (Modes 0-3)									
	Mode 0		**Mode 1**		**Mode 2**		**Mode 3**		**Unit**
	30		25		15		12		ns
	~ 33		40		~ 66		~ 83		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDIVW1	—	0.48	—	0.48	—	0.48	—	0.48	UI
tDIVW2	—	0.30	—	0.30	—	0.30	—	0.30	UI
tDIPW	0.31	—	0.31	—	0.31	—	0.31	—	tDSC(avg)
tDQS2DQ (training)	NA	NA	NA	NA	NA	NA	NA	NA	ns
tDQ2DQ (training)	—	NA	—	NA	—	NA	—	NA	ns
tDQSH (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSL (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSH (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDQSL (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDSC(avg) or tDSC	30	—	25	—	15	—	12	—	ns
Timing Mode Specific Values (Modes 4-7)									
	Mode 4		**Mode 5**		**Mode 6**		**Mode 7**		**Unit**
	10		7.5		6		5		ns
	100		~133		~166		200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDIVW1	—	0.48	—	0.48	—	0.48	—	0.48	UI
tDIVW2	—	0.30	—	0.30	—	0.30	—	0.30	UI
tDIPW	0.31	—	0.31	—	0.31	—	0.31	—	tDSC(avg)
tDQS2DQ (training)	NA	NA	NA	NA	NA	NA	NA	NA	ns
tDQ2DQ (training)	—	NA	—	NA	—	NA	—	NA	ns
tDQSH (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSL (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSH (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDQSL (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDSC(avg) or tDSC	10	—	7.5	—	6	—	5	—	ns
Timing Mode Specific Values (Modes 8-11)									
	Mode 8		**Mode 9**		**Mode 10**		**Mode 11**		**Unit**
	3.75		3		2.5		1.875		ns
	~267		~333		400		~533		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDIVW1	—	0.48	—	0.48	—	0.48	—	0.48	UI
tDIVW2	—	0.30	—	0.30	—	0.30	—	0.30	UI
tDIPW	0.31	—	0.31	—	0.31	—	0.33	—	tDSC(avg)
tDQS2DQ (training)	NA	NA	NA	NA	NA	NA	-0.200	0.200	ns
tDQ2DQ (training)	—	NA	—	NA	—	NA	—	0.100	ns
tDQSH (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSL (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSH (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDQSL (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDSC(avg) or tDSC	3.75	—	3	—	2.5	—	1.875	—	ns
Timing Mode Specific Values (Mode 12-15)									
	Mode 12		**Mode 13**		**Mode 14**		**Mode 15**		**Unit**

	1.667		1.5		1.364		1.25		ns
	600		~667		~733		800		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDIVW1	—	0.48	—	0.48	—	0.48	—	0.48	UI
tDIVW2	—	0.30	—	0.30	—	0.30	—	0.30	UI
tDIPW	0.33	—	0.33	—	0.33	—	0.33	—	tDSC(avg)
tDQS2DQ (training)	-0.200	0.200	-0.200	0.200	-0.200	0.200	-0.200	0.200	ns
tDQ2DQ (training)	—	0.100	—	0.100	—	0.100	—	0.100	ns
tDQSH (abs)	0.45	—	0.448	—	0.445	—	0.444	—	tDSC(avg)
tDQSL (abs)	0.45	—	0.448	—	0.445	—	0.444	—	tDSC(avg)
tDQSH (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDQSL (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDSC(avg) or tDSC	1.667	—	1.5	—	1.364	—	1.25	—	ns
Timing Mode Specific Values (Mode 16-19)									
	Mode 16		**Mode 17**		**Mode 18**		**Mode 19**		**Unit**
	1.111		1		0.909		0.833		ns
	900		1000		1100		1200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDIVW1	—	0.48	—	0.48	—	0.48	—	0.48	UI
tDIVW2	—	0.30	—	0.30	—	0.30	—	0.30	UI
tDIPW	0.33	—	0.33	—	0.33	—	0.33	—	tDSC(avg)
tDQS2DQ (training)	-0.200	0.200	-0.200	0.200	-0.200	0.200	-0.200	0.200	ns
tDQ2DQ (training)	—	0.100	—	0.100	—	0.100	—	0.100	ns
tDQSH (abs)	0.444	—	0.444	—	0.444	—	0.444	—	tDSC(avg)
tDQSL (abs)	0.444	—	0.444	—	0.444	—	0.444	—	tDSC(avg)
tDQSH (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDQSL (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDSC(avg) or tDSC	1.111	—	1	—	0.909	—	0.833	—	ns
Timing Mode Specific Values (Mode 20-22)									
	Mode 20		**Mode 21**		**Mode 22**				**Unit**
	0.714		0.625		0.555				ns
	1400		1600		1800				MHz
	Min	Max	Min	Max	Min	Max			
tDIVW1	—	0.48	—	0.48	—	0.48			UI
tDIVW2	—	0.30	—	0.30	—	0.30			UI
tDIPW	0.33	—	0.33	—	0.33	—			tDSC(avg)
tDQS2DQ (training)	-0.200	0.200	-0.200	0.200	-0.200	0.200			ns
tDQ2DQ (training)	—	0.100	—	0.100	—	0.100			ns
tDQSH (abs)	0.455	0.545	0.455	0.545	0.455	0.545			tDSC(avg)
tDQSL (abs)	0.455	0.545	0.455	0.545	0.455	0.545			tDSC(avg)
tDQSH (avg)	0.475	0.525	0.475	0.525	0.475	0.525			tDSC(avg)
tDQSL (avg)	0.475	0.525	0.475	0.525	0.475	0.525			tDSC(avg)
tDSC(avg) or tDSC	0.714	—	0.625	—	0.555	—			ns

NOTE:
1. Unit Interval (UI) is 0.5*tDSC(avg).

Table 4-82 NV-LPDDR4 Timing Parameter Values: Data Input

The Controller DQ RX Mask specifications in the Table 4-76 below are applicable to controllers that support the data rates listed in the tables below for NV-DDR3 mode. These specifications do not apply to NAND component

Timing Mode Specific Values (Mode 16-19)									
	Mode 16		**Mode 17**		**Mode 18**		**Mode 19**		**Unit**
	1.111		1		0.909		0.833		ns
	900		1000		1100		1200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDIVW1	—	0.40	—	0.40	—	0.40	—	0.40	UI
tDIVW2	—	0.25	—	0.25	—	0.25	—	0.25	UI
tDIPW	0.25	—	0.25	—	0.25	—	0.25	—	tDSC(avg)
Timing Mode Specific Values (Mode 20-22)									
	Mode 20		**Mode 21**		**Mode 22**				**Unit**
	0.714		0.625		0.555				ns
	1400		1600		1800				MHz
	Min	Max	Min	Max	Min	Max			
tDIVW1	—	0.40	—	0.40	—	0.40			UI
tDIVW2	—	0.25	—	0.25	—	0.25			UI
tDIPW	0.25	—	0.25	—	0.25	—			tDSC(avg)

NOTE:

1. Unit Interval (UI) is 0.5*tDSC(avg).
2. Vcent_DQ (pin_mid) shall be replaced by VrefQ in the case where External VrefQ is used or Internal VrefQ without Vref training is used.
3. At 1600Mbps, use of Rx mask specifications is optional, see vendor datasheet whether Rx mask specifications are supported by the device at that data rate.
4. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment

Table 4-83 Controller NV-LPDDR4 Timing Parameter Values: Data Input

Constant Timing Parameter Values			
	Min	Max	Unit
dQSQ/dT	-0.5	0.5	ps/^{o}C
dQSQ/dV	-0.35	0.35	ps/mv
tCALR2	25	—	ns
tDQSD	5	18	ns
tDVWd (device)	tDVWd = tQH – tDQSQ (TM0-TM12)		ns
tQH	0.37 (TM0-TM12)	—	tRC(avg)
tQSH	0.37	—	tRC(avg)
tQSL	0.37	—	tRC(avg)
tRC(abs)	tRC(avg) + tJITper(RE_n) min	tRC(avg) + tJITper(RE_n) max	ns
tRPRE2	25	—	ns
tRPST	tDQSRE + 0.5*tRC	—	ns
tRPSTH	15	—	ns
tDQSRH	3	5	ns

Timing Mode Specific Values (Modes 0-3)									
	Mode 0		Mode 1		Mode 2		Mode 3		Unit
	30		25		15		12		ns
	~ 33		40		~ 66		~ 83		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	—	2.5	—	2.0	—	1.4	—	1.0	ns
tDQDQ	—	—	—	—	—	—	—	—	ns
tRC(avg) or tRC	30	—	25	—	15	—	12	—	ns
tREH/tRP(abs) (no training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH/tRP(avg) (no training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tREH(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tRP(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tRP(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tDVWp (per pin)	NA	—	NA	—	NA	—	NA	—	ns
tAC	2	25	2	25	2	25	2	25	ns
tDQSRE	2	25	2	25	2	25	2	25	ns
Timing Mode Specific Values (Modes 4-7)									
	Mode 4		**Mode 5**		**Mode 6**		**Mode 7**		**Unit**
	10		7.5		6		5		ns
	100		~133		~166		200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	—	0.8	—	0.6	—	0.5	—	0.4	ns
tDQDQ	—	—	—	—	—	—	—	—	ns
tRC(avg) or tRC	10	—	7.5	—	6	—	5	—	ns
tREH/tRP(abs) (no training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH/tRP(avg) (no training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tREH(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tRP(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tRP(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tDVWp (per pin)	NA	—	NA	—	NA	—	NA	—	ns
tAC	2	25	2	25	2	25	2	25	ns
tDQSRE	2	25	2	25	2	25	2	25	ns
Timing Mode Specific Values (Modes 8-11)									
	Mode 8		**Mode 9**		**Mode 10**		**Mode 11**		**Unit**
	3.75		3		2.5		1.875		ns
	~267		~333		400		~533		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	—	0.350	—	0.3	—	0.25	—	0.188	ns
tDQDQ	—	—	—	—	—	—	—	—	ns
tRC(avg) or tRC	3.75	—	3	—	2.5	—	1.875	—	ns
tREH/tRP(abs) (no training)	0.43	—	0.43	—	0.43	—	0.45	—	tRC(avg)
tREH/tRP(avg) (no training)	0.45	0.55	0.45	0.55	0.45	0.55	0.47	0.53	tRC(avg)
tREH(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tRP(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tRP(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tDVWp (per pin)	NA	—	NA	—	NA	—	0.535	—	ns
tAC	2	25	2	25	2	25	2	25	ns
tDQSRE	2	25	2	25	2	25	2	25	ns
Timing Mode Specific Values (Mode 12-15)									
	Mode 12		**Mode 13**		**Mode 14**		**Mode 15**		**Unit**
	1.667		1.5		1.364		1.25		ns
	600		~667		~733		800		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	—	0.167	-0.250	0.250	-0.250	0.250	-0.250	0.250	ns

tDQDQ	—	—	—	0.200	—	0.200	—	0.200	ns
tRC(avg) or tRC	1.667	—	1.5	—	1.364	—	1.25	—	ns
tREH/tRP(abs) (no training)	0.45	—	—	—	—	—	—	—	tRC(avg)
tREH/tRP(avg) (no training)	0.47	0.53	—	—	—	—	—	—	tRC(avg)
tREH(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tRP(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tRP(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tDVWp (per pin)	0.475	—	0.428	—	0.389	—	0.356	—	ns
tAC	2	25	2	25	2	25	2	25	ns
tDQSRE	2	25	2	25	2	25	2	25	ns
Timing Mode Specific Values (Mode 16-19)									
	Mode 16		**Mode 17**		**Mode 18**		**Mode 19**		**Unit**
	1.111		1		0.909		0.833		ns
	900		1000		1100		1200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	-0.250	0.250	-0.250	0.250	-0.250	0.250	-0.250	0.250	ns
tDQDQ	—	0.200	—	0.200	—	0.200	—	0.200	ns
tRC(avg) or tRC	1.111	—	1	—	0.909	—	0.833	—	ns
tREH/tRP(abs) (no training)	—	—	—	—	—	—	—	—	tRC(avg)
tREH/tRP(avg) (no training)	—	—	—	—	—	—	—	—	tRC(avg)
tREH(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tRP(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tRP(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tDVWp (per pin)	0.317	—	0.285	—	0.259	—	0.237	—	ns
tAC	2	25	2	25	2	25	2	25	ns
tDQSRE	2	25	2	25	2	25	2	25	ns
Timing Mode Specific Values (Mode 20-22)									
	Mode 20		**Mode 21**		**Mode 22**				**Unit**
	0.714		0.625		0.555				ns
	1400		1600		1800				MHz
	Min	Max	Min	Max	Min	Max			
tDQSQ	-0.250	0.250	-0.250	0.250	-0.250	0.250			ns
tDQDQ	—	0.200	—	0.200	—	0.200			ns
tRC(avg) or tRC	1.111	—	1	—	0.909	—			ns
tREH/tRP(abs) (no training)	—	—	—	—	—	—			tRC(avg)
tREH/tRP(avg) (no training)	—	—	—	—	—	—			tRC(avg)
tREH(abs) (with training)	0.455	0.545	0.455	0.545	0.455	0.545			tRC(avg)
tRP(abs) (with training)	0.455	0.545	0.455	0.545	0.455	0.545			tRC(avg)
tREH(avg) (with training)	0.475	0.525	0.475	0.525	0.475	0.525			tRC(avg)
tRP(avg) (with training)	0.475	0.525	0.475	0.525	0.475	0.525			tRC(avg)
tDVWp (per pin)	0.203	—	0.178	—	0.158	—			ns
tAC	1.5	25	1.5	25	1.5	25			ns
tDQSRE	1.5	25	1.5	25	1.5	25			ns

Table 4-84 NV-LPDDR4 Timing Parameter Values: Data Output

4.20. Timing Diagrams

This section defines the timing diagrams for each phase of an operation (command, address, data input, and data output cycles) for each data interface. A timing diagram of the Read ID command using each data interface is shown in Figure 5-10, Figure 5-11, and Figure 5-12 for SDR, NV-DDR, and NV-DDR2/NV-DDR-3/NV-LPDDR4 respectively. A timing diagram of the Read Status command using each data interface is shown in Figure 5-17, Figure 5-18, and Figure 5-19 for SDR, NV-DDR, and NV-DDR2/NV-DDR-3/NV-LPDDR4 respectively.

4.20.1. SDR

4.20.1.1. Command Latch Timings

The requirements for the R/B_n signal only apply to commands where R/B_n is cleared to zero after the command is issued, as specified in the command definitions.

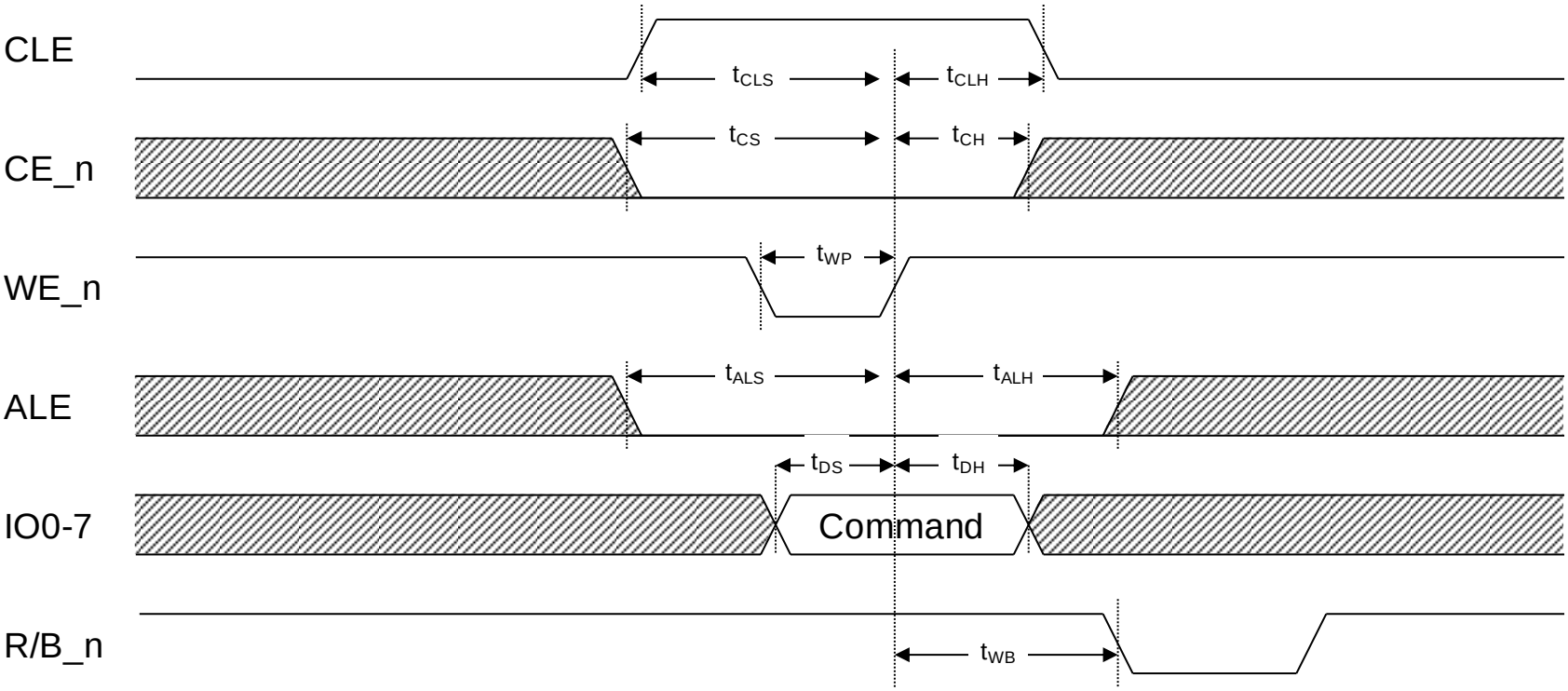


Figure 4-24 Command latch timings

4.20.1.2. Address Latch Timings

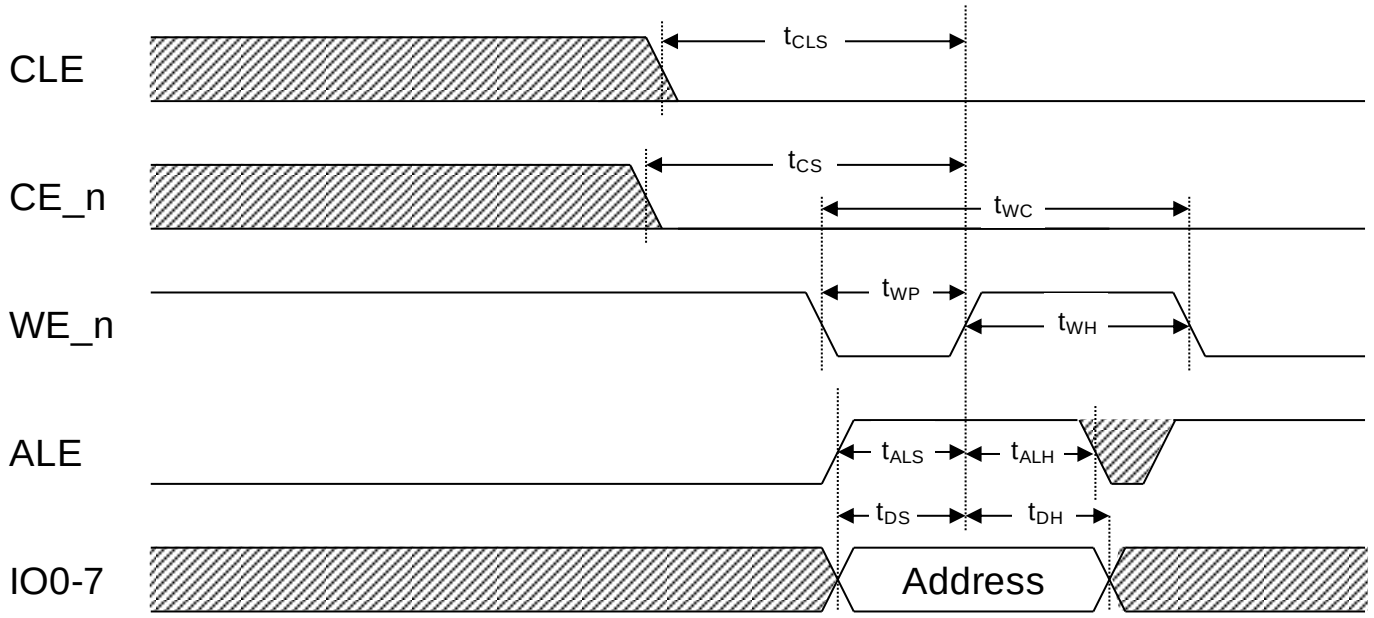


Figure 4-25 Address latch timings

4.20.1.3. Data Input Cycle Timings

Data input may be used with CE_n don't care. However, if CE_n don't care is used tCS and tCH timing requirements shall be met by the host, and WE_n falling edge shall always occur after the CE_n falling edge (i.e. tCS > tWP).

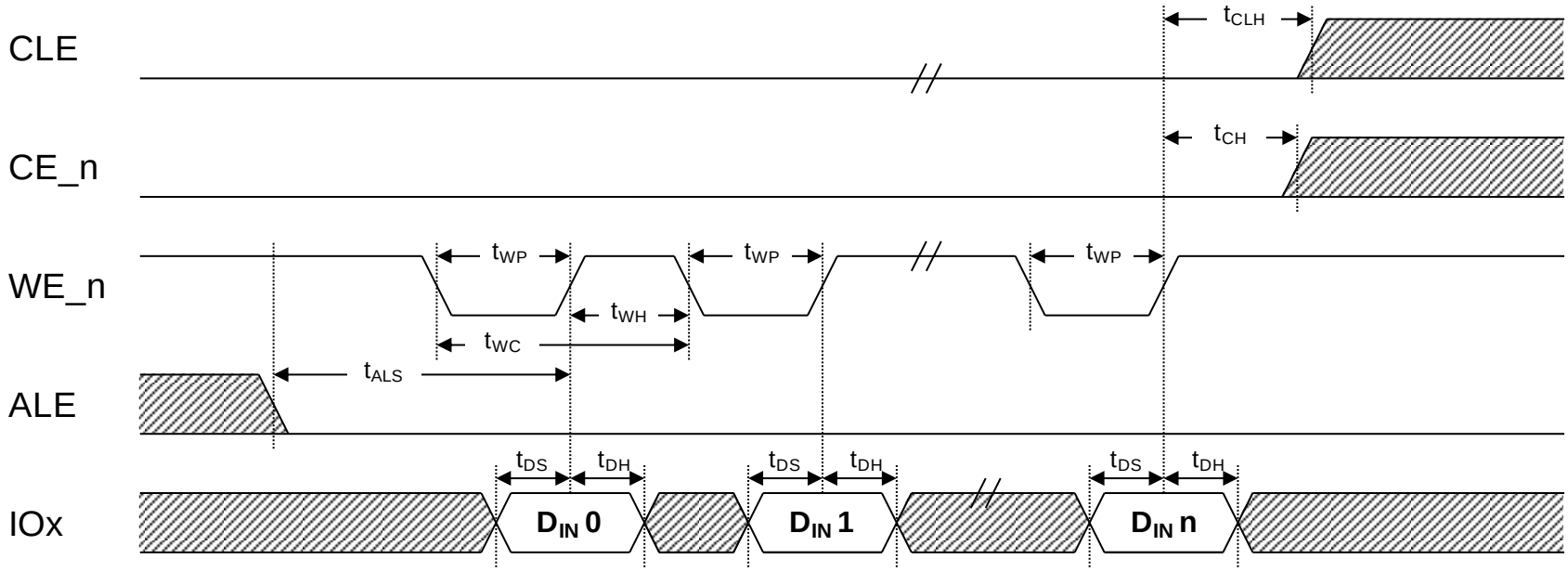


Figure 4-26 Data input cycle timings

4.20.1.4. Data Output Cycle Timings

Data output may be used with CE_n don't care. However, if CE_n don't care is used tCEA and tCOH timing requirements shall be met by the host and RE_n shall either remain low or RE_n falling edge shall occur after the CE_n falling edge.

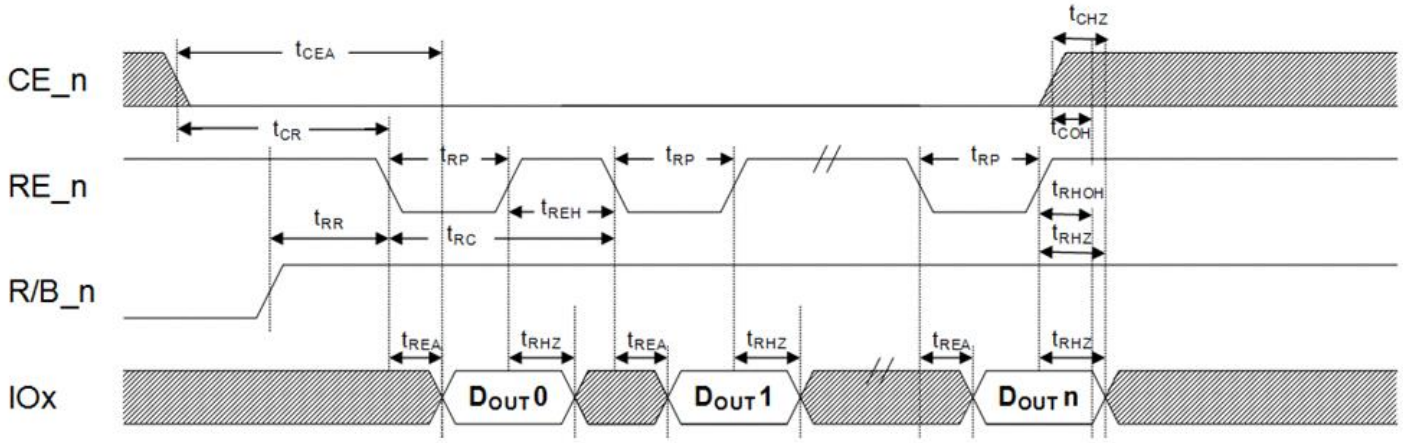


Figure 4-27 Data output cycle timings

4.20.1.5. Data Output Cycle Timings (EDO)

EDO data output cycle timings shall be used if the host drives tRC less than 30 ns. Data output may be used with CE_n don't care. However, if CE_n don't care is used tCEA and tCOH timing requirements shall be met by the host.

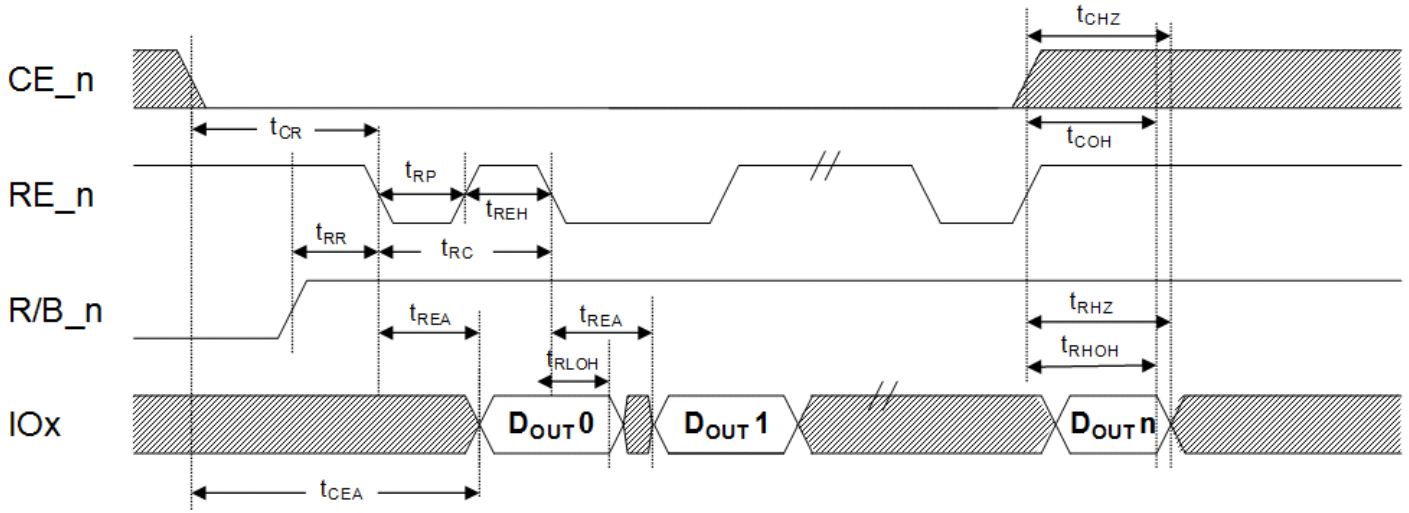


Figure 4-28 EDO data output cycle timings

4.20.1.6. Read Status Timings

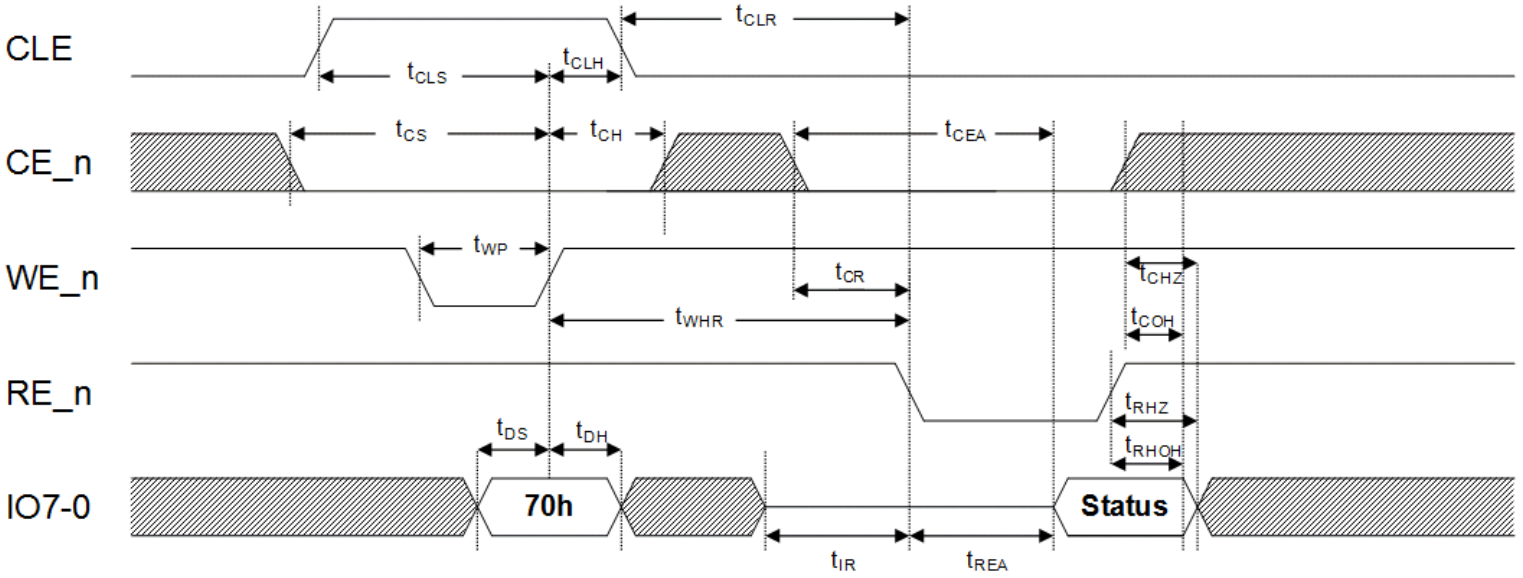


Figure 4-29 Read Status timings

4.20.1.7. Read Status Enhanced Timings

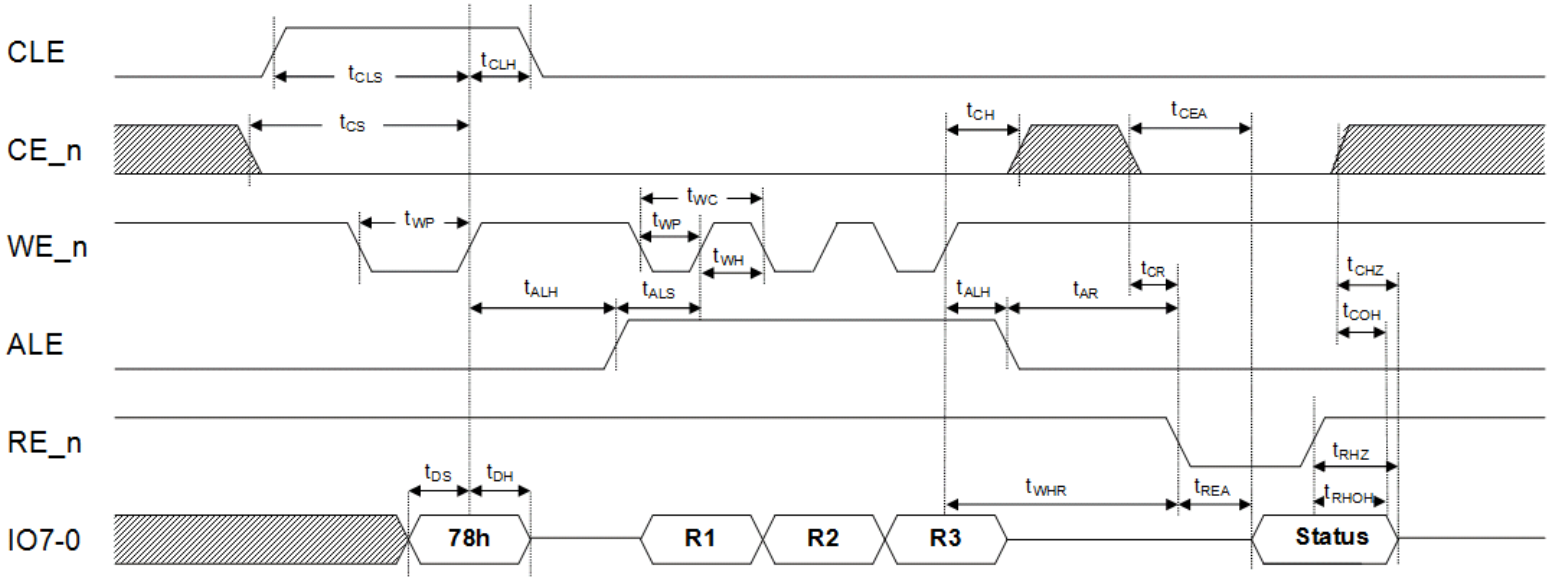


Figure 4-30 Read Status Enhanced timings

4.20.2. NV-DDR

For the command, address, data input, and data output diagrams, the tCS timing parameter may consume multiple clock cycles. The host is required to satisfy tCS by the rising edge of CLK shown in the diagrams, and thus needs to pull CE_n low far enough in advance to meet this requirement (which could span multiple clock cycles).

4.20.2.1. Command Cycle Timings

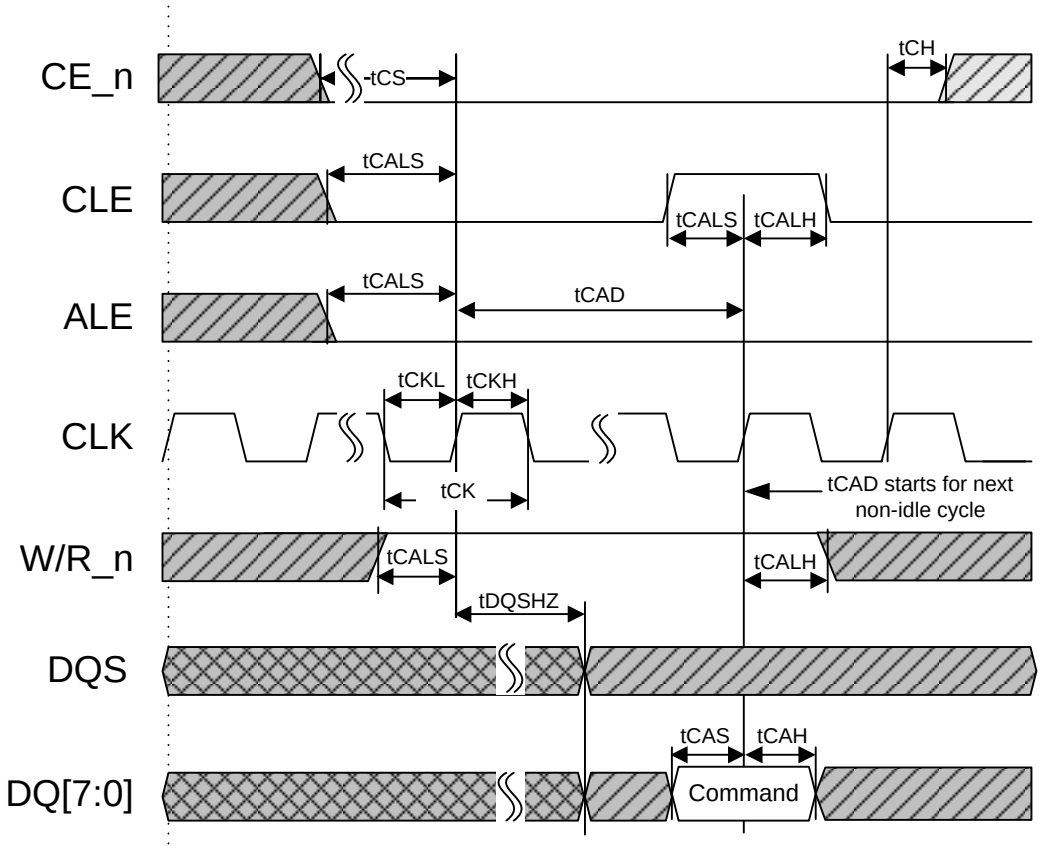


Figure 4-31 Command cycle timings

NOTE:

1. The cycle that tCAD is measured from may be an idle cycle (as shown), another command cycle, an address cycle, or a data cycle. The idle cycle is shown in this diagram for simplicity.
2. ALE and CLE shall be in a valid state when CE_n transitions from one to zero. In the diagram, it appears that tCS and tCALS are equivalent times. However, tCS and tCALS values are not the same, the timing parameter values should be consulted in Table 4-74.

4.20.2.2. Address Cycle Timings

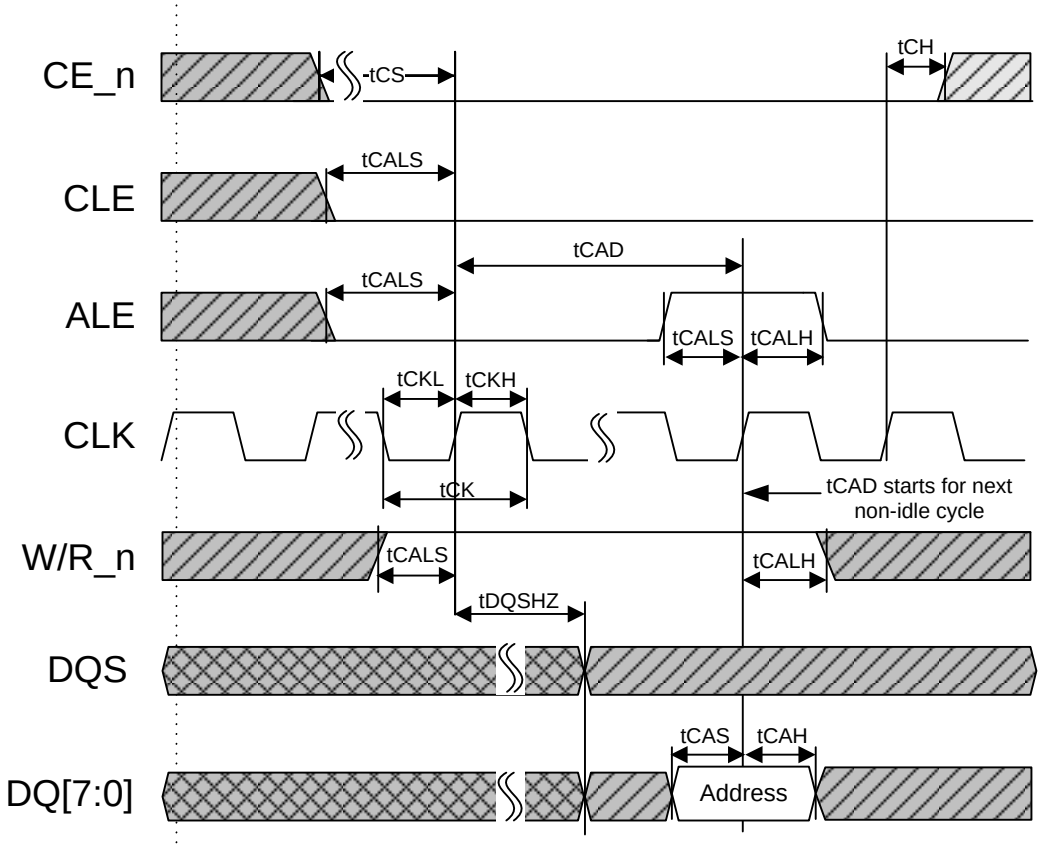


Figure 4-32 Address cycle timings

NOTE:

1. ALE and CLE shall be in a valid state when CE_n transitions from one to zero. In the diagram, it appears that tCS and tCALS are equivalent times. However, tCS and tCALS values are not the same, the timing parameter values should be consulted in Table 4-74.

4.20.2.3. Data Input Cycle Timings

Data input cycle timing describes timing for data transfers from the host to the device (i.e. data writes).

For the Set Features command, the same data byte is repeated twice. The data pattern in this case is D_0 D_0 D_1 D_1 D_2 D_2 etc. The device shall only latch one copy of each data byte. CLK should not be stopped during data input for the Set Features command. The device is not required to wait for the repeated data byte before beginning internal actions.

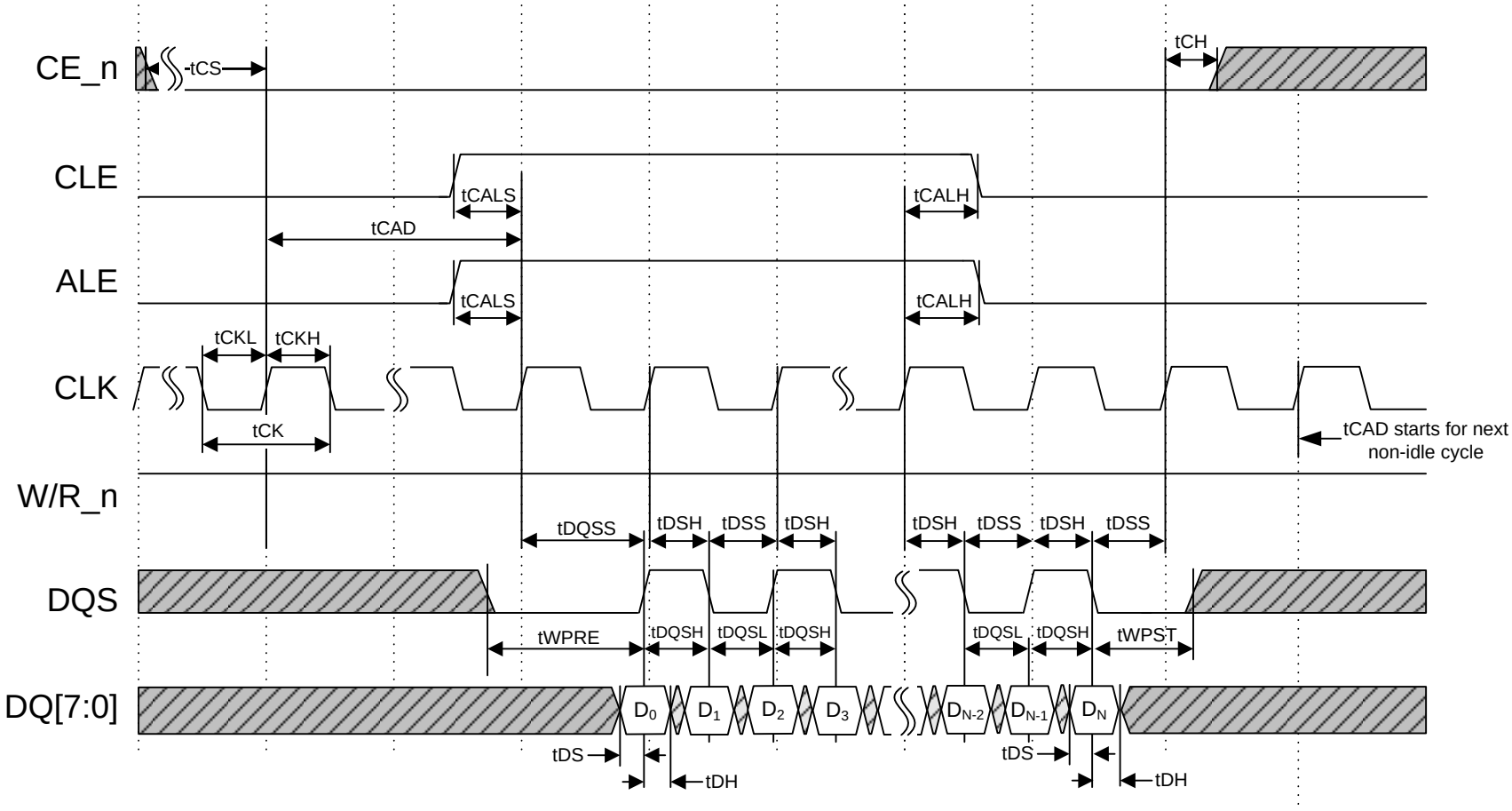


Figure 4-33 Data input cycle timing

4.20.2.4. Data Input Cycle Timings, CLK stopped

The host may save power during the data input cycles by holding the CLK signal high (i.e. stopping the CLK). The host may only stop the CLK during data input if the device supports this feature as indicated in the parameter page. Data input cycle timing describes timing for data transfers from the host to the device (i.e. data writes). Figure 4-34 describes data input cycling with the CLK signal stopped. The values of the ALE, CLE, and W/R_n signals are latched on the rising edge of CLK and thus while CLK is held high these signals are don't care.

Figure 4-35 shows data input cycling with the CLK signal stopped where the host has optionally paused data input. The host may pause data input if it observes the tDPZ timing parameter for re-starting data input to the device. When re-starting the CLK, the host shall observe the indicated timing parameters in Figure 4-34 and Figure 4-35, which include tDSS and tDSH.

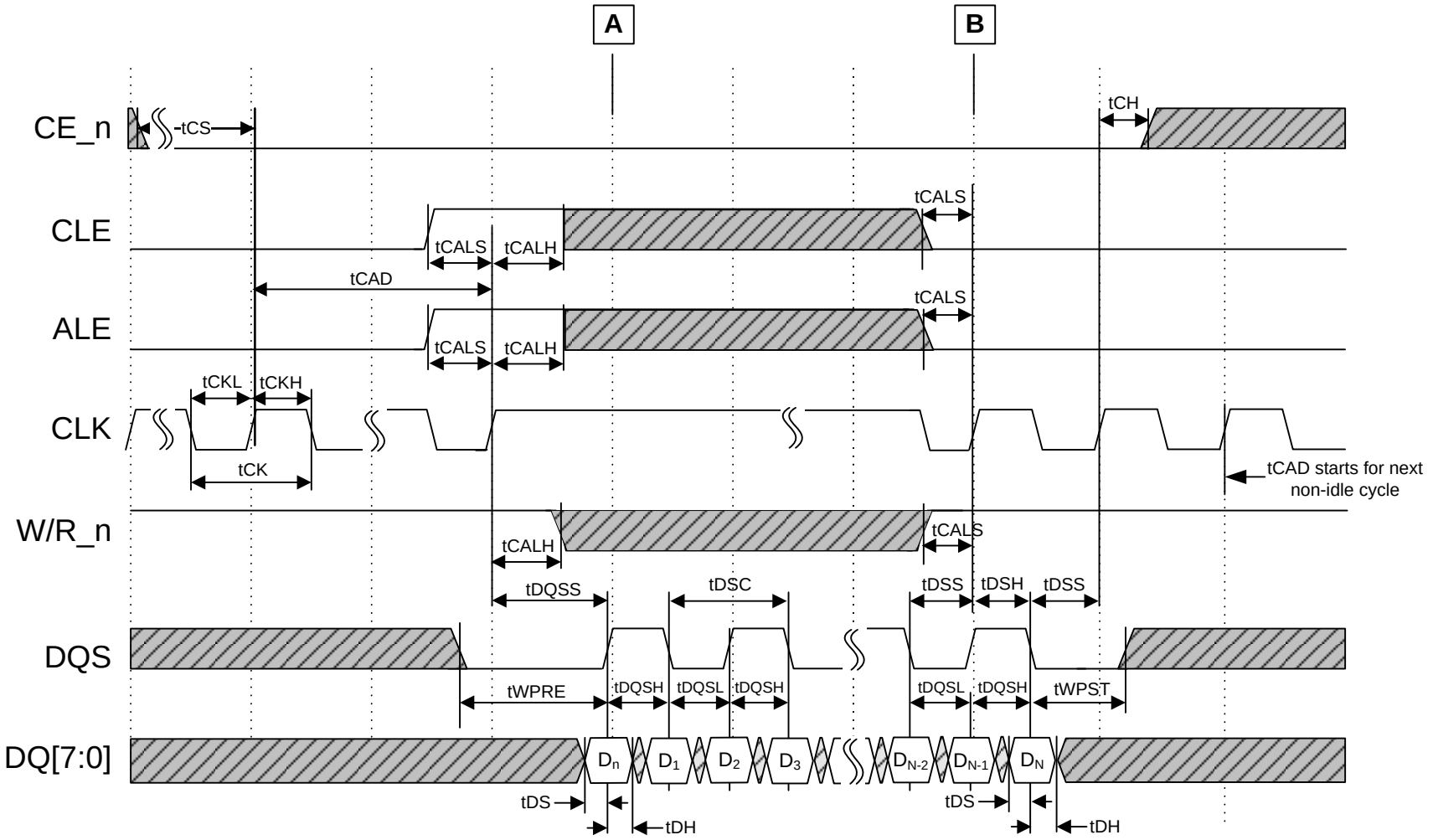


Figure 4-34 Data input cycle timing, CLK stopped

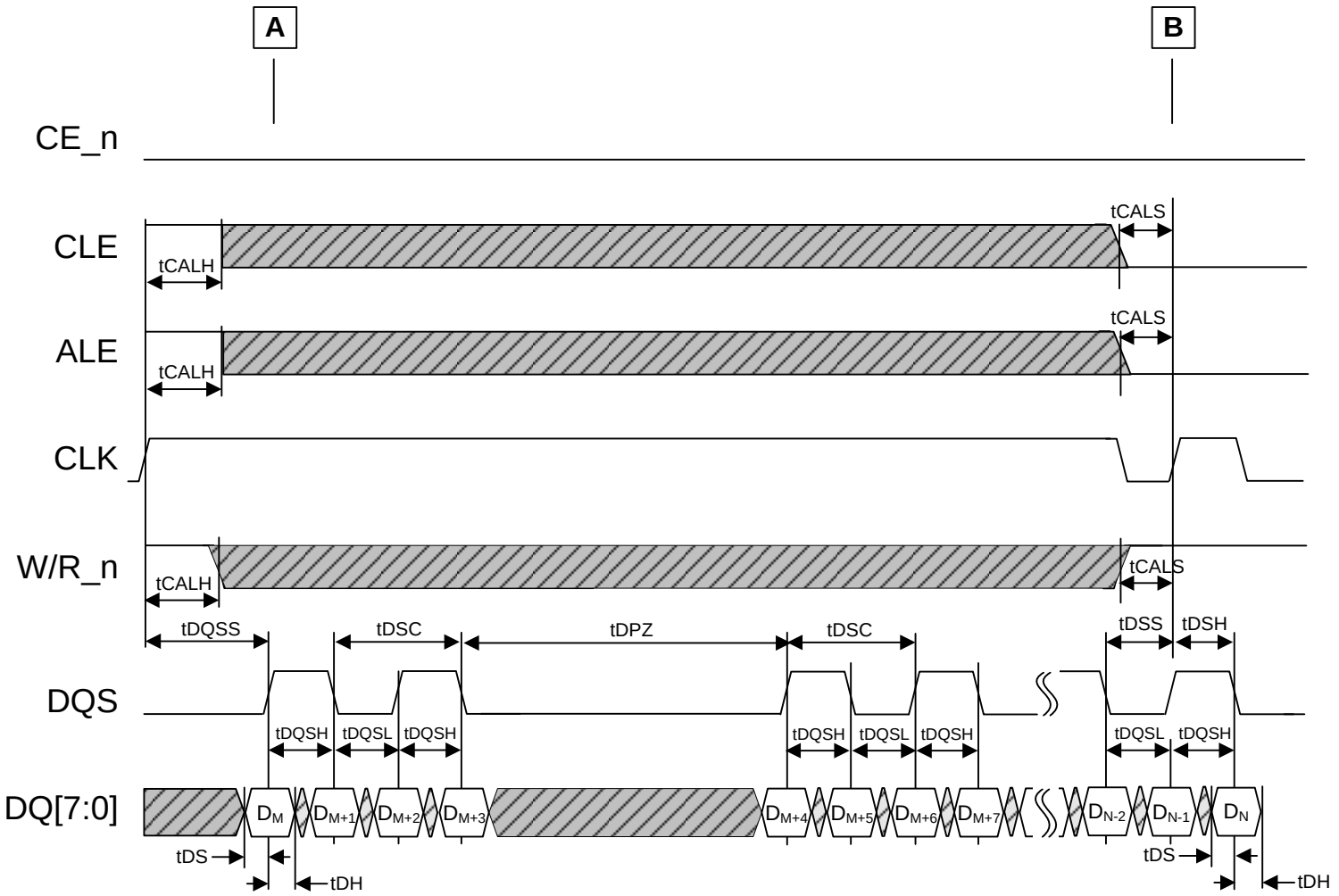


Figure 4-35 Data input cycle timing, CLK stopped with data pause

4.20.2.5. Data Output Cycle Timings

Data output cycle timing describes timing for data transfers from the device to the host (i.e. data reads). The host shall not start data output (i.e. transition ALE/CLE to 11b) until the tDQSD time has elapsed.

For the Read ID, Get Features, Read Status, and Read Status Enhanced commands, the same data byte is repeated twice. The data pattern in this case is D_0 D_0 D_1 D_1 D_2 D_2 etc. The host shall only latch one copy of each data byte.

A calculated parameter, tCKWR, indicates when W/R_n may be transitioned from a zero to one. This parameter is calculated as:

- tCKWR(min) = RoundUp{[tDQSCK(max) + tCK] / tCK}

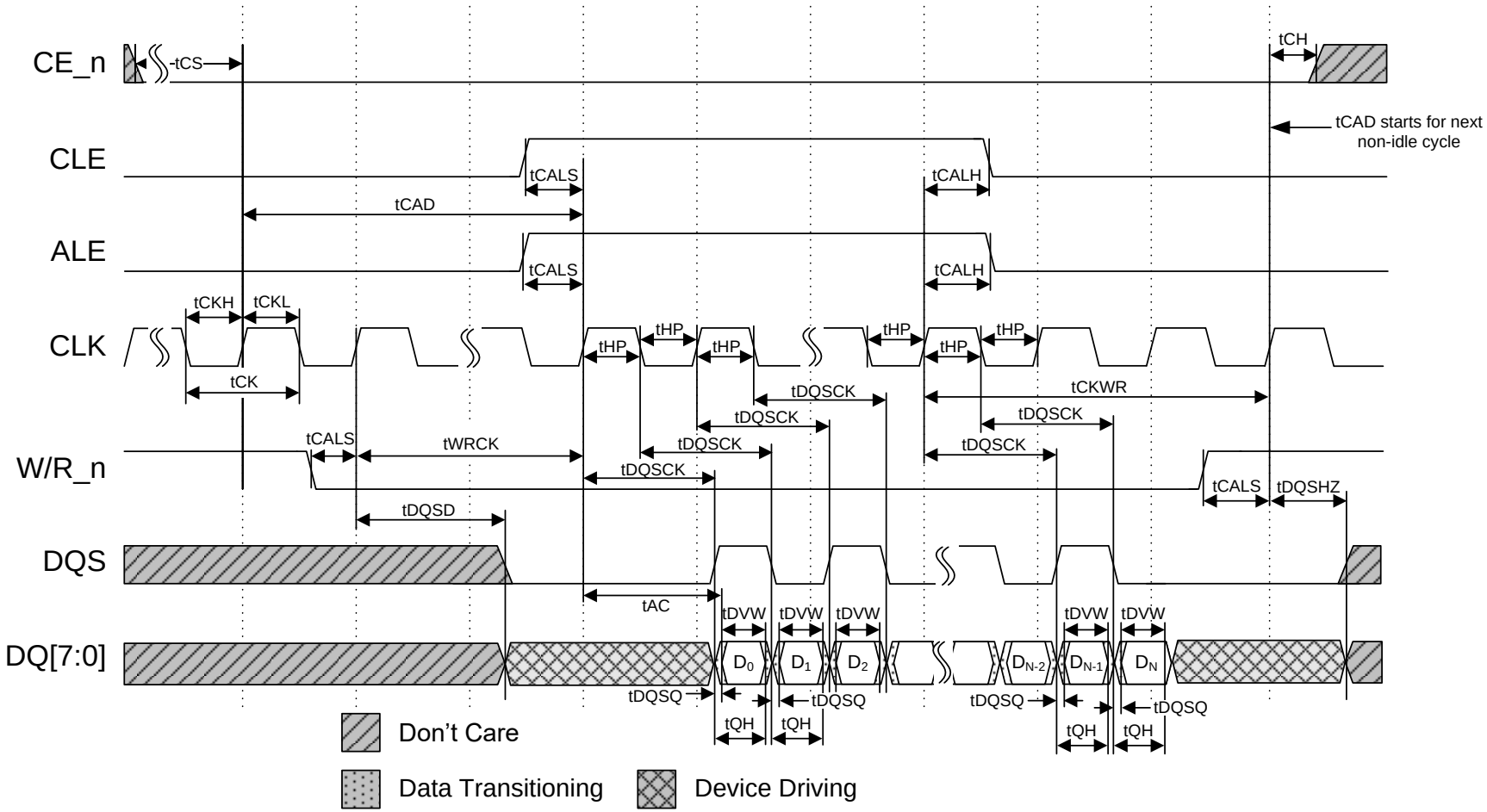


Figure 4-36 Data output cycle timing

4.20.2.6. W/R_n Behavior Timings

Figure 4-37 describes the ownership transition of the DQ bus and DQS signal. The host owns the DQ bus and DQS signal when W/R_n is one. The device owns the DQ bus and DQS signal when W/R_n is zero. The host shall tri-state the DQ bus and DQS signal whenever W/R_n is zero.

When W/R_n transitions from one to zero, the bus ownership is assumed by the device. The host shall tri-state the DQ bus and the DQS signal and the device shall start driving the DQS signal low within tDQSD after the transition of W/R_n to zero. When W/R_n transitions from zero to one, the bus ownership is assumed by the host. The device shall tri-state the DQ bus and DQS signal within tDQSHZ after the transition of W/R_n to one. DQS and the DQ bus should be driven high by the host during idle when no data operations are outstanding and W/R_n is set to one. There is a turn-around time whenever W/R_n changes its value where the DQS signal is tri-stated (as neither the host nor the device is driving the signal), see section 4.20.2.6.

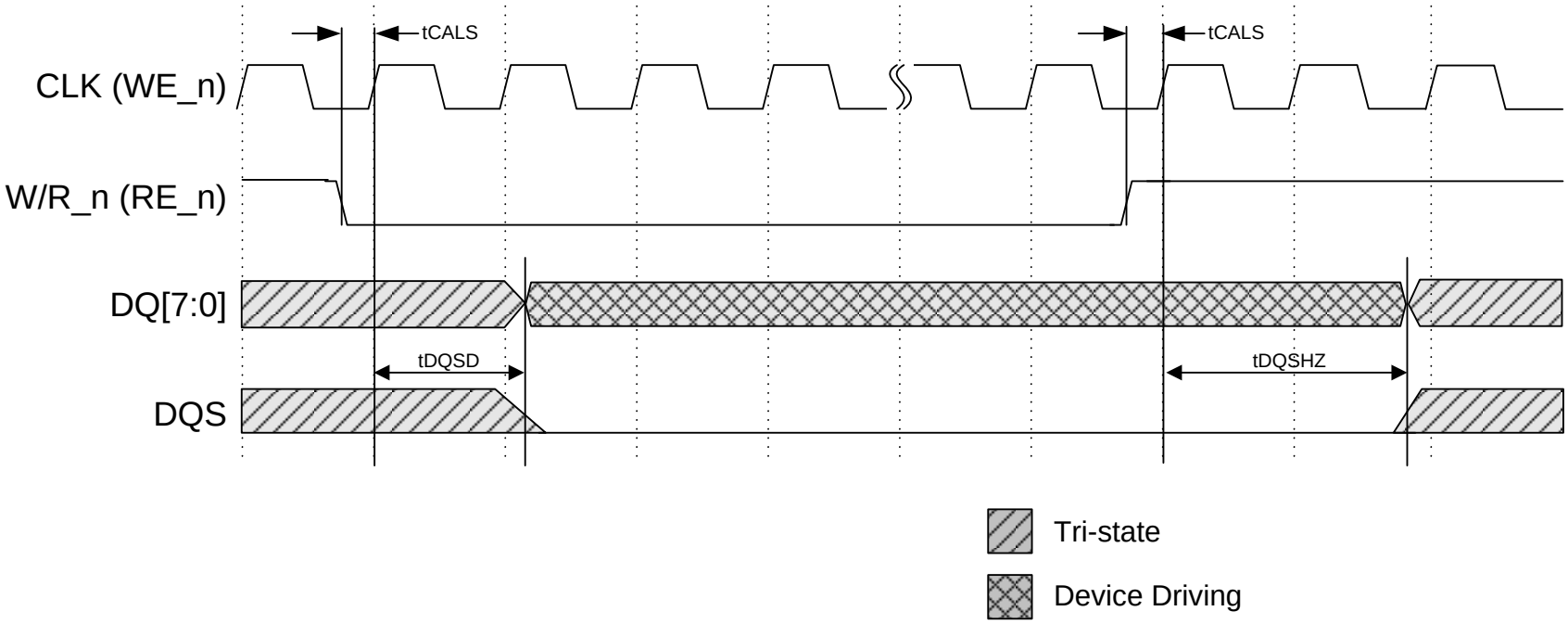


Figure 4-37 W/R_n timing

4.20.2.7. Satisfying Timing Requirements

In some cases, there are multiple timing parameters that shall be satisfied prior to the next phase of a command operation. For example, both tDQSD and tCCS shall be satisfied prior to data output commencing for the Change Write Column command. The host and device shall ensure all timing parameters are satisfied. In cases where tADL, tCCS, tRHW, or tWHR are required, then these are the governing parameters (i.e. these parameters are the longest times).

Figure 4-38 and Figure 4-39 show an example of a Read Status command that includes all the timing parameters for both the command and data phase of the operation. It may be observed that tWHR is the governing parameter prior to the data transfer starting. Also note that the same data byte is transmitted twice (D_0, D_0) for the Read Status command.

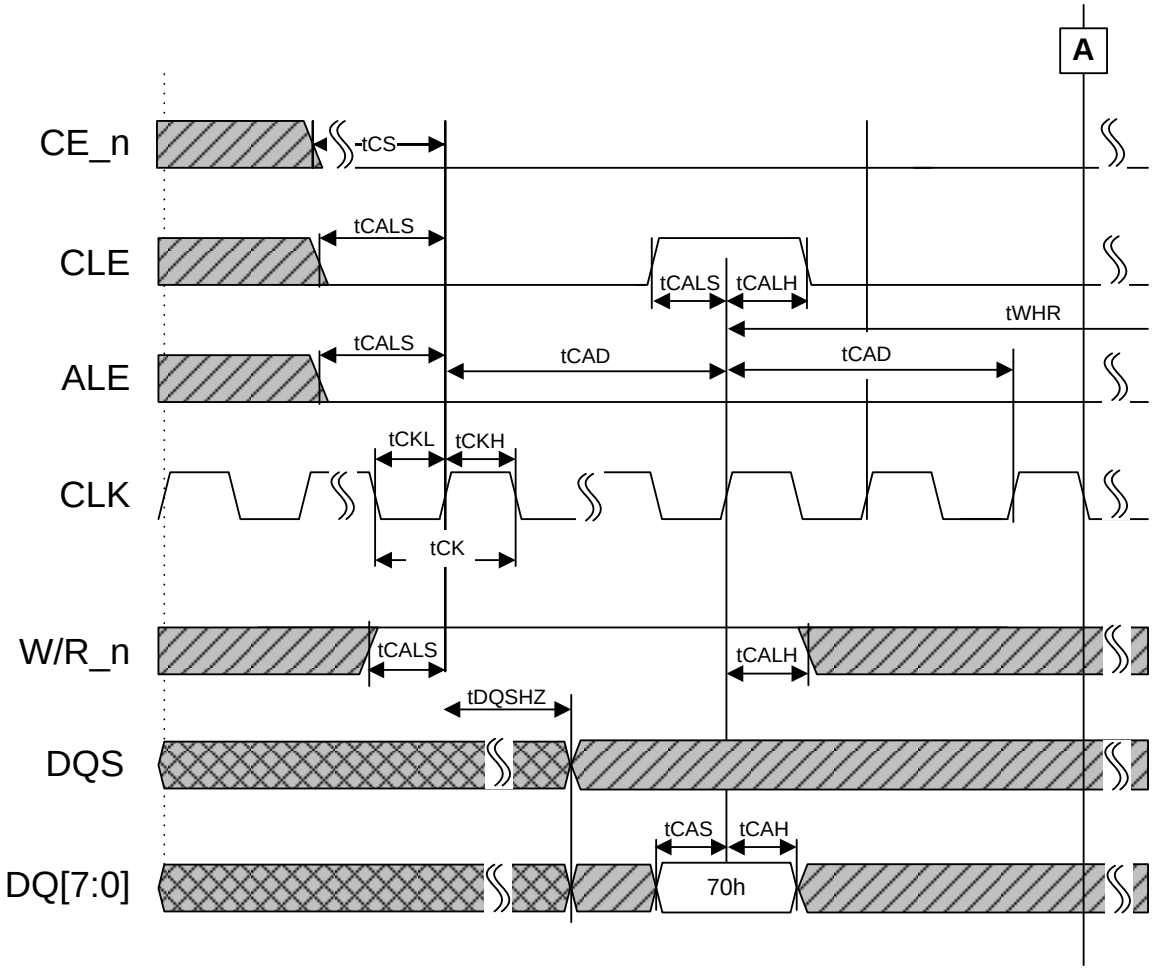


Figure 4-38 Read Status including tWHR and tCAD timing requirements

NOTE:

1. ALE and CLE shall be in a valid state when CE_n transitions from one to zero. In the diagram, it appears that tCS and tCALS are equivalent times. However, tCS and tCALS values are not the same, the timing parameter values should be consulted in Table 4-74.

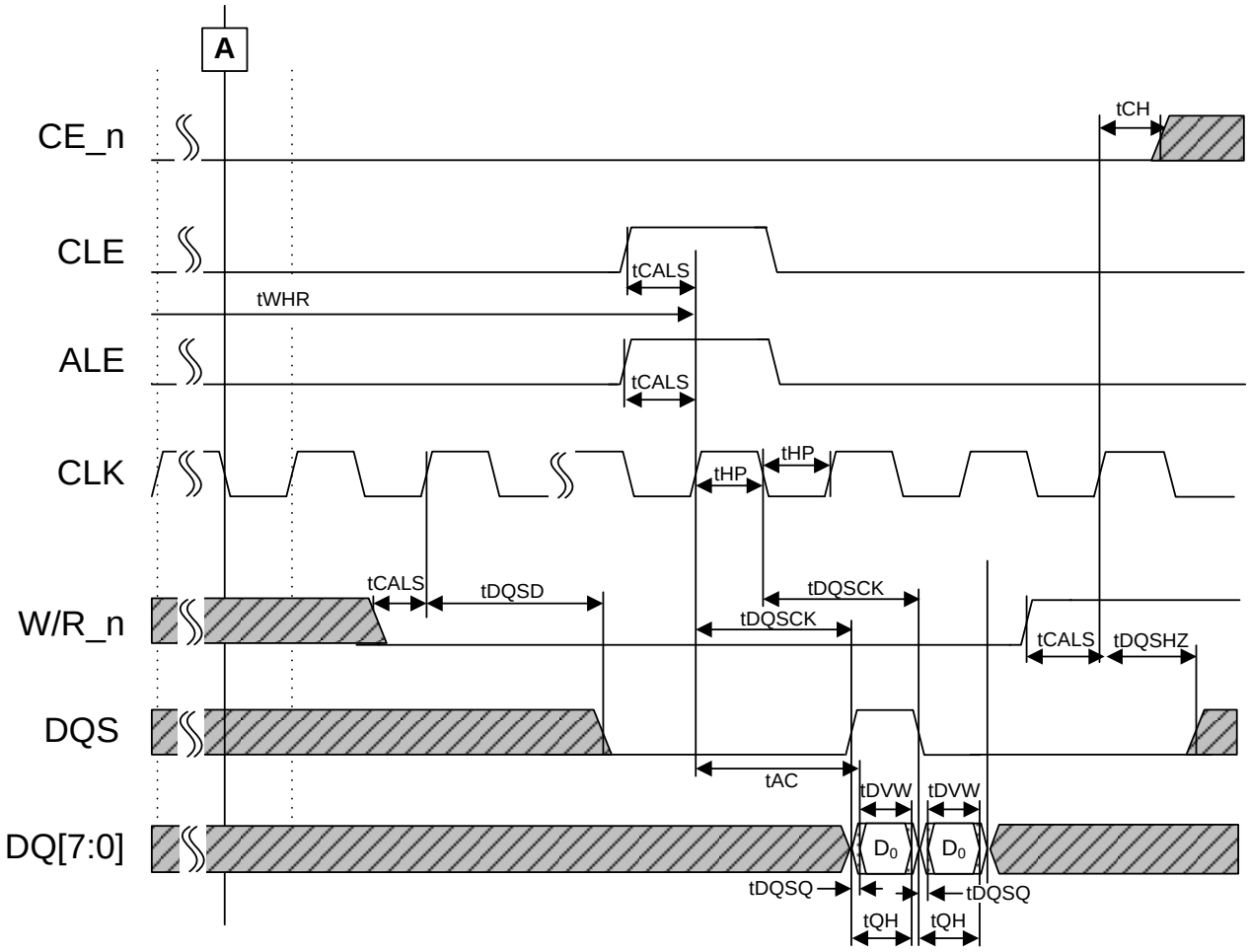


Figure 4-39 Read Status including tWHR and tCAD timing requirements, continued

4.20.3. NV-DDR2/NV-DDR3/NV-LPDDR4

The NV-DDR2 and NV-DDR3 timing diagrams show differential (complementary) signaling being used (RE_t/RE_c and DQS_t/DQS_c). Differential signaling is optional. RE_n and RE_t are the same signal; RE_c is not used when differential signaling is disabled. DQS and DQS_t are the same signal; DQS_c is not used when differential signaling is disabled. For the NV-LPDDR4 interface, differential signaling is always required.

4.20.3.1. Command Cycle Timings

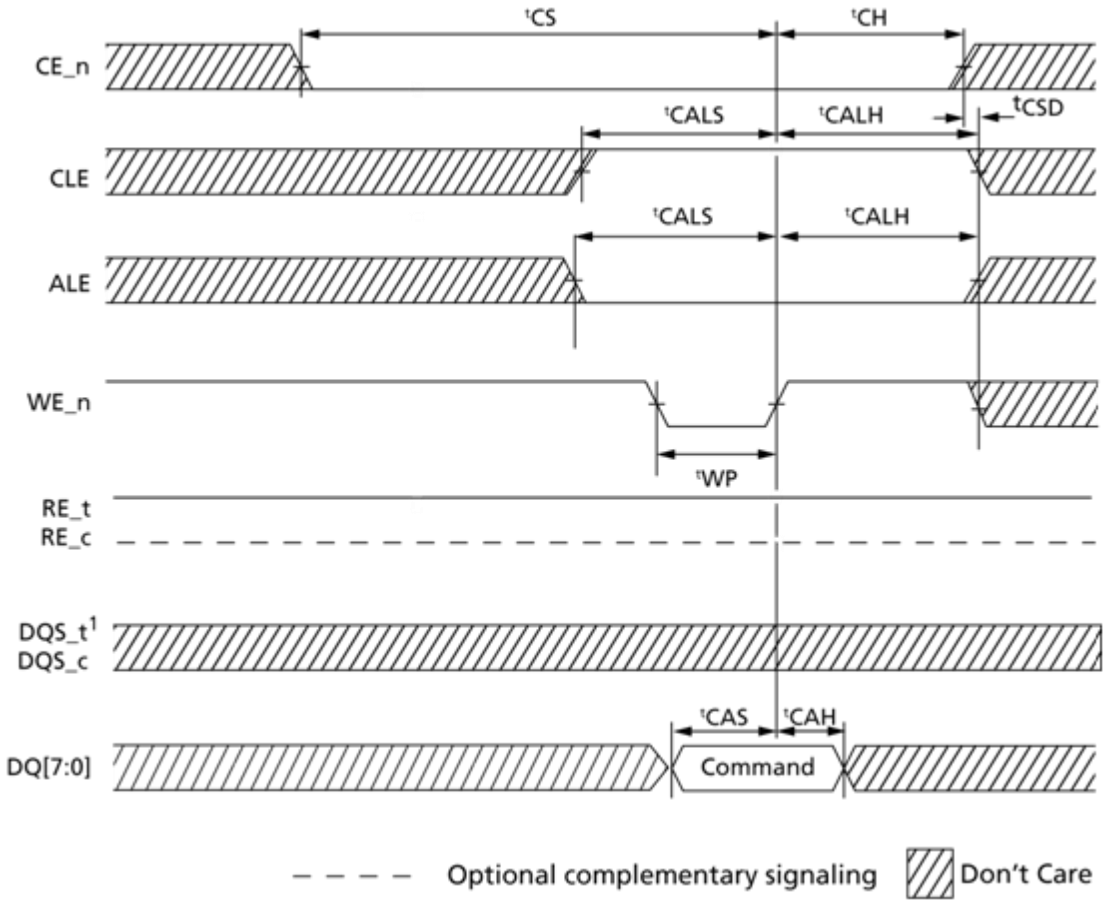


Figure 4-40 Command cycle timings

NOTE: When the bus state is not a data input or data output cycle, if ALE, CLE and CE_n are all low (i.e. Idle state) then DQS (DQS_t) shall be held high by the host to prevent the device from enabling ODT. If ODT is disabled, then DQS is a don't care during Idle states.

4.20.3.2. Address Cycle Timings

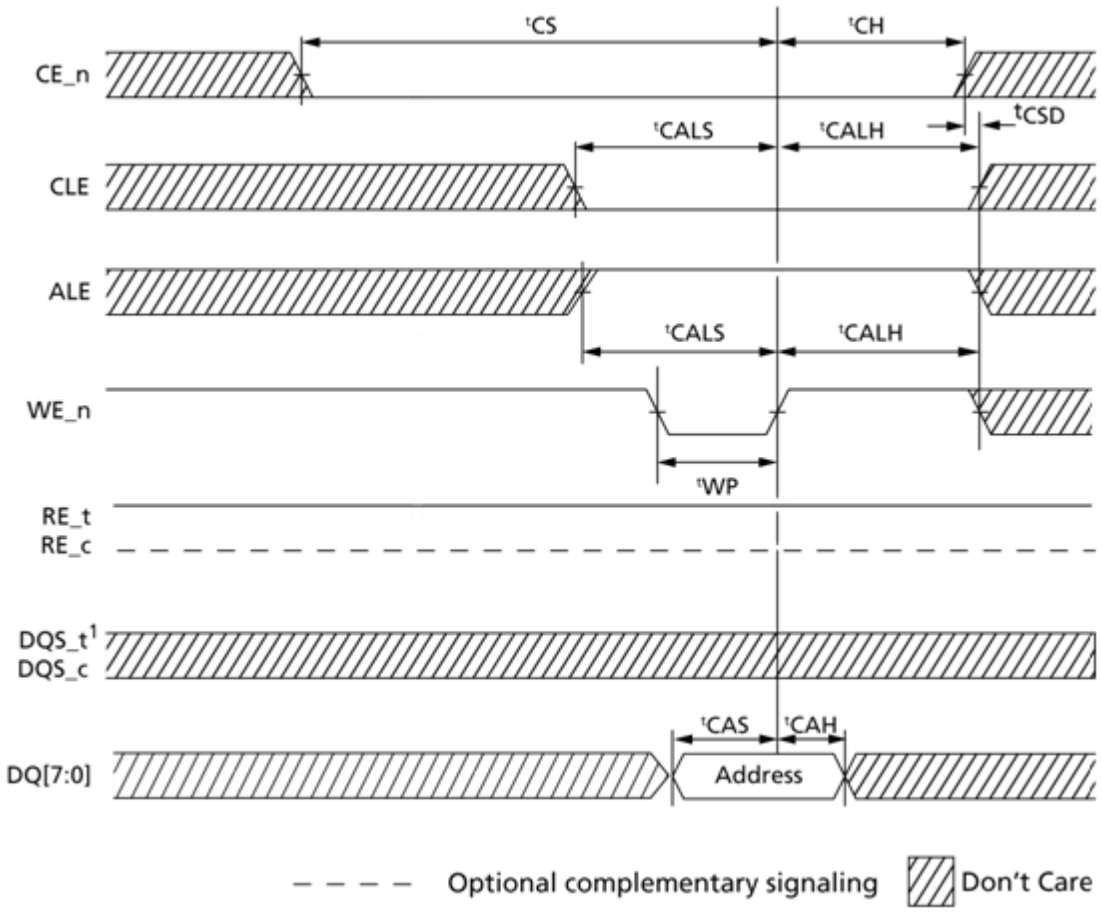


Figure 4-41 Address cycle timings

NOTE: When the bus state is not a data input or data output cycle, if ALE, CLE and CE_n are all low (i.e. Idle state) then DQS (DQS_t) shall be held high by the host to prevent the device from enabling ODT. If ODT is disabled, then DQS is a don't care during Idle states.

4.20.3.3. Data Input Cycle Timings

Data input cycle timing describes timing for data transfers from the host to the device (i.e. data writes).

For the Set Features and ODT Configure command, the same data byte is repeated twice. The data pattern in this case is D_0 D_0 D_1 D_1 D_2 D_2 etc. The device shall only latch one copy of each data byte.

ODT is not required to be used for data input. If ODT is selected for use via Set Features, then ODT is enabled and disabled during the points indicated in Figure 4-42.
Figure 4-43 shows the data input cycle timings, before training is completed.

NOTE:
1. tDBS references the last falling edge of either CLE, ALE or CE_n.
2. To exit the data burst, either CE_n, ALE, or CLE is set to one by the host.
3. Devices that support >1600MT/s on the NV-DDR3 interface may require tCALQS2 and tWPRE2 to be met even when ODT is disabled. See Vendor Datasheet.
4. For the NV-LPDDR4 interface, tCALQS shall not be used and tCALQS2 is required. For the NV-LPDDR4 interface, tWPRE shall not be used and tWPRE2 is required.

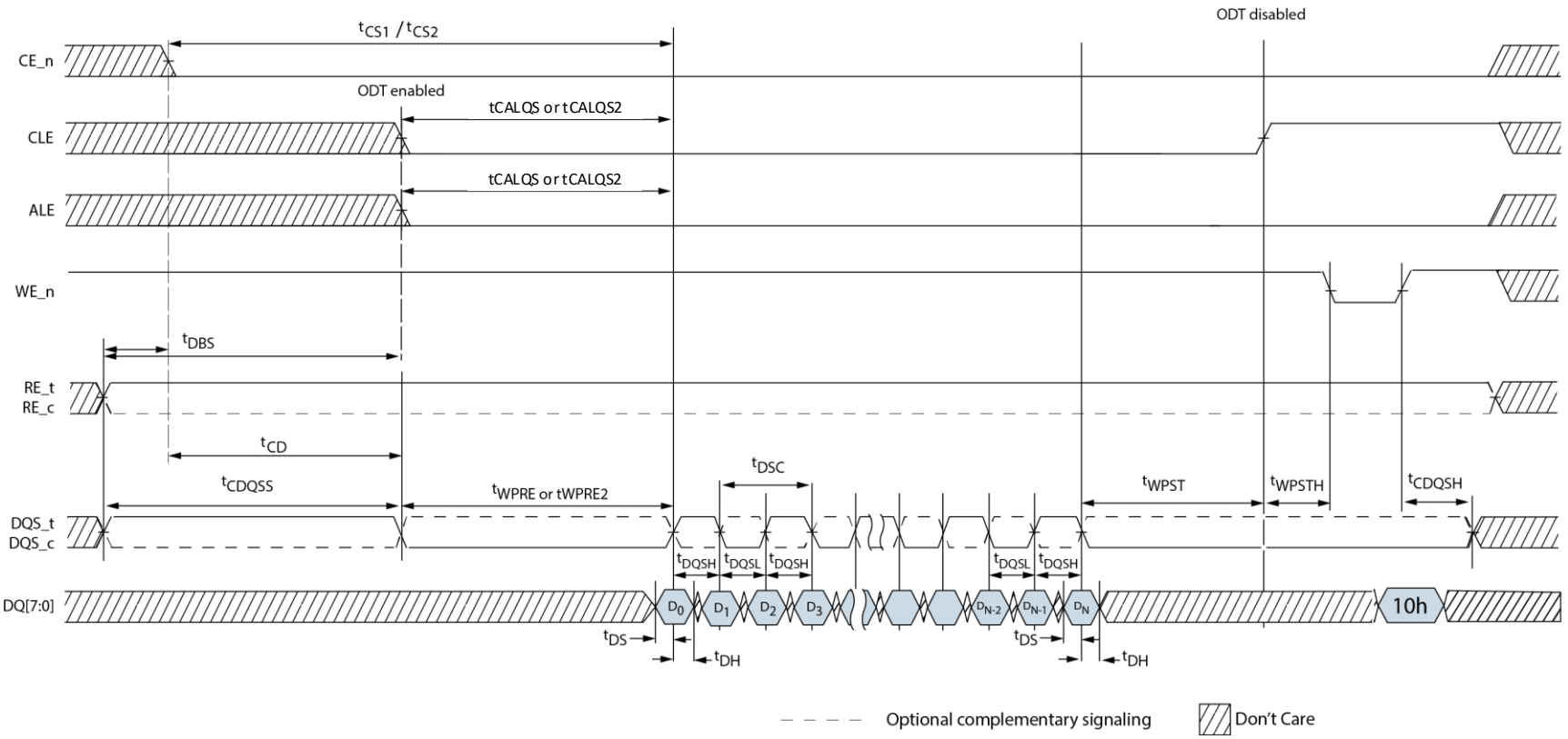


Figure 4-42 Data input cycle timing

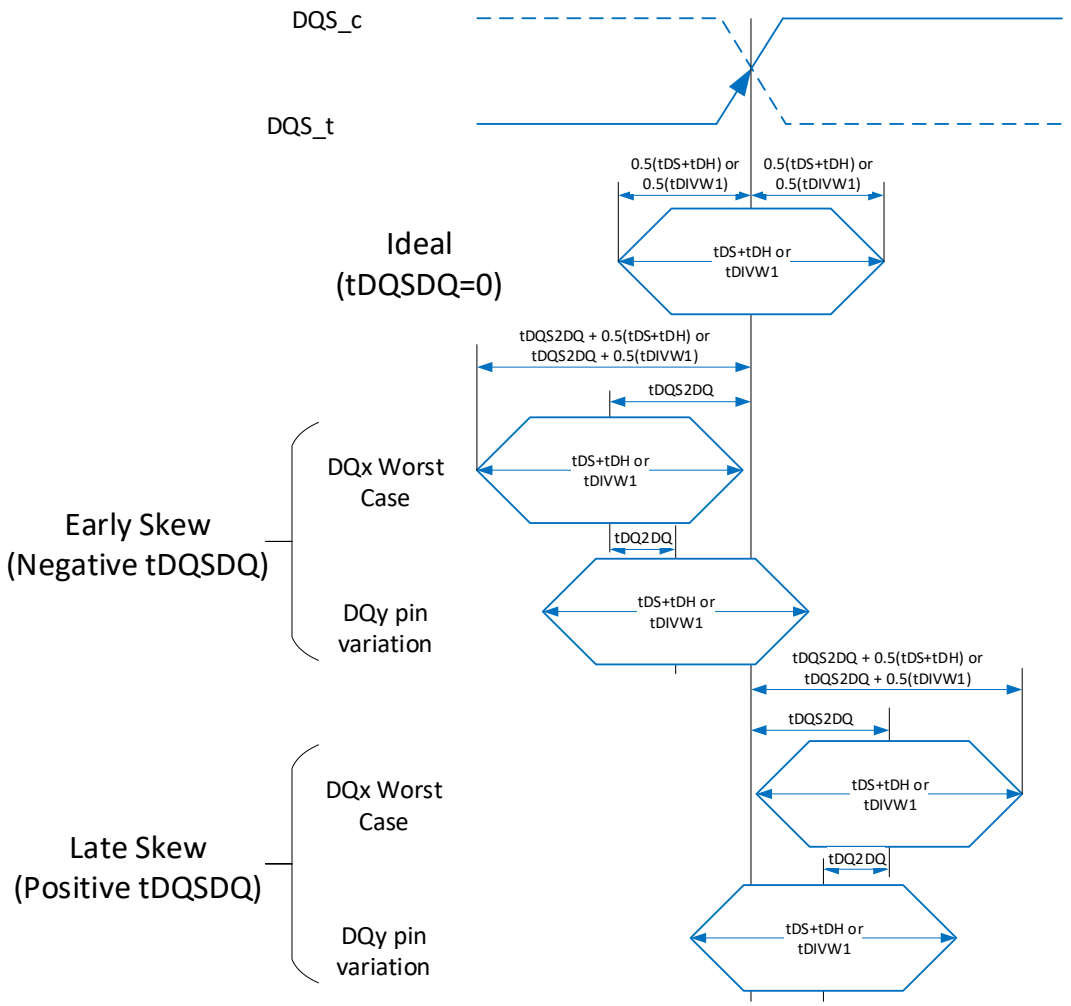


Figure 4-43 Data input cycle timing (before training)

4.20.3.4. Data Output Cycle Timings

Data output cycle timing describes timing for data transfers from the device to the host (i.e. data reads).

For the Read ID, Get Features, Read Status, and Read Status Enhanced commands, the same data byte is repeated twice. The data pattern in this case is D_0 D_0 D_1 D_1 D_2 D_2 etc. The host shall only latch one copy of each data byte.

ODT is not required to be used for data output. If ODT is selected for use via Set Features, then ODT is enabled and disabled during the points indicated in Figure 4-44. If training has completed for data output, Figure 4-45 shows the data output cycle timings.

NOTE:
1. tDBS references the last falling edge of either CLE, ALE or CE_n.
2. To exit the data burst, either CE_n, ALE, or CLE is set to one by the host. tCHZ only applies when CE_n is used to end the data burst.
3. Devices that support >1600MT/s on the NV-DDR3 interface may require tCALR2 and tRPRE2 to be met even when ODT is disabled. See Vendor Datasheet.
4. For the NV-LPDDR4 interface, tCALR shall not be used and tCALR2 is required. For the NV-LPDDR4 interface, tRPRE shall not be used and tRPRE2 is required.

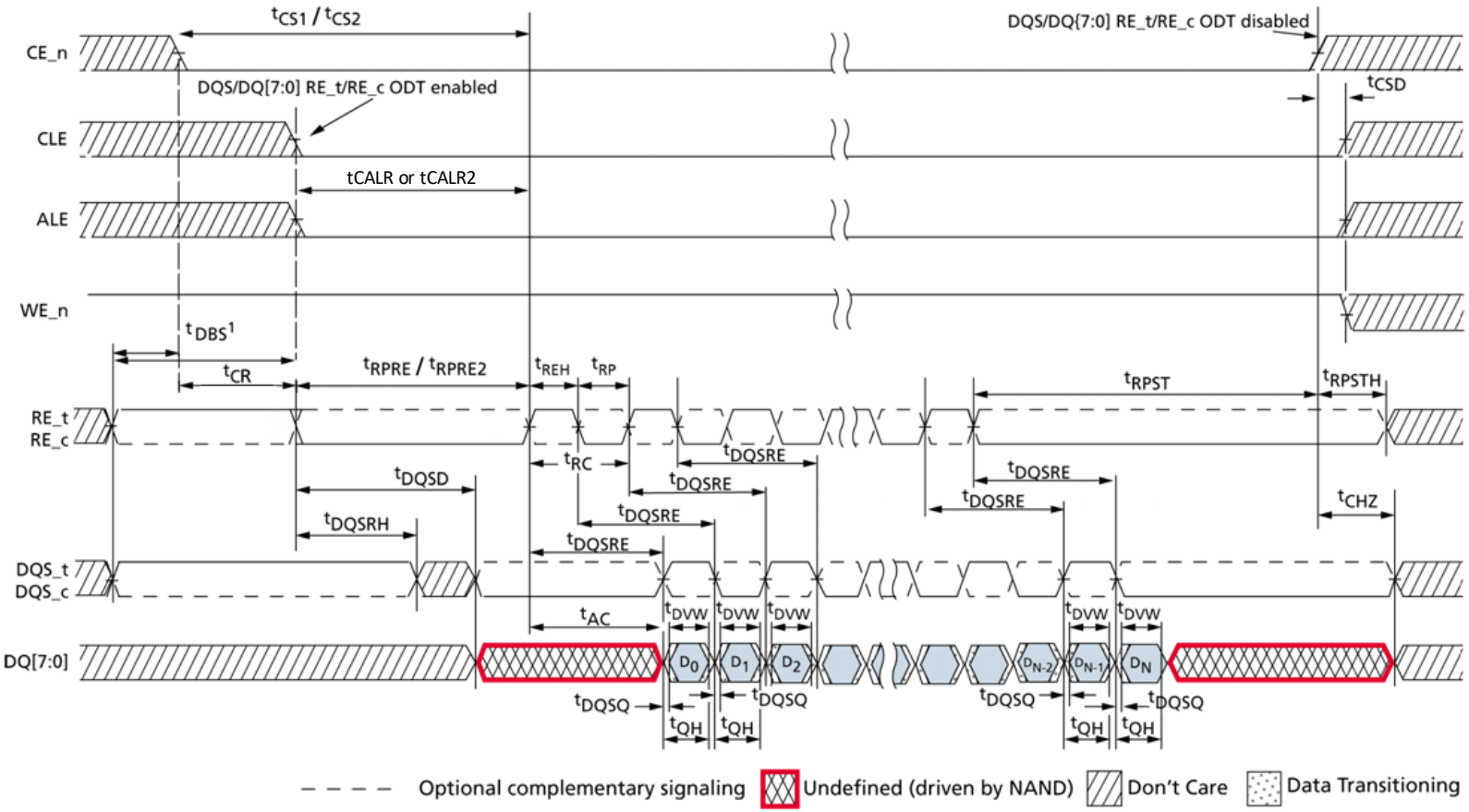


Figure 4-44 Data output cycle timing

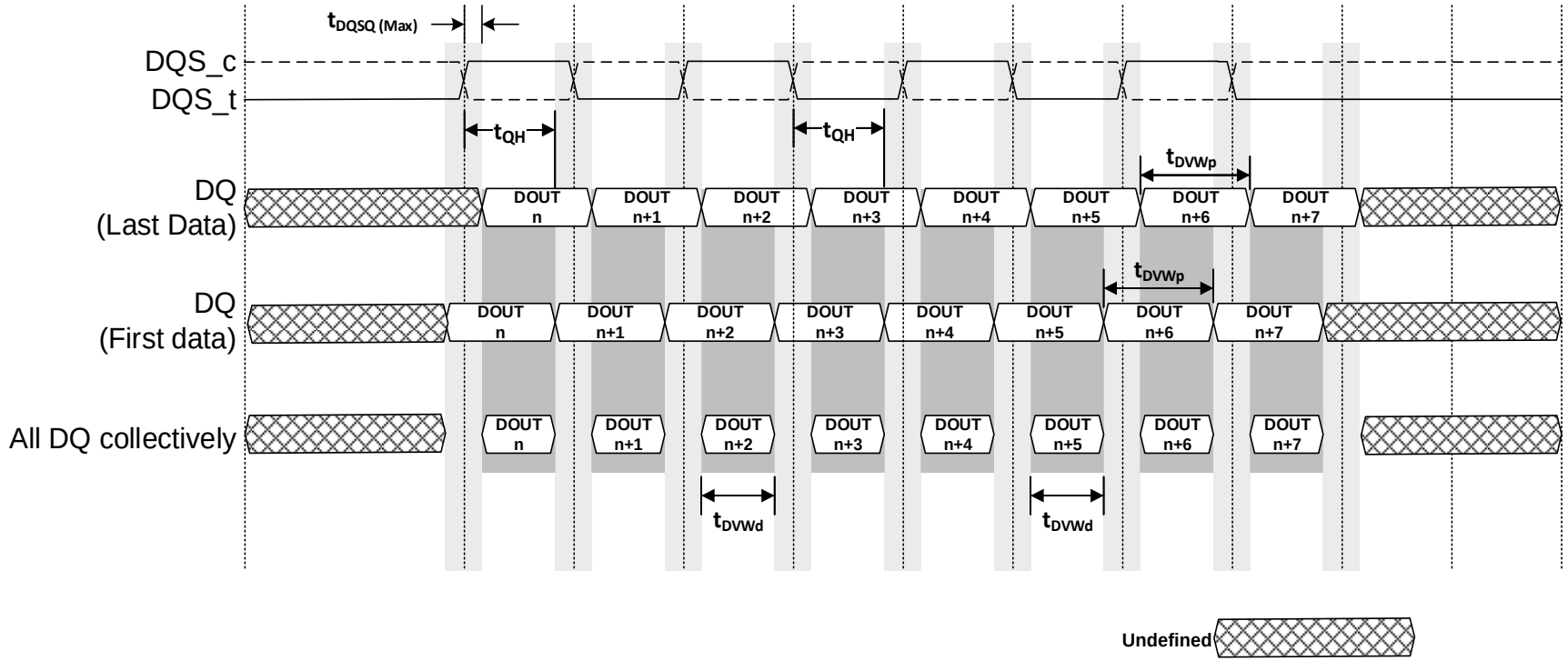


Figure 4-45 Data output valid window timing related specs: tDQSQ, tQH, tDVWd, tDVWp

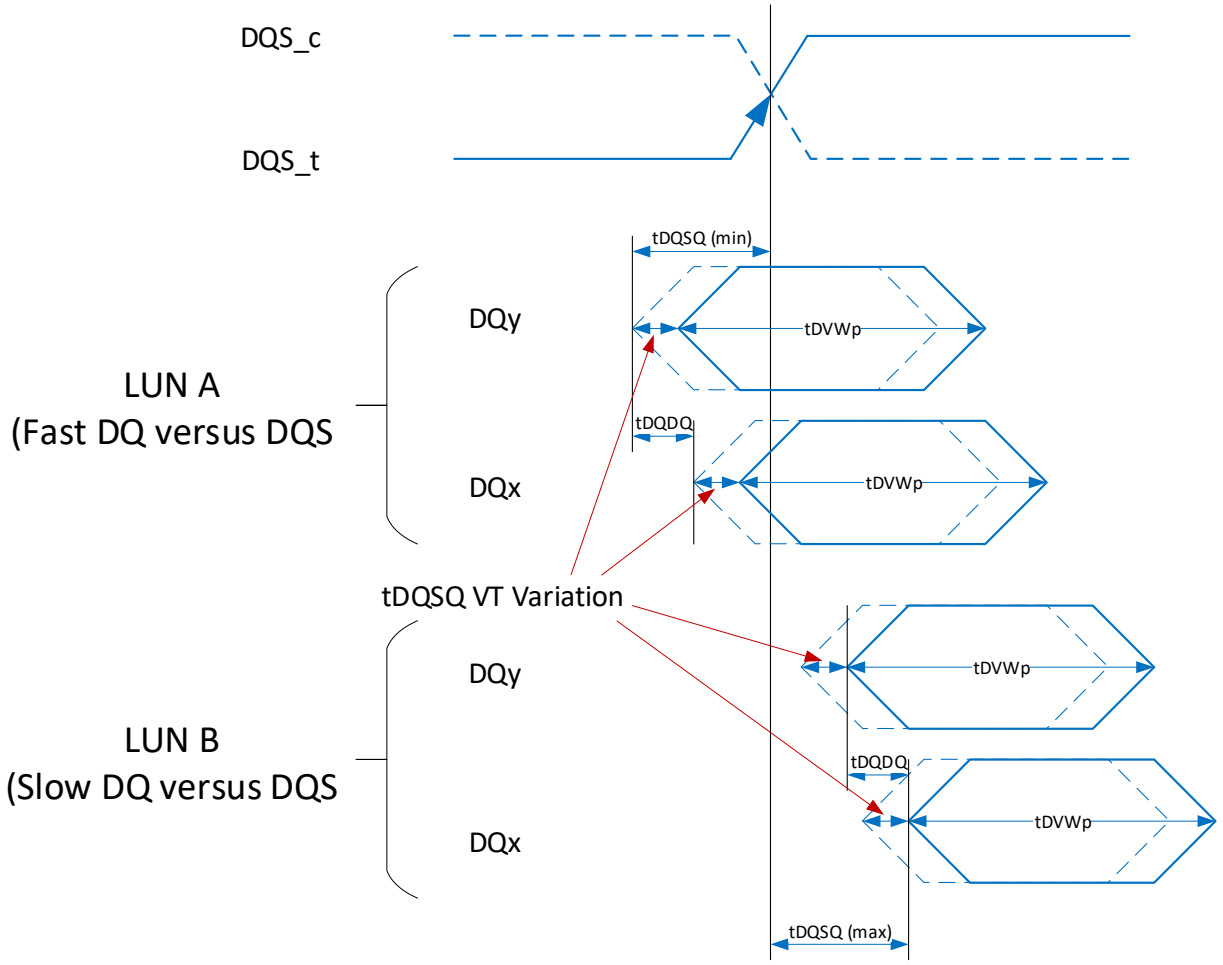


Figure 4-46 Data output valid window timing for >1200MT/s – tDQSQ, tDQDQ, tDVWp parameter

5. Command Definition

5.1. Command Set

Table 5-1 outlines the ONFI command set.

The value specified in the first command cycle identifies the command to be performed. Some commands have a second command cycle as specified in Table 5-1. Typically, commands that have a second command cycle include an address.

Command	O/M	1st Cycle	2nd Cycle	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy	Target level commands
Read	M	00h	30h		Y	
Multi-plane	O	00h	32h		Y	
Copyback Read	O	00h	35h		Y	
Change Read Column	M	05h	E0h		Y	
Change Read Column Enhanced	O	06h	E0h		Y	
Read Cache Random	O	00h	31h		Y	
ODT Disable	O	1Bh		Y	Y	Y
ODT Enable	O	1Ch		Y	Y	Y
Read Cache Sequential	O	31h			Y	
Read Cache End	O	3Fh			Y	
Block Erase	M	60h	D0h		Y	
Multi-plane	O	60h	D1h		Y	
Read Status	M	70h		Y	Y	
Read Status Enhanced	O	78h		Y	Y	
Page Program	M	80h	10h		Y	
Multi-plane	O	80h	11h		Y	
Page Cache Program	O	80h	15h		Y	
Copyback Program	O	85h	10h		Y	
Multi-plane	O	85h	11h		Y	
Small Data Move[2]	O	85h	11h		Y	
Change Write Column[1]	M	85h			Y	
Change Row Address[1]	O	85h			Y	
Read ID	M	90h				Y
Volume Select[3]	O	E1h		Y	Y	
ODT Configure[3]	O	E2h				
Read Parameter Page	M	ECh				Y
Read Unique ID	O	EDh				Y
Get Features	O	EEh				Y
Set Features	O	EFh				Y
Command Based DCC Training	O	18h				
Read DQ Training	M	62h				
Write TX DQ Training Pattern	M	63h				
Write TX DQ Training Readback	M	64h				
Write RX DQ Training	O	76h				
LUN Get Features	O	D4h			Y	
LUN Set Features	O	D5h			Y	
ZQ Calibration Short	O	D9h			Y	
ZQ Calibration Long	O	F9h			Y	
Reset LUN	O	FAh		Y	Y	
Synchronous Reset	O	FCh		Y	Y	Y
Reset	M	FFh		Y	Y	Y

NOTE:
1. Change Write Column specifies the column address only. Change Row Address specifies the row address and the column address. Refer to the specific command definitions.
2. Small Data Move's first opcode may be 80h if the operation is a program only with no data output. For the last second cycle of a Small Data Move, it is a 10h command to confirm the Program or Copyback operation.
3. Volume Select shall be supported if the device supports either CE_n pin reduction or matrix termination. ODT Configure shall be supported if the device supports matrix termination.

Table 5-1 Command set

Reserved opcodes shall not be used by the device, as the ONFI specification may define the use of these opcodes in a future revision. Vendor specific opcodes may be used at the discretion of the vendor and shall never be defined for standard use by ONFI.

Type	Opcode
Standard Command Set	00h, 05h – 06h, 10h – 11h, 15h, 18h, 30h – 32h, 35h, 3Fh, 60h, 62h – 64h, 70h, 76h, 78h, 80h – 81h, 85h, 90h, 1Bh – 1Ch, D0h – D1h, D4h – D5h, D9h, E0h –E2h, ECh – EFh, F1h – F2h, F9h, FAh, FCh, FFh
Vendor Specific	01h – 04h, 07h – 0Ah, 0Ch – 0Fh, 13h, 16h – 17h, 19h – 1Ah, 1Dh – 2Fh, 33h – 34h, 36h – 3Eh, 40h – 5Fh, 61h, 65h – 6Fh, 71h – 75h, 77h, 79h – 7Fh, 84h, 87h – 8Dh, 8Fh, 91h – CFh, D2h – D3h, D6h – D8h, DAh – DFh, E3h – EBh, F0h, F3h – F8h, FBh, FD – FEh
Reserved	0Bh, 12h, 14h, 82h – 83h, 86h, 8Eh

Table 5-2 Opcode Reservations

5.2. Command Descriptions

The command descriptions in section 5 are shown in a format that is agnostic to the data interface being used (when the command may be used in either data interface). An example of the agnostic command description for Change Write Column is shown in Figure 5-1. The agnostic command examples shall be translated to a command description for the particular data interface selected. The command description for Change Write Column in the SDR data interface is shown in Figure 5-2. The command description for Change Write Column in the NV-DDR data interface is shown in Figure 5-3. The command description for Change Write Column in the NV-DDR2/3 and NV-LPDDR4 data interface is shown in Figure 5-4. Note that the timing parameters defined in section 4 shall be observed for each command (e.g. the tCAD timing parameter for the NV-DDR data interface).

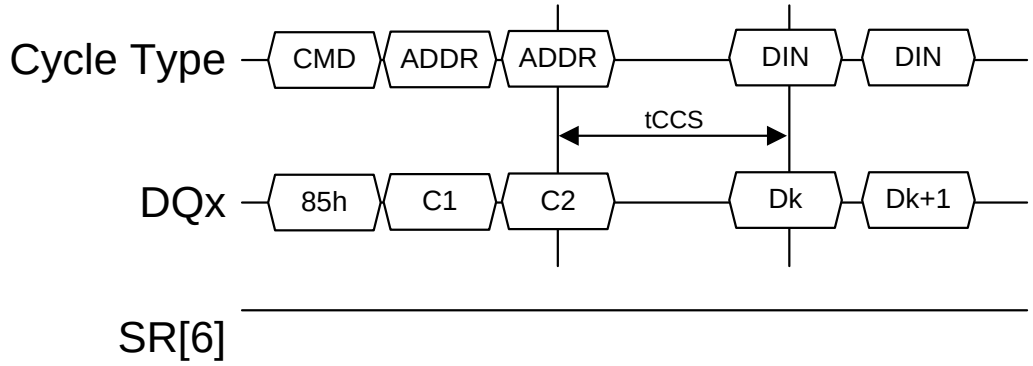


Figure 5-1 Agnostic command description

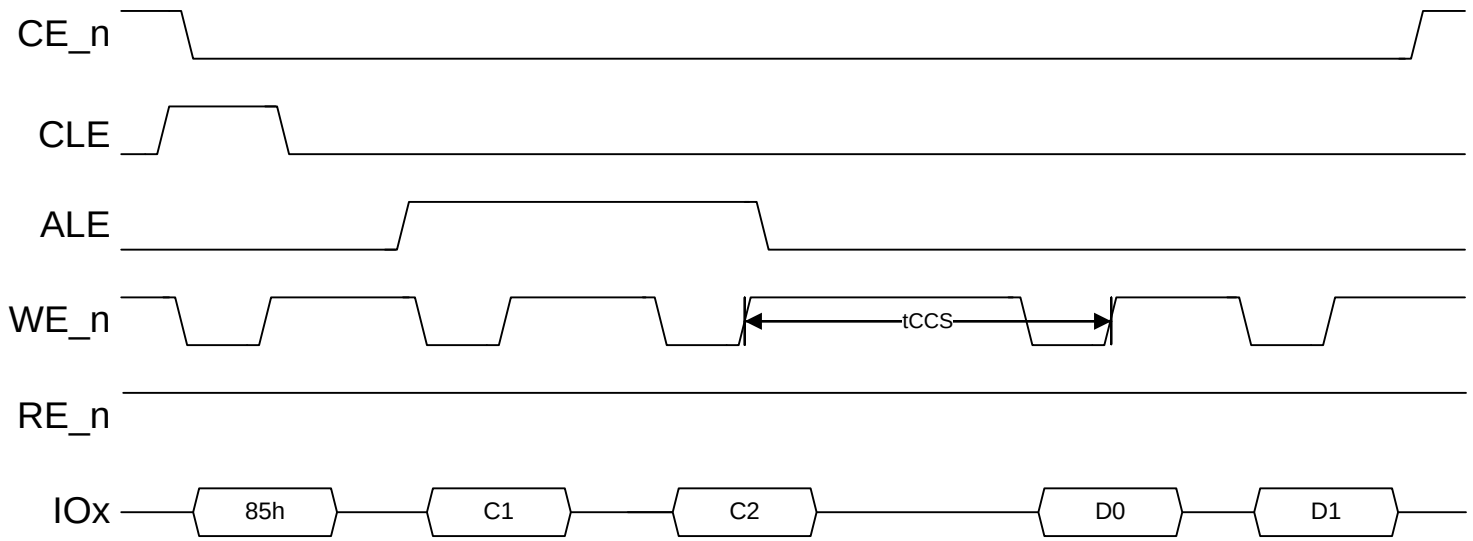


Figure 5-2 SDR data interface command description

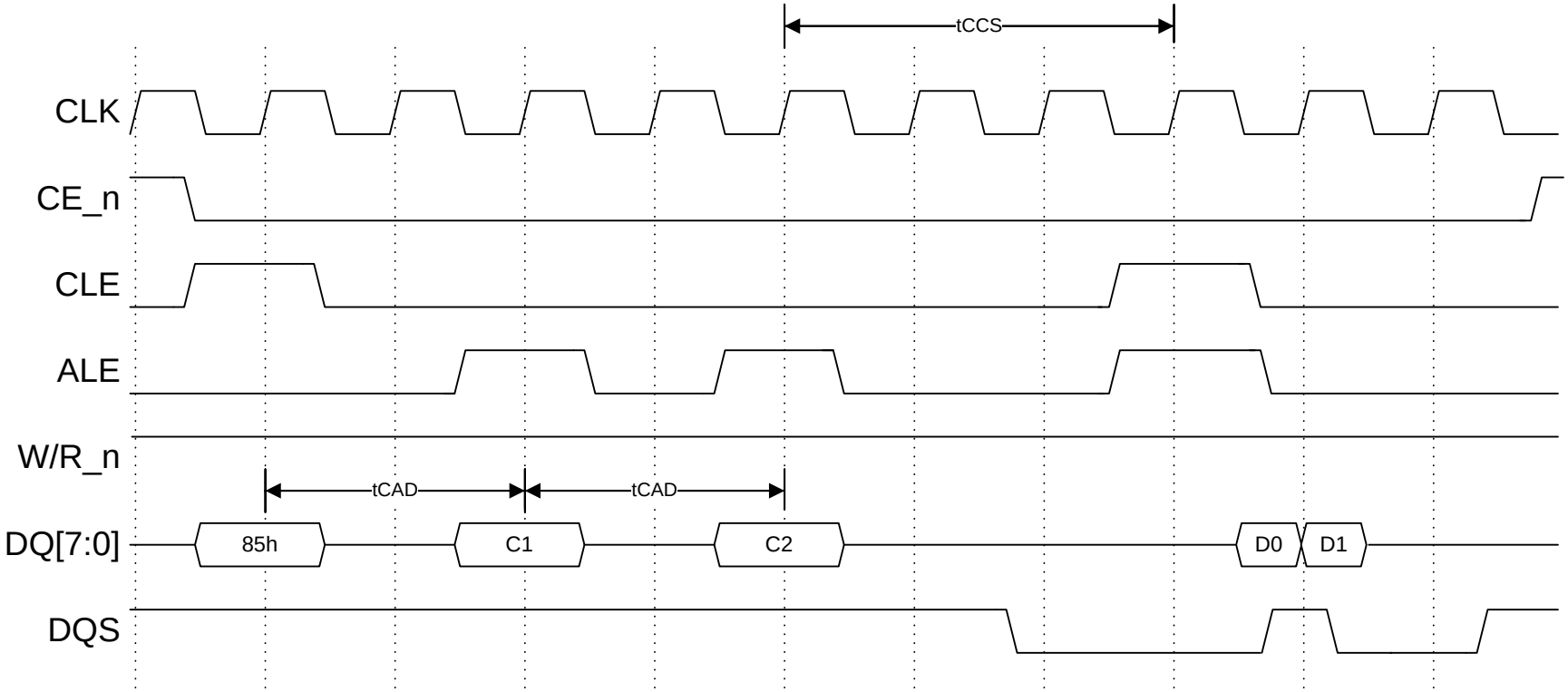


Figure 5-3 NV-DDR data interface command description

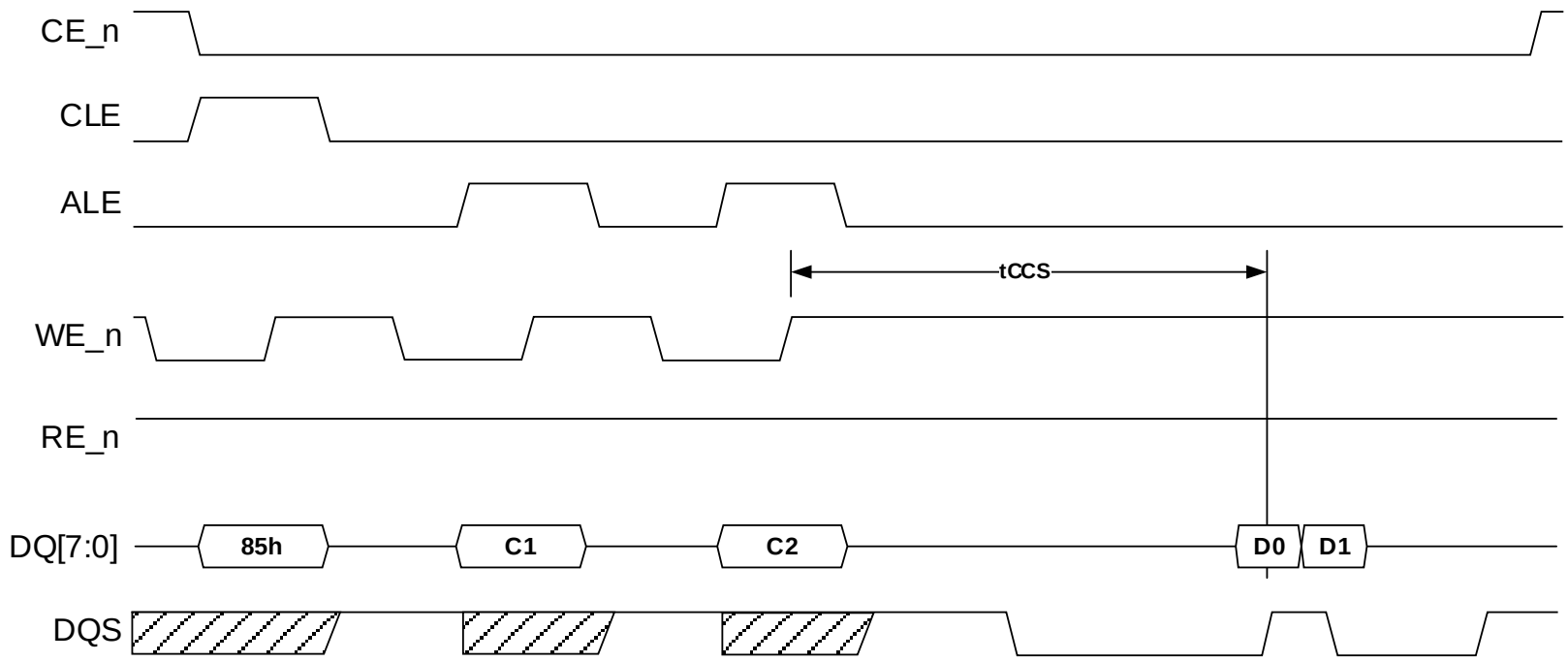


Figure 5-4 NV-DDR2, NV-DDR3 and NV-LPDDR4 data interface command description

NOTE:

1. When the bus state is not a data input or data output cycle, if ALE, CLE and CE_n are all low (i.e. Idle state) then DQS (DQS_t) shall be held high by the host to prevent the device from enabling ODT. If ODT is disabled, then DQS is a don't care during Idle states.
2. Differential signaling (use of DQS_c and RE_c) is required for the NV-LPDDR4 interface.

5.3. Reset Definition

The Reset function puts the target in its default power-up state and if issued when configured to NV-DDR or NV-DDR2 interface places the target in the SDR data interface. The R/B_n value is unknown when Reset is issued; R/B_n is guaranteed to be low tWB after the Reset is issued.

Note that some feature settings are retained across Reset commands (as specified in section 5.31). As part of the Reset command, all LUNs are also reset. The command may be executed with the target in any state, except during power-on when Reset shall not be issued until R/B_n is set to one. Figure 5-5 defines the Reset behavior and timings.

If issued when configured in the NV-DDR3 data interface, the target shall remain in the NV-DDR3 data interface following this command. If issued when configured in the NV-LPDDR4 data interface, the target shall remain in the NV-LPDDR4 data interface following this command.

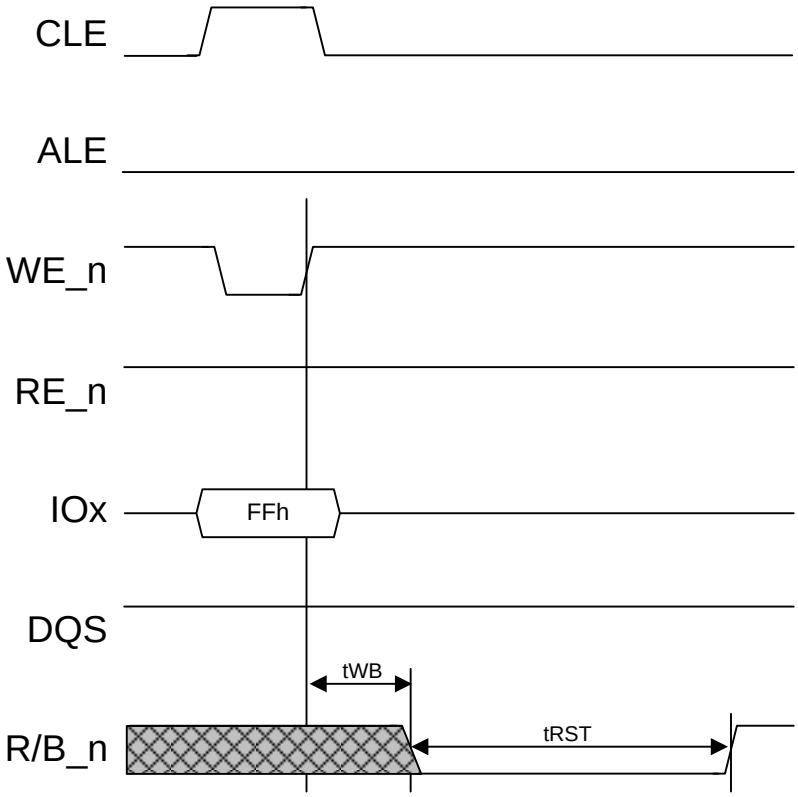


Figure 5-5 Reset timing diagram

5.4. Synchronous Reset Definition

The Synchronous Reset command resets the target and all LUNs. The command may be executed with the target in any state. Figure 5-6 defines the Synchronous Reset behavior and timings. The R/B_n value is unknown when Synchronous Reset is issued; R/B_n is guaranteed to be low tWB after the Synchronous Reset is issued.

This command is optional and may be supported by devices that support the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interfaces. This command is only accepted when using

the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface. The host should not issue this command when the device is configured to the SDR data interface. The target shall remain in the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface following this command.

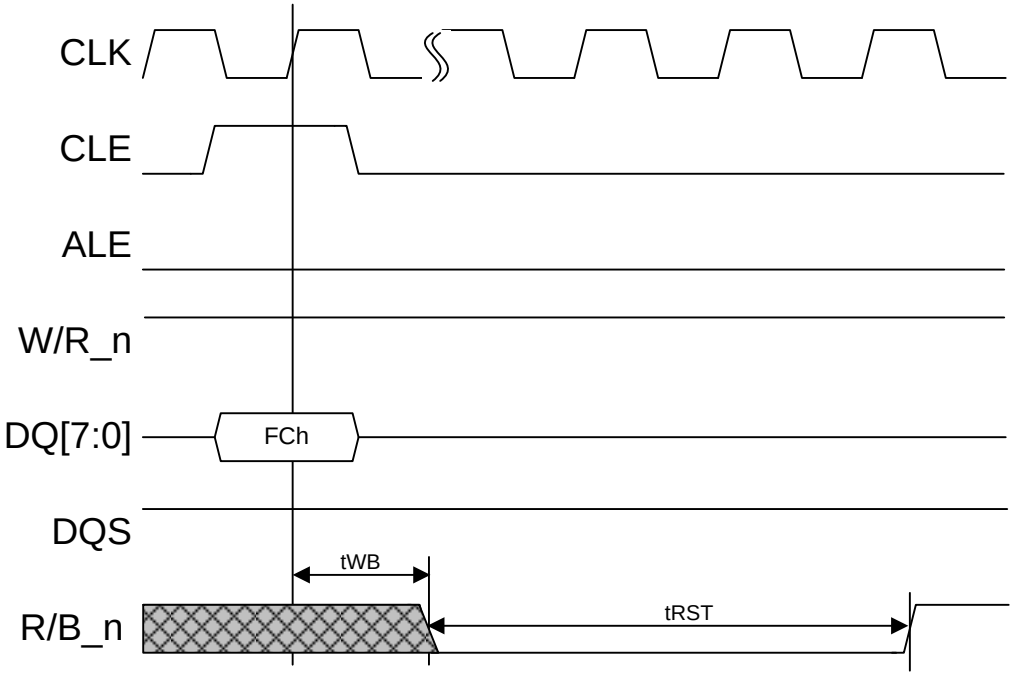


Figure 5-6 Synchronous Reset timing diagram

5.5. Reset LUN Definition

The Reset LUN command is used to reset a particular LUN. This command is accepted by only the LUN addressed as part of the command. The command may be executed with the LUN in any state. Figure 5-7 defines the Reset LUN behavior and timings. The SR[6] value is unknown when Reset LUN is issued; SR[6] is guaranteed to be low tWB after the Reset LUN command is issued. This command does not affect the data interface configuration for the target.

Reset LUN should be used to cancel ongoing command operations, if desired. When there are issues with the target, e.g. a hang condition, the Reset (FFh) or Synchronous Reset (FCh) commands should be used.

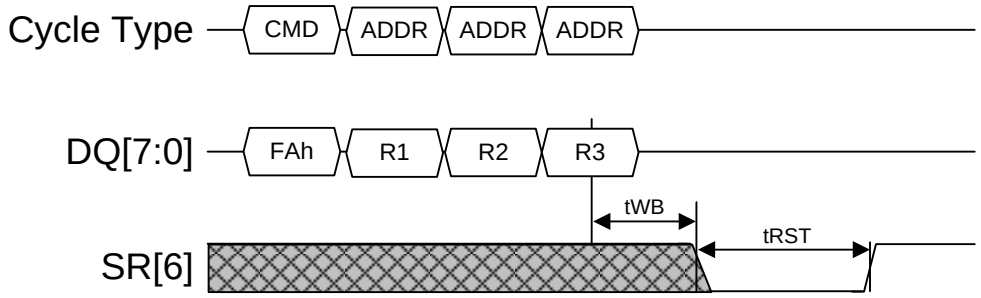


Figure 5-7 Reset LUN timing diagram

5.6. Read ID Definition

The Read ID function identifies that the target supports the ONFI specification. If the target supports the ONFI specification, then the ONFI signature shall be returned. The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. For devices prior to ONFI 4.0, reading beyond four bytes yields indeterminate values. Figure 5-8 defines the Read ID behavior and timings.

Definition for 5th and 6th byte of Read ID was added for ONFI 4.0. The 5th byte is used to identify that the device has powered up in the NV-DDR3 interface.

When issuing Read ID in the NV-DDR, NV-DDR2 NV-DDR3 or NV-LPDDR4 data interface, each data byte is received twice. The host shall only latch one copy of each data byte. See section 4.4.

For the Read ID command, only addresses of 00h and 20h are valid. To retrieve the ONFI signature an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature).

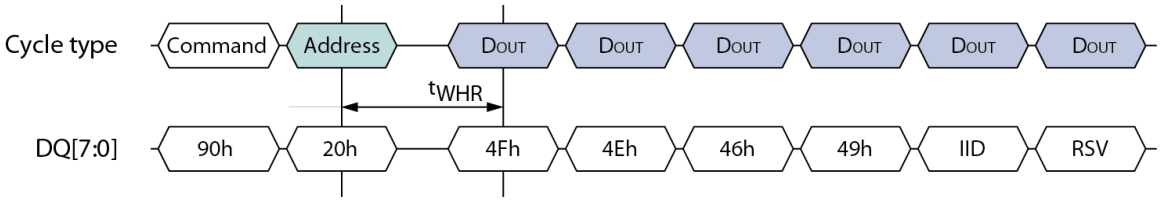


Figure 5-8 Read ID timing diagram for ONFI signature

IID	Power on Interface ID, 01h for NV-DDR3, 00h for SDR
RSV	6th byte is reserved for future use

The Power on Interface ID is set only once per power cycle and does not change. If the device exits power-on reset (FFh) with the SDR or NV-DDR3 power on interface active, issuing SET FEATURES (EFh) to change the interface will not change the IID value.

The Read ID function can also be used to determine the JEDEC manufacturer ID and the device ID for the particular NAND part by specifying an address of 00h. Figure 5-9 defines the Read ID behavior and timings for retrieving the JEDEC manufacturer ID and device ID. Reading beyond the first two bytes yields values as specified by the manufacturer.

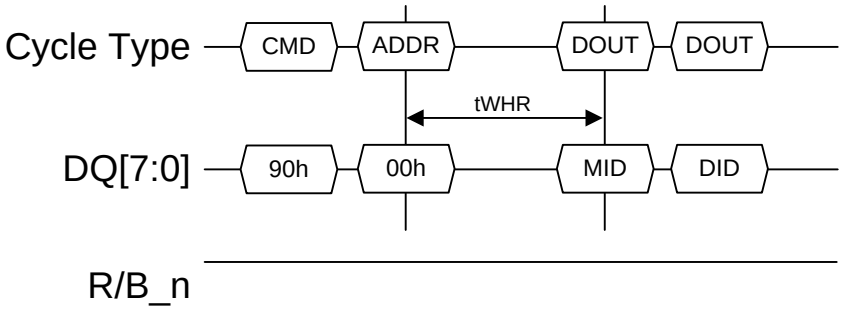


Figure 5-9 Read ID timing diagram for manufacturer ID

MID Manufacturer ID for manufacturer of the part, assigned by JEDEC.

DID Device ID for the part, assigned by the manufacturer.

The Read ID command may be issued using either the SDR, NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interfaces. The timing parameters for each data interface are shown in Figure 5-10, Figure 5-11, and Figure 5-12.

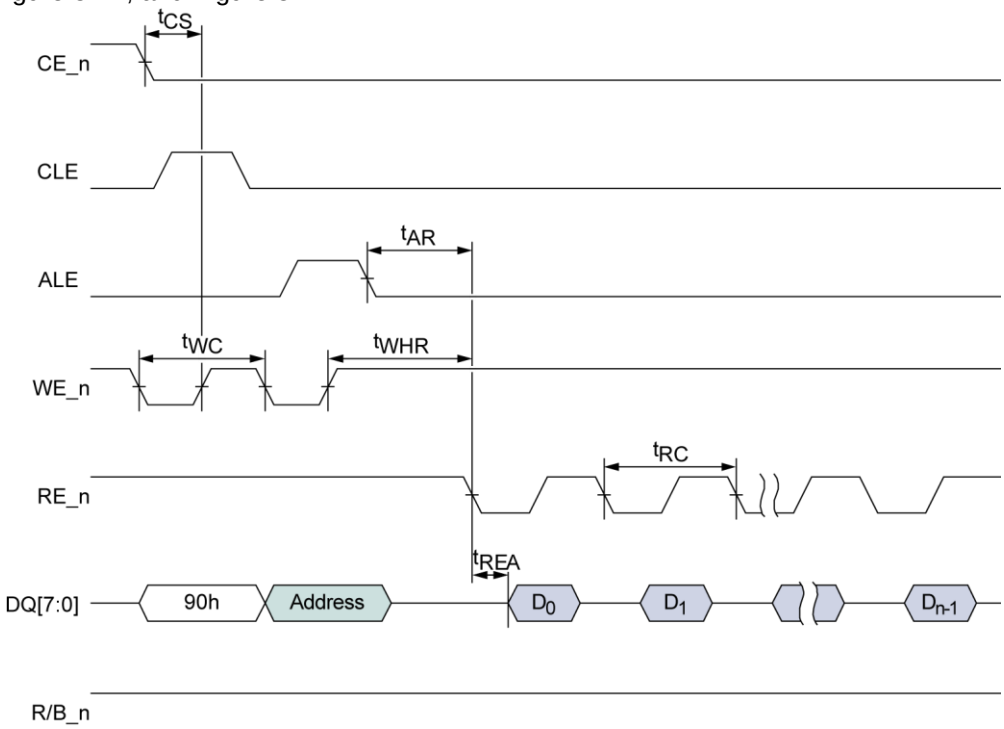


Figure 5-10 Read ID command using SDR data interface

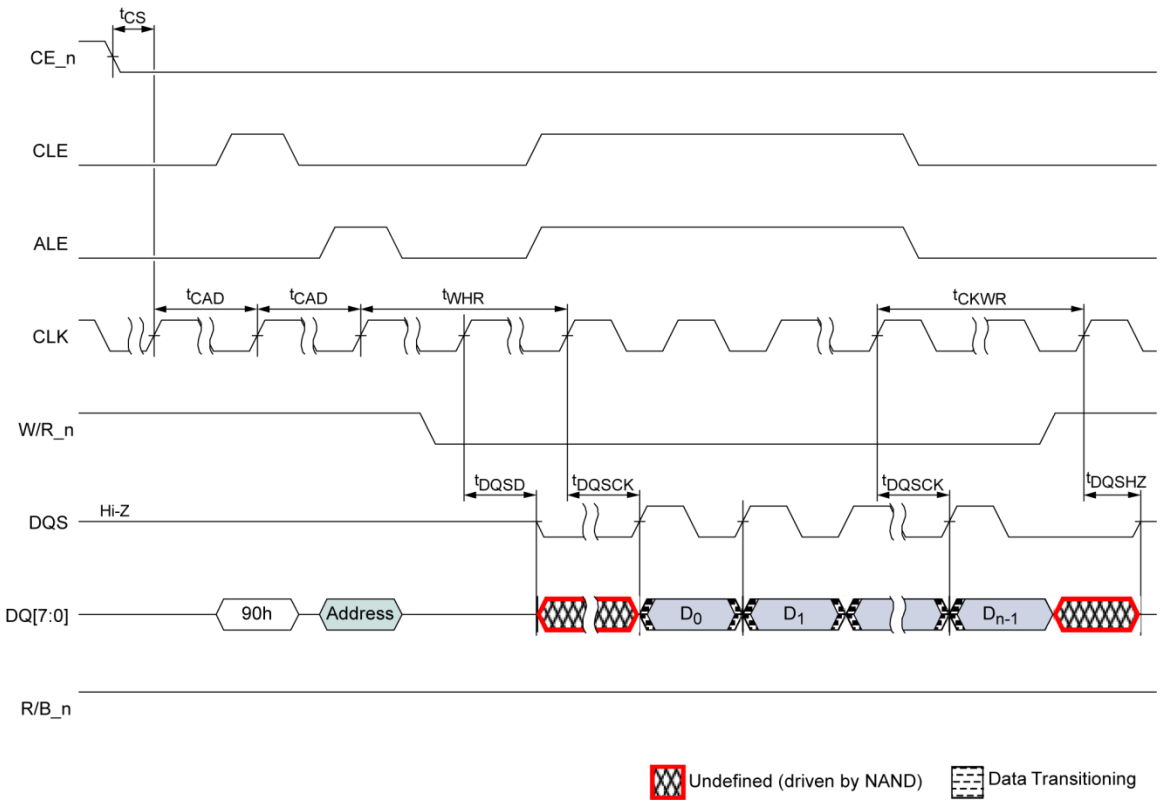


Figure 5-11 Read ID command using NV-DDR data interface

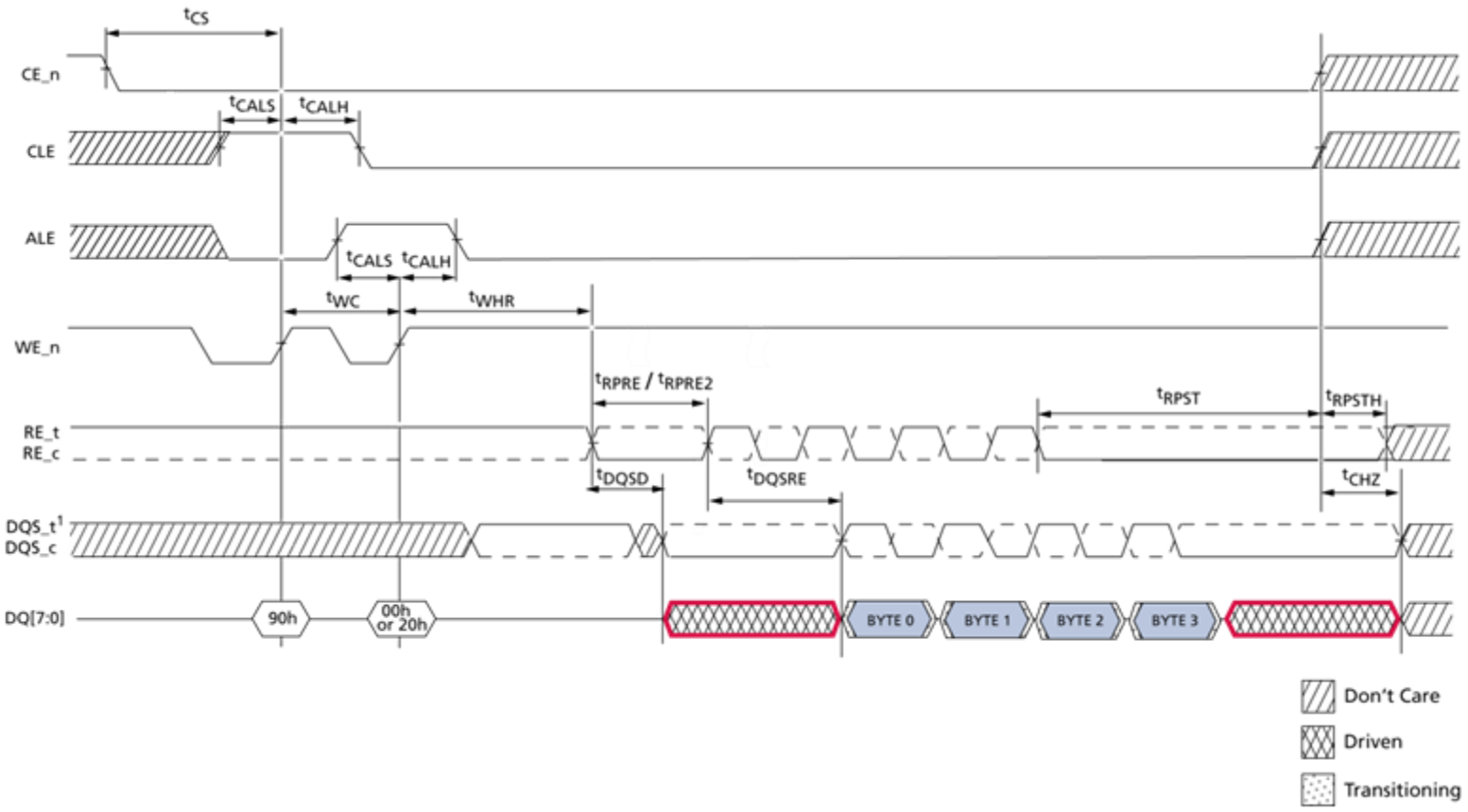


Figure 5-12 Read ID command using NV-DDR2 NV-DDR3 or NV-LPDDR4 data interface

NOTE 1: The data bytes in Figure 5-11 and Figure 5-12 are repeated twice (on the rising and falling edge of DQS). In Figure 5-12, when the bus state is not a data input or data output cycle, if ALE, CLE and CE_n are all low (i.e. Idle state) then DQS (DQS_t) shall be held high by the host to prevent the device from enabling ODT. If ODT is disabled, then DQS is a don't care during Idle states.

5.7. Read Parameter Page Definition

The Read Parameter Page function retrieves the data structure that describes the target's organization, features, timings and other behavioral parameters. There may also be additional information provided in an extended parameter page. Figure 5-13 defines the Read Parameter Page behavior.

Values in the parameter page are static and shall not change. The host is not required to read the parameter page after power management events.

The first time the host executes the Read Parameter Page command after power-on, timing mode 0 shall be used. If the host determines that the target supports more advanced timing modes, those supported timing modes may be used for subsequent execution of the Read Parameter Page command.

The Change Read Column command may be issued following execution of the Read Parameter Page to read specific portions of the parameter page.

Read Status may be used to check the status of Read Parameter Page during execution. After completion of the Read Status command, 00h shall be issued by the host on the command line to continue with the data output flow for the Read Parameter Page command (NOTE: Some NAND vendors may require the use of Change Read Column sequence instead of 00h command to output data from the NAND, see vendor datasheet).

Read Status Enhanced and Change Read Column Enhanced shall not be used during execution of the Read Parameter Page command.

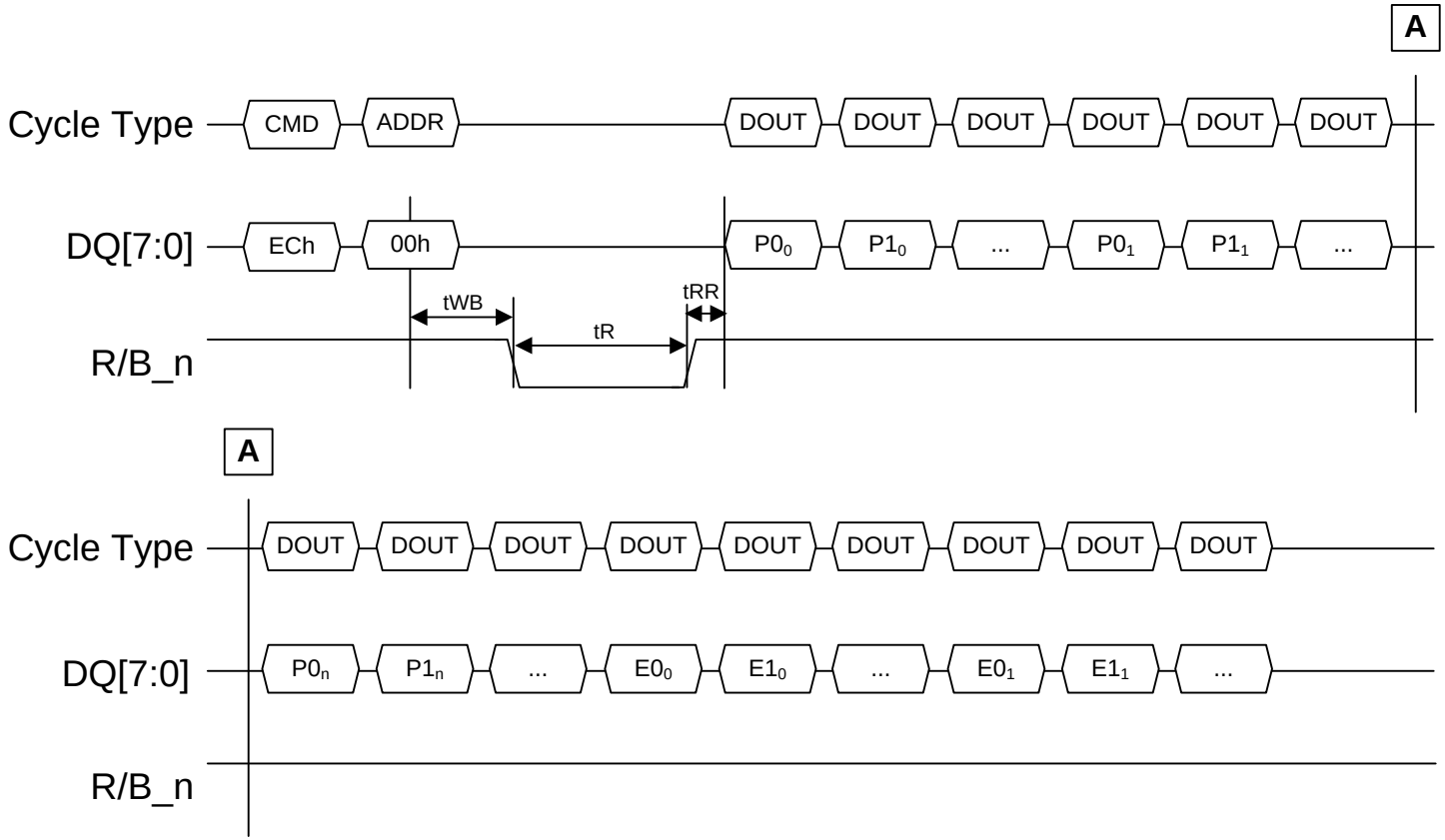


Figure 5-13 Read Parameter Page command timing

P0$_k$-Pn$_k$ The kth copy of the parameter page data structure. See section 5.7.1. Reading bytes beyond the end of the final parameter page copy (or beyond the final extended parameter page copy if supported) returns indeterminate values.

E0$_k$-En$_k$ The kth copy of the extended parameter page data structure. See section 5.7.2. Reading bytes beyond the end of the final extended parameter page copy returns indeterminate values. This field is only present when the extended parameter page is supported, as indicated in the Features supported field of the parameter page.

5.7.1. Parameter Page Data Structure Definition

Table 5-3 defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte. See section 1.3.2.3 for more information on the representation of word and Dword values.

Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the target will return how many data *bytes* are in a page. For a device that supports 16-bit data access, the host is required to convert byte values to word values for its use.

Unused fields should be cleared to 0h by the target.

Byte	O/M	Description
		Revision information and features block
0-3	M	Parameter page signature Byte 0: 4Fh, “O” Byte 1: 4Eh, “N” Byte 2: 46h, “F” Byte 3: 49h, “I”
4-5	M	Revision number 14-15 Reserved (0) 13 1 = supports ONFI version 5.1 12 1 = supports ONFI version 5.0 11 1 = supports ONFI version 4.2 10 1 = supports ONFI version 4.1 9 1 = supports ONFI version 4.0 8 1 = supports ONFI version 3.2 7 1 = supports ONFI version 3.1 6 1 = supports ONFI version 3.0 5 1 = supports ONFI version 2.3 4 1 = supports ONFI version 2.2 3 1 = supports ONFI version 2.1 2 1 = supports ONFI version 2.0 1 1 = supports ONFI version 1.0 0 Reserved (0)
6-7	M	Features supported 15 1 = supports Package Electrical Specification 14 1 = supports ZQ calibration 13 1 = supports NV-DDR3 12 1 = supports external Vpp 11 1 = supports Volume addressing 10 1 = supports NV-DDR2 9 1 = supports NV-LPDDR4 8 1 = supports program page register clear enhancement 7 1 = supports extended parameter page 6 1 = supports multi-plane read operations 5 1 = supports NV-DDR 4 1 = supports odd to even page Copyback 3 1 = supports multi-plane program and erase operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width

Byte	O/M	Description
8-9	M	Optional commands supported 14-15 Reserved (0) 13 1 = supports ZQ calibration (Long and Short) 12 1 = supports LUN Get and LUN Set Features 11 1 = supports ODT Configure 10 1 = supports Volume Select 9 1 = supports Reset LUN 8 1 = supports Small Data Move 7 1 = supports Change Row Address 6 1 = supports Change Read Column Enhanced 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache commands 0 1 = supports Page Cache Program command
10	O	ONFI-JEDEC JTG primary advanced command support 4-7 Reserved (0) 3 1 = supports Multi-plane Block Erase 2 1 = supports Multi-plane Copyback Program 1 1 = supports Multi-plane Page Program 0 1 = supports Random Data Out
11	M	Training commands supported 7 1 = supports Per-Pin Vrefq Training (Absolute Value method) 6 1 = supports Per-Pin Vrefq Training (offset method) 5 1 = supports Internal vrefq Training 4 1 = supports Write RX DQ training 3 1 = supports Write TX DQ training 2 1 = supports Read DQ training 1 1 = supports Implicit (command based) DCC training 0 1 = supports Explicit DCC Training
12-13	O	Extended parameter page length
14	O	Number of parameter pages
15	M	Training commands supported 1-7 Reserved (0) 0 1 = supports Write Duty Cycle Adjustment Training (WDCA)
16-31		Reserved (0)
	Manufacturer information block	
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64	M	JEDEC manufacturer ID
65-66	O	Date code
67-79		Reserved (0)
	Memory organization block	
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89		Reserved (0)
90-91		Reserved (0)
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)

Byte	O/M	Description
100	M	Number of logical units (LUNs)
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles
102	M	Number of bits per cell
103-104	M	Bad blocks maximum per LUN
105-106	M	Block endurance
107	M	Guaranteed valid blocks at beginning of target
108-109	M	Block endurance for guaranteed valid blocks
110	M	Number of programs per page
111		Reserved (0)
112	M	Number of bits ECC correctability
113	M	Number of plane address bits 4-7 Reserved (0) 0-3 Number of plane address bits
114	O	Multi-plane operation attributes 6-7 Reserved (0) 5 1 = lower bit XNOR block address restriction 4 1 = read cache supported 3 Address restrictions for cache operations 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent multi-plane support
115	O	Reserved (0)
116-117	O	NV-DDR3 timing mode support 4-15 Reserved (0) 3 1 = supports timing mode 22 2 1 = supports timing mode 21 1 1 = supports timing mode 20 0 1 = supports timing mode 19
118-121	O	NV-LPDDR4 timing mode support 20-31 Reserved (0) 19 1 = supports timing mode 22 18 1 = supports timing mode 21 17 1 = supports timing mode 20 16 1 = supports timing mode 19 15 1 = supports timing mode 18 14 1 = supports timing mode 17 13 1 = supports timing mode 16 12 1 = supports timing mode 15 11 1 = supports timing mode 14 10 1 = supports timing mode 13 9 1 = supports timing mode 12 8 1 = supports timing mode 11 7 1 = supports timing mode 10 6 1 = supports timing mode 9 5 1 = supports timing mode 8 4 1 = supports timing mode 7 3 1 = supports timing mode 6 2 1 = supports timing mode 5 1 1 = supports timing mode 4 0 1 = supports timing modes 0-3
122-127		Reserved (0)

Byte	O/M	Description
	Electrical parameters block	
128	O	Reserved (0)
129-130	M	SDR timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1
131-132	O	Reserved (0)
133-134	O	Reserved (0)
135-136	O	Reserved (0)
137-138	O	Reserved (0)
139-140	O	Reserved (0)
141	O	NV-DDR timing mode support 7 Reserved (0) 6 Obsolete 5 1 = supports NV-DDR timing mode 5 4 1 = supports NV-DDR timing mode 4 3 1 = supports NV-DDR timing mode 3 2 1 = supports NV-DDR timing mode 2 1 1 = supports NV-DDR timing mode 1 0 1 = supports NV-DDR timing mode 0
142	O	NV-DDR2 timing mode support 7 1 = supports timing mode 7 6 1 = supports timing mode 6 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0
143	O	NV-DDR / NV-DDR2 features 4-7 Reserved (0) 3 1 = device requires Vpp enablement sequence 2 1 = device supports CLK stopped for data input 1 Reserved (0) 0 tCAD value to use
144-145	O	Reserved (0)
146-147	O	Reserved (0)
148-149	O	Reserved (0)
150	O	Reserved (0)
151	M	Driver strength support. If the device supports NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface, then one and only one of bit 0, bit 3, and bit 4 shall be set. If bit 0, bit 3, and bit 4 are all cleared to zero, then the driver strength at power-on is undefined. 5-7 Reserved (0) 4 1 = supports 35 Ohm, 37.5 Ohm and 50 Ohm drive strength. Default is 35 Ohm

Byte	O/M	Description
		3 1 = supports 37.5 Ohm and 50 Ohm drive strength. Default is 37.5 Ohm. 2 1 = supports 18 Ohm drive strength. 1 1 = supports 25 Ohm drive strength. 0 1 = supports 35 Ohm and 50 Ohm drive strength. Default is 35 Ohm.
152-153	O	Reserved (0)
154-155	O	Reserved (0)
156-157	O	Reserved (0)
158	O	NV-DDR2/3 features 6-7 Reserved (0) 5 1 = external VREFQ required for ≥ 200 MT/s 4 1 = supports differential signaling for DQS 3 1 = supports differential signaling for RE_n 2 1 = supports ODT value of 30 Ohms 1 1 = supports matrix termination ODT 0 1 = supports self-termination ODT
159	M	NV-DDR2/3 warmup cycles 4-7 Data Input warmup cycles support 0-3 Data Output warmup cycles support
160-161	O	NV-DDR3 timing mode support 15 1 = supports timing mode 18 14 1 = supports timing mode 17 13 1 = supports timing mode 16 12 1 = supports timing mode 15 11 1 = supports timing mode 14 10 1 = supports timing mode 13 9 1 = supports timing mode 12 8 1 = supports timing mode 11 7 1 = supports timing mode 10 6 1 = supports timing mode 9 5 1 = supports timing mode 8 4 1 = supports timing mode 7 3 1 = supports timing mode 6 2 1 = supports timing mode 5 1 1 = supports timing mode 4 0 1 = supports timing modes 0-3
162	O	NV-DDR2 timing mode support 3-7 Reserved (0) 2 1 = supports NV-DDR2 timing mode 10 1 1 = supports NV-DDR2 timing mode 9 0 1 = supports NV-DDR2 timing mode 8
163		Reserved (0)
	Vendor block	
164-165	M	Vendor specific Revision number
166-253		Vendor specific
254-255	M	Integrity CRC

Byte	O/M	Description
	Redundant Parameter Pages	
256-511	M	Value of bytes 0-255
512-767	M	Value of bytes 0-255
768+	O	Additional redundant parameter pages

Table 5-3 Parameter page definitions

5.7.1.1. Byte 0-3: Parameter page signature

This field contains the parameter page signature. When two or more bytes of the signature are valid, then it denotes that a valid copy of the parameter page is present.

Byte 0 shall be set to 4Fh.

Byte 1 shall be set to 4Eh.

Byte 2 shall be set to 46h.

Byte 3 shall be set to 49h.

5.7.1.2. Byte 4-5: Revision number

This field indicates the revisions of the ONFI specification that the target complies to. The target may support multiple revisions of the ONFI specification. This is a bit field where each defined bit corresponds to a particular specification revision that the target may support.

Bit 0 shall be cleared to zero.

Bit 1 when set to one indicates that the target supports the ONFI revision 1.0 specification.

Bit 2 when set to one indicates that the target supports the ONFI revision 2.0 specification.

Bit 3 when set to one indicates that the target supports the ONFI revision 2.1 specification.

Bit 4 when set to one indicates that the target supports the ONFI revision 2.2 specification.

Bit 5 when set to one indicates that the target supports the ONFI revision 2.3 specification.

Bit 6 when set to one indicates that the target supports the ONFI revision 3.0 specification.

Bit 7 when set to one indicates that the target supports the ONFI revision 3.1 specification.

Bit 8 when set to one indicates that the target supports the ONFI revision 3.2 specification.

Bit 9 when set to one indicates that the target supports the ONFI revision 4.0 specification.

Bit 10 when set to one indicates that the target supports the ONFI revision 4.1 specification.

Bit 11 when set to one indicates that the target supports the ONFI revision 4.2 specification.

Bit 12 when set to one indicates that the target supports the ONFI revision 5.0 specification.

Bit 13 when set to one indicates that the target supports the ONFI revision 5.1 specification.

Bits 14-15 are reserved and shall be cleared to zero.

5.7.1.3. Byte 6-7: Features supported

This field indicates the optional features that the target supports.

Bit 0 when set to one indicates that the target's data bus width is 16-bits. Bit 0 when cleared to zero indicates that the target's data bus width is 8-bits. The host shall use the indicated data bus width for all ONFI commands that are defined to be transferred at the bus width (x8 or x16). Note that some commands, like Read ID, always transfer data as 8-bit only. If the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interfaces are supported, then the data bus width shall be 8-bits.

Bit 1 when set to one indicates that the target supports multiple LUN operations (see section 3.1.3). If bit 1 is cleared to zero, then the host shall not issue commands to a LUN unless all other LUNs on the target are idle (i.e. R/B_n is set to one).

Bit 2 when set to one indicates that the target supports non-sequential page programming operations, such that the host may program pages within a block in arbitrary order. Bit 2 when cleared to zero indicates that the target does not support non-sequential page programming operations. If bit 2 is cleared to zero, the host shall program all pages within a block in order starting with page 0.

Bit 3 when set to one indicates that the target supports multi-plane program and erase operations. Refer to section 5.7.1.28.

Bit 4 when set to one indicates that there are no even / odd page restrictions for Copyback operations. Specifically, a read operation may access an odd page and then program the contents to an even page using Copyback. Alternatively, a read operation may access an even page and then program the contents to an odd page using Copyback. Bit 4 when cleared to zero indicates that the host shall ensure that Copyback reads and programs from odd page to odd page or alternatively from even page to even page.

Bit 5 when set to one indicates that the NV-DDR data interface is supported by the target. If bit 5 is set to one, then the target shall indicate the NV-DDR timing modes supported in the NV-DDR timing mode support field. Bit 5 when cleared to zero indicates that the NV-DDR data interface is not supported by the target.

Bit 6 when set to one indicates that the target supports multi-plane read operations. Refer to section 5.7.1.28.

Bit 7 when set to one indicates the target includes an extended parameter page that is stored in the data bytes following the last copy of the parameter page. If bit 7 is cleared to zero, then an extended parameter page is not supported. Refer to section 5.7.2. NOTE: This bit was inadvertently specified in the BA NAND specification to show support for BA NAND. If the device supports BA NAND, then the number of bits of ECC correctability should be cleared to 0h in byte 112 of the parameter page.

Bit 8 when set to one indicates that the target supports clearing only the page register for the LUN addressed with the Program (80h) command. If bit 8 is cleared to zero, then a Program (80h) command clears the page register for each LUN that is part of the target. At power-on, the device clears the page register for each LUN that is part of the target. Refer to section 5.31.1 for how to enable this feature.

Bit 9 when set to one indicates that the NV-LPDDR4 interface is supported by the target. If bit 9 is set to one, then the target shall indicate the NV-LPDDR4 timing modes supported in the NV-

LPDDR4 timing mode support field. Bit 9 when cleared to zero indicates that the NV-LPDDR4 data interface is not supported by the target.

Bit 10 when set to one indicates that the NV-DDR2 data interface is supported by the target. If bit 10 is set to one, then the target shall indicate the NV-DDR2 timing modes supported in the NV-DDR2 timing mode support field. Bit 10 when cleared to zero indicates that the NV-DDR2 data interface is not supported by the target.

Bit 11 when set to one indicates that the NAND Target supports Volume addressing, as defined in section 3.2. If bit 11 is cleared to zero, then the target does not support Volume addressing.

Bit 12 when set to one indicates that the target supports external Vpp. If bit 12 is cleared to zero, then the target does not support external Vpp.

Bit 13 when set to one indicates that the NV-DDR3 data interface is supported by the target. If bit 13 is set to one, then the target shall indicate the NV-DDR3 timing modes supported in the NV-DDR3 timing mode support field. Bit 13 when cleared to zero indicates that the NV-DDR3 data interface is not supported by the target.

Bit 14 when set to one indicates that the target supports ZQ calibration. If bit 14 is cleared to zero, then the target does not support ZQ calibration.

Bit 15 when set to one indicates that the target supports Package Electrical Specification and Pad Capacitance (see section 4.11.3) If bit 15 is cleared to zero, then the target does not support Package Electrical Specification and Pad Capacitance.

5.7.1.4. Byte 8-9: Optional commands supported

This field indicates the optional commands that the target supports.

Bit 0 when set to one indicates that the target supports the Page Cache Program command. If bit 0 is cleared to zero, the host shall not issue the Page Cache Program command to the target.

Bit 1 when set to one indicates that the target supports the Read Cache Random, Read Cache Sequential, and Read Cache End commands. If bit 1 is cleared to zero, the host shall not issue the Read Cache Sequential, Read Cache Random, or Read Cache End commands to the target.

Bit 2 when set to one indicates that the target supports the Get Features and Set Features commands. If bit 2 is cleared to zero, the host shall not issue the Get Features or Set Features commands to the target.

Bit 3 when set to one indicates that the target supports the Read Status Enhanced command. If bit 3 is cleared to zero, the host shall not issue the Read Status Enhanced command to the target. Read Status Enhanced shall be supported if the target has multiple LUNs or supports multi-plane operations.

Bit 4 when set to one indicates that the target supports the Copyback Program and Copyback Read commands. If bit 4 is cleared to zero, the host shall not issue the Copyback Program or Copyback Read commands to the target. If multi-plane operations are supported and this bit is set to one, then multi-plane copyback operations shall be supported.

Bit 5 when set to one indicates that the target supports the Read Unique ID command. If bit 5 is cleared to zero, the host shall not issue the Read Unique ID command to the target.

Bit 6 when set to one indicates that the target supports the Change Read Column Enhanced command. If bit 6 is cleared to zero, the host shall not issue the Change Read Column Enhanced command to the target.

Bit 7 when set to one indicates that the target supports the Change Row Address command. If bit 7 is cleared to zero, the host shall not issue the Change Row Address command to the target.

Bit 8 when set to one indicates that the target supports the Small Data Move command for both Program and Copyback operations. If bit 8 is cleared to zero, the target does not support the Small Data Move command for Program or Copyback operations. The Small Data Move command is mutually exclusive with overlapped multi-plane support. Refer to section 5.19. When bit 8 is set to one, the device shall support the 11h command to flush any internal data pipeline regardless of whether multi-plane operations are supported.

Bit 9 when set to one indicates that the target supports the Reset LUN command. If bit 9 is cleared to zero, the host shall not issue the Reset LUN command.

Bit 10 when set to one indicates that the target supports the Volume Select command. If bit 10 is cleared to zero, the host shall not issue the Volume Select command. The device shall support the Volume Select command if it supports either the CE_n pin reduction or matrix termination features.

Bit 11 when set to one indicates that the target supports the ODT Configure command. If bit 11 is cleared to zero, the host shall not issue the ODT Configure command. The device shall support the ODT Configure command if it supports the matrix termination feature.

Bit 12 when set to one indicates that the target supports the LUN Get Features and LUN Set Features commands. If bit 12 is cleared to zero, the host shall not issue the LUN Get Features or LUN Set Features commands to the target.

Bit 13 when set to one indicates that the target supports the ZQ Calibration Long and ZQ Calibration Short commands. If bit 13 is cleared to zero, the host shall not issue ZQ Calibration Long or ZQ Calibration Short commands.

Bits 14-15 are reserved and shall be cleared to zero.

5.7.1.5. Byte 10: ONFI-JEDEC JTG primary advanced command support

This field indicates the primary advanced commands defined by the ONFI-JEDEC Joint Taskgroup that are supported by the target. Specifically, these are commands where the primary version of the advanced commands is not based on an ONFI heritage. Support for primary advanced commands that are based on an ONFI heritage are indicated in their traditional parameter page location.

Bit 0 when set to one indicates that the target supports the ONFI-JEDEC JTG primary Random Data Out command. If bit 0 is cleared to zero, the host shall not issue the ONFI-JEDEC JTG primary Random Data Out command to the target. Specifically, the ONFI-JEDEC JTG primary Random Data Out command is the sequence 00h - Column and Row Address Cycles Input - 05h - Column Address Cycles Input - E0h. Refer to the vendor device datasheet for the number of address cycles needed after the 00h and 05h commands.

Bit 1 when set to one indicates that the target supports the ONFI-JEDEC JTG primary Multi-plane Page Program command. If bit 1 is cleared to zero, the host shall not issue the ONFI-JEDEC JTG primary Multi-plane Page Program command to the target. Specifically, the ONFI-JEDEC JTG

primary Multi-plane Page Program command utilizes 81h for the first cycle of program sequences after the initial program sequence instead of 80h.

Bit 2 when set to one indicates that the target supports the ONFI-JEDEC JTG primary Multi-plane Copyback Program command. If bit 2 is cleared to zero, the host shall not issue the ONFI-JEDEC JTG primary Multi-plane Copyback Program command to the target. Specifically, the ONFI-JEDEC JTG primary Multi-plane Copyback Program command utilizes 81h for the first cycle of program sequences after the initial program sequence instead of 85h.

Bit 3 when set to one indicates that the target supports the ONFI-JEDEC JTG primary Multi-plane Block Erase command. If bit 3 is cleared to zero, the host shall not issue the ONFI-JEDEC JTG primary Multi-plane Block Erase command to the target. Specifically, the ONFI-JEDEC JTG primary Multi-plane Block Erase does not utilize the D1h command cycle between block addresses.

Bits 4-7 are reserved and shall be cleared to zero.

5.7.1.6. Byte 11: Training Commands Support

This field indicates the training commands supported as defined by the ONFI-JEDEC Joint Taskgroup that are supported by the target.

Bit 0 when set to one indicates that the target supports Explicit DCC training. If bit 0 is cleared to zero, the host does not support Explicit DCC training. Specifically, Explicit DCC training is initiated with a Set Features command (EFh) at B0[0] of feature address 20h.

Bit 1 when set to one indicates that the target supports Implicit (command based) DCC training. If bit 1 is cleared to zero, the host does not support Implicit (command based) DCC training. Specifically, Implicit DCC training is initiated with an Implicit DCC training command (18h) along with a targeted address.

Bit 2 when set to one indicates that the target supports Read DQ training. If bit 2 is cleared to zero, the host does not support Read DQ training. Specifically, Read DQ training is initiated with a Read DQ training command (62h) along with a targeted address.

Bit 3 when set to one indicates that the target supports Write DQ TX training. If bit 3 is cleared to zero, the host does not support Write DQ TX training. Specifically, Write DQ TX training is initiated with command 63h along with a targeted address and read back using command 64h.

Bit 4 when set to one indicates that the target supports Write DQ RX training. If bit 4 is cleared to zero, the host does not support Write DQ RX training. Specifically, Write DQ RX training is initiated with command 76h along with a targeted address.

Bit 5 when set to one indicates that the target supports Internal Vrefq Training. If bit 5 is cleared to zero, the host does not support Internal Vrefq Training.

Bit 6 when set to one indicates that the target supports Per-Pin Vrefq Training by Offset method. If bit 6 is cleared to zero, the host does not support Per-Pin Vrefq Training by Offset method.

Bit 7 when set to one indicates that the target supports Per-Pin Vrefq Training by Absolute Value method. If bit 7 is cleared to zero, the host does not support Per-Pin Vrefq Training by Absolute Value method.

5.7.1.7. Byte 12-13: Extended parameter page length

If the target supports an extended parameter page as indicated in the Features supported field, then this field specifies the length of the extended parameter page in multiples of 16 bytes. Thus, a value of 2 corresponds to 32 bytes and a value of 3 corresponds to 48 bytes. The minimum size is 3, corresponding to 48 bytes.

5.7.1.8. Byte 14: Number of parameter pages

If the target supports an extended parameter page as indicated in the Features supported field, then this field specifies the number of parameter pages present, including the original and the subsequent redundant versions. As an example, a value of 3 means that there are three parameter pages present and thus the extended parameter page starts at byte 768. The number of extended parameter pages should match the number of parameter pages.

5.7.1.9. Byte 15: Additional Training Commands Support

This field indicates the additional training commands supported as defined by the ONFI-JEDEC Joint Taskgroup that are supported by the target

Bit 0 when set to one indicates that the target supports Write Duty Cycle Training. If bit 0 is cleared to zero, the host does not support Write Duty-Cycle Adjustment

Bits 1-7 are reserved and shall be cleared to zero.

5.7.1.10. Byte 32-43: Device manufacturer

This field contains the manufacturer of the device. The content of this field is an ASCII character string of twelve bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

There is no standard for how the manufacturer represents their name in the ASCII string. If the host requires use of a standard manufacturer ID, it should use the JEDEC manufacturer ID (refer to section 5.7.1.12).

5.7.1.11. Byte 44-63: Device model

This field contains the model number of the device. The content of this field is an ASCII character string of twenty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

5.7.1.12. Byte 64: JEDEC manufacturer ID

This field contains the JEDEC manufacturer ID for the manufacturer of the device.

5.7.1.13. Byte 65-66: Date code

This field contains a date code for the time of manufacture of the device. Byte 65 shall contain the two least significant digits of the year (e.g. a value of 05h to represent the year 2005). Byte 66 shall contain the workweek, where a value of 00h indicates the first week of January.

If the date code functionality is not implemented, the value in this field shall be 0000h.

5.7.1.14. Byte 80-83: Number of data bytes per page

This field contains the number of data bytes per page. The value reported in this field shall be a power of two. The minimum value that shall be reported is 512 bytes.

5.7.1.15. Byte 84-85: Number of spare bytes per page

This field contains the number of spare bytes per page. There are no restrictions on the value.

Appendix B lists recommendations for the number of bytes per page based on the page size and the number of bits of ECC correctability for the device.

5.7.1.16. Byte 92-95: Number of pages per block

This field contains the number of pages per block. This value shall be a multiple of 32. Refer to section 3.1 for addressing requirements.

5.7.1.17. Byte 96-99: Number of blocks per logical unit

This field contains the number of blocks per logical unit. There are no restrictions on this value. Refer to section 3.1 for addressing requirements.

5.7.1.18. Byte 100: Number of logical units (LUNs)

This field indicates the number of logical units the target supports. Logical unit numbers are sequential, beginning with a LUN address of 0. This field shall be greater than zero.

5.7.1.19. Byte 101: Number of Address Cycles

This field indicates the number of address cycles used for row and column addresses. The reported number of address cycles shall be used by the host in operations that require row and/or column addresses (e.g. Page Program).

Bits 0-3 indicate the number of address cycles used for the row address. This field shall be greater than zero.

Bits 4-7 indicate the number of address cycles used for the column address. This field shall be greater than zero.

NOTE: Throughout this specification examples are shown with 2-byte column addresses and 3-byte row addresses. However, the host is responsible for providing the number of column and row address cycles in each of these sequences based on the values in this field.

5.7.1.20. Byte 102: Number of bits per cell

This field indicates the number of bits per cell in the Flash array. This field shall be greater than zero.

A value of FFh indicates that the number of bits per cell is not specified.

5.7.1.21. Byte 103-104: Bad blocks maximum per LUN

This field contains the maximum number of blocks that may be defective at manufacture and over the life of the device per LUN. The maximum rating assumes that the host is following the block endurance requirements and the ECC requirements reported in the parameter page.

5.7.1.22. Byte 105-106: Block endurance

This field indicates the maximum number of program/erase cycles per addressable page/block. This value assumes that the host is using at least the minimum ECC correctability reported in the parameter page.

A page may be programmed in partial operations subject to the value reported in the Number of programs per page field. However, programming different locations within the same page does not count against this value more than once per full page.

The block endurance is reported in terms of a value and a multiplier according to the following equation: value x $10^{multiplier}$. Byte 105 comprises the value. Byte 106 comprises the multiplier. For example, a target with an endurance of 75,000 cycles would report this as a value of 75 and a multiplier of 3 (75 x 10^3). For a write once device, the target shall report a value of 1 and a multiplier of 0. For a read-only device, the target shall report a value of 0 and a multiplier of 0. The value field shall be the smallest possible; for example 100,000 shall be reported as a value of 1 and a multiplier of 5 (1 x 10^5).

5.7.1.23. Byte 107: Guaranteed valid blocks at beginning of target

This field indicates the number of guaranteed valid blocks starting at block address 0 of the target. The minimum value for this field is 1h. The blocks are guaranteed to be valid for the endurance specified for this area (see section 5.7.1.24) when the host follows the specified number of bits to correct.

5.7.1.24. Byte 108-109: Block endurance for guaranteed valid blocks

This field indicates the minimum number of program/erase cycles per addressable page/block in the guaranteed valid block area (see section 5.7.1.23). This value requires that the host is using at least the minimum ECC correctability reported in the parameter page. This value is not encoded. If the value is 0000h, then no minimum number of cycles is specified, though the block(s) are guaranteed valid from the factory.

5.7.1.25. Byte 110: Number of programs per page

This field indicates the maximum number of times a portion of a page may be programmed without an erase operation. After the number of programming operations specified have been performed, the host shall issue an erase operation to that block before further program operations to the affected page. This field shall be greater than zero. Programming the same portion of a page without an erase operation results in indeterminate page contents.

5.7.1.26. Byte 112: Number of bits ECC correctability

This field indicates the number of bits that the host should be able to correct per 512 bytes of data. With this specified amount of error correction by the host, the target shall achieve the block endurance specified in the parameter page. When the specified amount of error correction is applied by the host and the block endurance is followed, then the maximum number of bad blocks shall not be exceeded by the device. All used bytes in the page shall be protected by host controller ECC including the spare bytes if the minimum ECC requirement has a value greater than zero.

If the recommended ECC codeword size is not 512 bytes, then this field shall be set to FFh. The host should then read the Extended ECC Information that is part of the extended parameter page to retrieve the ECC requirements for this device.

When this value is cleared to zero, the target shall return valid data.

5.7.1.27. Byte 113: Multi-plane addressing

This field describes parameters for multi-plane addressing.

Bits 0-3 indicate the number of bits that are used for multi-plane addressing. This value shall be greater than 0h when multi-plane operations are supported. For information on the plane address location, refer to section 3.1.1.

Bits 4-7 are reserved.

5.7.1.28. Byte 114: Multi-plane operation attributes

This field describes attributes for multi-plane operations. This byte is mandatory when multi-plane operations are supported as indicated in the Features supported field.

Bit 0 indicates whether overlapped multi-plane operations are supported. If bit 0 is set to one, then overlapped multi-plane operations are supported. If bit 0 is cleared to zero, then concurrent multi-plane operations are supported.

Bit 1 indicates that there are no block address restrictions for the multi-plane operation. If set to one all block address bits may be different between multi-plane operations. If cleared to zero, there are block address restrictions. Refer to bit 5 for the specific block address restrictions required.

Bit 2 indicates whether program cache is supported with multi-plane programs. If set to one then program cache is supported for multi-plane program operations. If cleared to zero then program cache is not supported for multi-plane program operations. Note that program cache shall not be used with multi-plane copyback program operations. See bit 3 for restrictions on the multi-plane addresses that may be used.

Bit 3 indicates whether the block address bits other than the multi-plane address bits of multi-plane addresses may change during either: a) a program cache sequence between 15h commands, or b) a read cache sequence between 31h commands. If set to one and bit 2 is set to one, then the host may change the number of multi-plane addresses and the value of the block address bits (other than the multi-plane address bits) in the program cache sequence. If set to one and bit 4 is set to one, then the host may change the number of multi-plane addresses and the value of the block address bits (other than the multi-plane address bits) in the read cache sequence. If cleared to zero and bit 2 is set to one, then for each program cache operation the block address bits (other than the plane address bits) and number of multi-plane addresses issued to the LUN shall be the same. If cleared to zero and bit 4 is set to one, then for each read cache operation the block address bits (other than the multi-plane address bits) and number of multi-plane addresses issued to the LUN shall be the same.

Bit 4 indicates whether read cache is supported with multi-plane reads. If set to one then read cache is supported for multi-plane read operations. If cleared to zero then read cache is not supported for multi-plane read operations. Note that read cache shall not be used with multi-plane copyback read operations.

Bit 5 indicates the type of block address restrictions required for the multi-plane operation. If set to one then all block address bits (other than the multi-plane address bits) shall be the same if the XNOR of the lower multi-plane address bits between two multi-plane addresses is one. If cleared to zero, all block address bits (other than the multi-plane address bits) shall be the same regardless of the multi-plane address bits between two plane addresses. See section 3.1.1.1 for a detailed definition of interleaved block address restrictions. These restrictions apply to all multi-plane operations (Read, Program, Erase, and Copyback Program).

Bits 6-7 are reserved.

5.7.1.29. Byte 116-117: NV-DDR3 timing mode support (cont.)

This field indicates the NV-DDR3 timing modes above mode 18 that are supported. If the NV-DDR3 data interface is supported by the target, at least one NV-DDR3 timing mode shall be supported. The target shall support an inclusive range of NV-DDR3 timing modes (i.e. if timing mode n-1 and n+1 are supported, then the target shall also support timing mode n).

Bit 0 when set to one indicates that the target supports NV-DDR3 timing modes 19.

Bit 1 when set to one indicates that the target supports NV-DDR3 timing modes 20.

Bit 2 when set to one indicates that the target supports NV-DDR3 timing modes 21.

Bit 3 when set to one indicates that the target supports NV-DDR3 timing modes 22.

Bits 4-15 are reserved.

5.7.1.30. Byte 118-121: NV-LPDDR4 timing mode support

This field indicates the NV-LPDDR4 timing modes supported. If the NV-LPDDR4 data interface is supported by the target, at least one NV-LPDDR4 timing mode shall be supported. The target shall support an inclusive range of NV-LPDDR4 timing modes (i.e. if timing mode n-1 and n+1 are supported, then the target shall also support timing mode n).

Bit 0 when set to one indicates that the target supports NV-LPDDR4 timing modes 0-3.

Bit 1 when set to one indicates that the target supports NV-LPDDR4 timing mode 4.

Bit 2 when set to one indicates that the target supports NV-LPDDR4 timing mode 5.

Bit 3 when set to one indicates that the target supports NV-LPDDR4 timing mode 6.

Bit 4 when set to one indicates that the target supports NV-LPDDR4 timing mode 7.

Bit 5 when set to one indicates that the target supports NV-LPDDR4 timing mode 8.

Bit 6 when set to one indicates that the target supports NV-LPDDR4 timing mode 9.

Bit 7 when set to one indicates that the target supports NV-LPDDR4 timing mode 10.

Bit 8 when set to one indicates that the target supports NV-LPDDR4 timing mode 11.

Bit 9 when set to one indicates that the target supports NV-LPDDR4 timing mode 12.

Bit 10 when set to one indicates that the target supports NV-LPDDR4 timing mode 13.

Bit 11 when set to one indicates that the target supports NV-LPDDR4 timing mode 14.

Bit 12 when set to one indicates that the target supports NV-LPDDR4 timing mode 15.

Bit 13 when set to one indicates that the target supports NV-LPDDR4 timing mode 16.

Bit 14 when set to one indicates that the target supports NV-LPDDR4 timing mode 17.

Bit 15 when set to one indicates that the target supports NV-LPDDR4 timing mode 18.

Bit 16 when set to one indicates that the target supports NV-LPDDR4 timing mode 19.

Bit 17 when set to one indicates that the target supports NV-LPDDR4 timing mode 20.

Bit 18 when set to one indicates that the target supports NV-LPDDR4 timing mode 21.

Bit 19 when set to one indicates that the target supports NV-LPDDR4 timing mode 22.

5.7.1.31. Byte 129-130: SDR timing mode support

This field indicates the SDR timing modes supported. The target shall always support SDR timing mode 0.

Bit 0 shall be set to one. It indicates that the target supports SDR timing mode 0.

Bit 1 when set to one indicates that the target supports SDR timing mode 1.

Bit 2 when set to one indicates that the target supports SDR timing mode 2.

Bit 3 when set to one indicates that the target supports SDR timing mode 3.

Bit 4 when set to one indicates that the target supports SDR timing mode 4.

Bit 5 when set to one indicates that the target supports SDR timing mode 5.

Bits 6-15 are reserved and shall be cleared to zero.

5.7.1.32. Byte 141: NV-DDR timing mode support

This field indicates the NV-DDR timing modes supported. If the NV-DDR data interface is supported by the target, at least one NV-DDR timing mode shall be supported. The target shall support an inclusive range of NV-DDR timing modes (i.e. if timing mode n-1 and n+1 are supported, then the target shall also support timing mode n).

Bit 0 when set to one indicates that the target supports NV-DDR timing mode 0.

Bit 1 when set to one indicates that the target supports NV-DDR timing mode 1.

Bit 2 when set to one indicates that the target supports NV-DDR timing mode 2.

Bit 3 when set to one indicates that the target supports NV-DDR timing mode 3.

Bit 4 when set to one indicates that the target supports NV-DDR timing mode 4.

Bit 5 when set to one indicates that the target supports NV-DDR timing mode 5.

Bits 6-7 are reserved and shall be cleared to zero.

5.7.1.33. Byte 142: NV-DDR2 timing mode support

This field indicates the NV-DDR2 timing modes supported. If the NV-DDR2 data interface is supported by the target, at least one NV-DDR2 timing mode shall be supported. The target shall support an inclusive range of NV-DDR2 timing modes (i.e. if timing mode n-1 and n+1 are supported, then the target shall also support timing mode n).

Bit 0 when set to one indicates that the target supports NV-DDR2 timing mode 0.

Bit 1 when set to one indicates that the target supports NV-DDR2 timing mode 1.

Bit 2 when set to one indicates that the target supports NV-DDR2 timing mode 2.

Bit 3 when set to one indicates that the target supports NV-DDR2 timing mode 3.

Bit 4 when set to one indicates that the target supports NV-DDR2 timing mode 4.

Bit 5 when set to one indicates that the target supports NV-DDR2 timing mode 5.

Bit 6 when set to one indicates that the target supports NV-DDR2 timing mode 6.

Bit 7 when set to one indicates that the target supports NV-DDR2 timing mode 7.

5.7.1.34. Byte 143: NV-DDR / NV-DDR2 / NV-DDR3 features

This field describes features and attributes for NV-DDR, NV-DDR2, NV-DDR3 and/or NV-LPDDR4 operation. This byte is mandatory when the NV-DDR or NV-DDR2 data interface is supported.

Bit 0 indicates the tCAD value that shall be used by the host. If bit 0 is set to one, then the host shall use the tCADs (slow) value in NV-DDR command, address and data transfers. If bit 0 is cleared to zero, then the host shall use the tCADf (fast) value in NV-DDR command, address and data transfers. This field applies to the NV-DDR data interface only.

Bit 1 is reserved

Bit 2 indicates that the device supports the CLK being stopped during data input, as described in Figure 4-34. If bit 2 is set to one, then the host may optionally stop the CLK during data input for power savings. If bit 2 is set to one, the host may pause data while the CLK is stopped. If bit 2 is cleared to zero, then the host shall leave CLK running during data input. This field applies to the NV-DDR data interface only.

Bit 3 indicates that the device requires the power-on sequence to provide valid Vcc before Vpp and the power-down sequence to remove Vpp before removing Vcc.

Bits 4-7 are reserved.

5.7.1.35. Byte 151: Driver strength support

This field describes if the target supports configurable driver strengths and its associated features. If the device supports NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface, then one and only one of bit 0, bit 3, and bit 4 shall be set. If bit 0, bit 3, and bit 4 are all cleared to zero, then the driver strength at power-on is undefined.

Bit 0 when set to one indicates that the target supports configurable driver strength settings as defined in Table 4-10. If this bit is set to one, then the device shall support both the 35 Ohm and 50 Ohm settings. If this bit is set to one, then the device shall power-on with a driver strength at the 35 Ohm value defined in Table 4-10.

Bit 1 when set to one indicates that the target supports the 25 Ohm setting in Table 4-10 for use in the I/O Drive Strength setting.

Bit 2 when set to one indicates that the target supports the 18 Ohm setting in Table 4-10 for use in the I/O Drive Strength setting.

Bit 3 when set to one indicates that the target supports configurable driver strength settings as defined in Table 4-10. If this bit is set to one, then the device shall support both the 37.5 Ohm and 50 Ohm settings. If this bit is set to one, then the device shall power-on with a driver strength at the 37.5 Ohm value defined in Table 4-10.

Bit 4 when set to one indicates that the target supports configurable driver strength settings as defined in Table 4-10. If this bit is set to one, then the device shall support the 35 Ohm, 37.5 Ohm, and 50 Ohm settings. If this bit is set to one, then the device shall power-on with a driver strength at the 35 Ohm value defined in Table 4-10.

Bits 5-7 are reserved.

5.7.1.36. Byte 158: NV-DDR2/3 and NV-LPDDR4 features

This field describes features and attributes for NV-DDR2 and NV-DDR3 operation. This byte is mandatory when the NV-DDR2 NV-DDR3 or NV-LPDDR4 data interface is supported.

Bit 0 indicates if self-termination ODT is supported. If bit 0 is set to one, then self-termination ODT is supported. If bit 0 is cleared to zero, then self-termination ODT is not supported and the host shall not enable ODT. Refer to section 4.17.

Bit 1 indicates if matrix termination ODT is supported. If bit 1 is set to one, then matrix termination ODT is supported. If bit 1 is cleared to zero, then matrix termination ODT is not supported and the host shall not issue the ODT Configure command. If matrix termination ODT is supported, then the device shall also support self-termination ODT. Refer to section 4.17.

Bit 2 indicates if the optional on-die termination value of 30 Ohms is supported. If bit 2 is set to one, then the on-die termination value of 30 Ohms is supported. If bit 2 is cleared to zero, then the on-die termination value of 30 Ohms is not supported and the host shall not select that value.

Bit 3 indicates if the optional differential signaling for RE_n is supported. If bit 3 is set to one, then differential signaling for RE_n is supported. If bit 3 is cleared to zero, then differential signaling for RE_n is not supported. Refer to section 4.11.2.

Bit 4 indicates if the optional differential signaling for DQS is supported. If bit 4 is set to one, then differential signaling for DQS is supported. If bit 4 is cleared to zero, then differential signaling for DQS is not supported. Refer to section 4.11.2.

Bit 5 indicates if external VREFQ is required for speeds ≥ 200 MT/s. If bit 5 is set to one, then external VREFQ is required and VEN shall be set to one by the host when using timing modes with speeds ≥ 200 MT/s (refer to section 5.31.2). If bit 5 is cleared to zero, then external VREFQ is optional for use by the host when using timing modes with speeds ≥ 200 MT/s.

Bits 6-7 are reserved.

5.7.1.37. Byte 159: NV-DDR2/3 and NV-LPDDR4 warmup cycles

This field describes support for warmup cycles for NV-DDR2 NV-DDR3 or NV-LPDDR4 operation. Warmup cycles are defined in section 4.16. This byte is mandatory when the NV-DDR2 NV-DDR3 or NV-LPDDR4 data interface is supported.

Bits 0-3 indicate the number of warmup cycles that are supported for data output operation. If this field is cleared to 0h, then the target does not support warmup cycles for data output operation. The host shall not configure the target to a number of warmup cycles that exceeds the value provided. Refer to section 5.31.2 for details on configuring the number of warmup cycles for data output.

Bits 4-7 indicate the number of warmup cycles that are supported for data input operation. If this field is cleared to 0h, then the target does not support warmup cycles for data input operation. The host shall not configure the target to a number of warmup cycles that exceeds the value provided. Refer to section 5.31.2 for details on configuring the number of warmup cycles for data input.

5.7.1.38. Byte 160-161: NV-DDR3 timing mode support

This field indicates the NV-DDR3 timing modes supported. If the NV-DDR3 data interface is supported by the target, at least one NV-DDR3 timing mode shall be supported. The target shall support an inclusive range of NV-DDR3 timing modes (i.e. if timing mode n-1 and n+1 are supported, then the target shall also support timing mode n).

Bit 0 when set to one indicates that the target supports NV-DDR3 timing modes 0-3.

Bit 1 when set to one indicates that the target supports NV-DDR3 timing mode 4.

Bit 2 when set to one indicates that the target supports NV-DDR3 timing mode 5.

Bit 3 when set to one indicates that the target supports NV-DDR3 timing mode 6.

Bit 4 when set to one indicates that the target supports NV-DDR3 timing mode 7.

Bit 5 when set to one indicates that the target supports NV-DDR3 timing mode 8.

Bit 6 when set to one indicates that the target supports NV-DDR3 timing mode 9.

Bit 7 when set to one indicates that the target supports NV-DDR3 timing mode 10.

Bit 8 when set to one indicates that the target supports NV-DDR3 timing mode 11.

Bit 9 when set to one indicates that the target supports NV-DDR3 timing mode 12.

Bit 10 when set to one indicates that the target supports NV-DDR3 timing mode 13.

Bit 11 when set to one indicates that the target supports NV-DDR3 timing mode 14.

Bit 12 when set to one indicates that the target supports NV-DDR3 timing mode 15.

Bit 13 when set to one indicates that the target supports NV-DDR3 timing mode 16.

Bit 14 when set to one indicates that the target supports NV-DDR3 timing mode 17.

Bit 15 when set to one indicates that the target supports NV-DDR3 timing mode 18.

5.7.1.39. Byte 162: NV-DDR2 timing mode support

This field is a continuation of Byte 142. This field indicates the NV-DDR2 timing modes supported. If the NV-DDR2 data interface is supported by the target, at least one NV-DDR2 timing mode shall be supported. The target shall support an inclusive range of NV-DDR2 timing modes (i.e. if timing mode n-1 and n+1 are supported, then the target shall also support timing mode n).

Bit 0 when set to one indicates that the target supports NV-DDR2 timing mode 8.

Bit 1 when set to one indicates that the target supports NV-DDR3 timing mode 9.

Bit 2 when set to one indicates that the target supports NV-DDR3 timing mode 10.

Bits 3-7 are reserved and shall be cleared to zero.

5.7.1.40. Byte 164-165: Vendor specific Revision number

This field indicates a vendor specific revision number. This field should be used by vendors to indicate the supported layout for the vendor specific parameter page area and the vendor specific feature addresses. The format of this field is vendor specific.

5.7.1.41. Byte 166-253: Vendor specific

This field is reserved for vendor specific use.

5.7.1.42. Byte 254-255: Integrity CRC

The Integrity CRC (Cyclic Redundancy Check) field is used to verify that the contents of the parameter page were transferred correctly to the host. The CRC of the parameter page is a word (16-bit) field. The CRC calculation covers all of data between byte 0 and byte 253 of the parameter page inclusive.

The CRC shall be calculated on byte (8-bit) quantities starting with byte 0 in the parameter page. The bits in the 8-bit quantity are processed from the most significant bit (bit 7) to the least significant bit (bit 0).

The CRC shall be calculated using the following 16-bit generator polynomial:

$G(X) = X_{16} + X_{15} + X_2 + 1$

This polynomial in hex may be represented as 8005h.

The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

5.7.1.43. Byte 256-511: Redundant Parameter Page 1

This field shall contain the values of bytes 0-255 of the parameter page. Byte 256 is the value of byte 0.

The redundant parameter page is used when the integrity CRC indicates that there was an error in bytes 0-255. The redundant parameter page shall be stored in non-volatile media; the target shall not create these bytes by retransmitting the first 256 bytes.

5.7.1.44. Byte 512-767: Redundant Parameter Page 2

This field shall contain the values of bytes 0-255 of the parameter page. Byte 512 is the value of byte 0.

The redundant parameter page is used when the integrity CRC indicates that there was an error in bytes 0-255 and in the first redundant parameter page. The redundant parameter page shall be stored in non-volatile media; the target shall not create these bytes by retransmitting the first 256 bytes.

5.7.1.45. Byte 768+: Additional Redundant Parameter Pages

Bytes at offset 768 and above may contain additional redundant copies of the parameter page. There is no limit to the number of redundant parameter pages that the target may provide. The target may provide additional copies to guard against the case where all three mandatory copies have invalid CRC checks.

The host should determine whether an additional parameter page is present by checking the first Dword. If at least two out of four bytes match the parameter page signature, then an additional parameter page is present.

5.7.2. Extended Parameter Page Data Structure Definition

The extended parameter page, if present, provides additional information to the host that there was insufficient space to include in the parameter page. The extended parameter page is organized in sections. Each section is a multiple of 16 bytes in length. The section types are specified in Table 5-4.

Section Type	Section Definition
0	Unused section marker. No section present.
1	Section type and length specifiers.
2	Extended ECC information.
3-255	Reserved

Table 5-4 Section Type Definitions

Section types shall be specified in the extended parameter page in order (other than section type value 0). For example, if section type 12 and section type 15 were both present in the extended parameter page then section type 12 shall precede section type 15. There shall only be one instantiation of each section type. All unused sections shall be marked with a section type value of 0. When software encounters a section type value of 0, this marks the end of the valid sections.

Table 5-5 defines the layout of section type 1. Section type 1 specifies additional sections when more than eight sections are present in the extended parameter page. The length of section type 1 shall be a multiple of 16 bytes.

Byte	O/M	Description
0	M	Section 8 type
1	M	Section 8 length
2	O	Section 9 type
3	O	Section 9 length
4	O	Section 10 type
5	O	Section 10 length
6 – (end)	O	Section 11 – n type & lengths

Table 5-5 Section Type 1: Additional Section Type and Length Specifiers

Table 5-6 defines the layout of section type 2. Section type 2 specifies extended ECC information. Each extended ECC information block is eight bytes in length. If an extended ECC information block is not specified, then all values in that block shall be cleared to 0h. The length of section type 2 shall be a multiple of 16 bytes.

Byte	O/M	Description
0-7	M	Extended ECC information block 0
8-15	O	Extended ECC information block 1
16 – (end)	O	Extended ECC information block 2 – n (if present)

Table 5-6 Section Type 2: Extended ECC Information

The definition of the extended ECC information block is specified in section 3.4.

Table 5-7 defines the extended parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte. See section 1.3.2.3 for more information on the representation of word and Dword values.

Values are reported in the extended parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the target will return how many data *bytes* are in a page. For a device that supports 16-bit data access, the host is required to convert byte values to word values for its use.

Unused fields should be cleared to 0h by the target.

Byte	O/M	Description
	Revision information and features block	
0-1	M	Integrity CRC
2-5	M	Extended parameter page signature Byte 0: 45h, “E” Byte 1: 50h, “P” Byte 2: 50h, “P” Byte 3: 53h, “S”
6-15		Reserved (0)
16	M	Section 0 type
17	M	Section 0 length
18	M	Section 1 type
19	M	Section 1 length
20	O	Section 2 type
21	O	Section 2 length
22-31	O	Section 3 – 7 types & lengths
32 – (end)	M	Section information

Table 5-7 Extended Parameter Page definition

5.7.2.1. Byte 0-1: Integrity CRC

The Integrity CRC (Cyclic Redundancy Check) field is used to verify that the contents of the extended parameter page were transferred correctly to the host. The CRC of the extended parameter page is a word (16-bit) field. The CRC calculation covers all of data between byte 2 and the end of the extended parameter page inclusive.

The CRC shall be calculated on byte (8-bit) quantities starting with byte 2 in the extended parameter page to the end of the extended parameter page. The bits in the 8-bit quantity are processed from the most significant bit (bit 7) to the least significant bit (bit 0).

The CRC shall be calculated using the following 16-bit generator polynomial:

$G(X) = X_{16} + X_{15} + X_2 + 1$

This polynomial in hex may be represented as 8005h.

The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

5.7.2.2. Byte 2-5: Extended parameter page signature

This field contains the extended parameter page signature. When two or more bytes of the signature are valid, then it denotes that a valid copy of the extended parameter page is present.

Byte 2 shall be set to 45h.

Byte 3 shall be set to 50h.

Byte 4 shall be set to 50h.

Byte 5 shall be set to 53h.

5.7.2.3. Byte 16: Section 0 type

Section 0 is the first section in the extended parameter page and begins at byte offset 32. This field specifies the type of section 0. Section types are defined in Table 5-4.

5.7.2.4. Byte 17: Section 0 length

Section 0 is the first section in the extended parameter page and begins at byte offset 32. This field specifies the length of section 0. The length is specified in multiples of 16 bytes. Thus, a value of 1 corresponds to 16 bytes and a value of 2 corresponds to 32 bytes.

5.7.2.5. Byte 18: Section 1 type

Section 1 is the second section in the extended parameter page and starts immediately following section 0. This field specifies the type of section 1. Section types are defined in Table 5-4. If section 1 is not present, then the type field shall be cleared to 0.

5.7.2.6. Byte 19: Section 1 length

Section 1 is the second section in the extended parameter page and starts immediately following section 0. This field specifies the length of section 1. The length is specified in multiples of 16 bytes. Thus, a value of 1 corresponds to 16 bytes and a value of 2 corresponds to 32 bytes. If section 1 is not present, then the length field shall be cleared to 0.

5.7.2.7. Byte 20: Section 2 type

Section 2 is the third section in the extended parameter page and starts immediately following section 1. This field specifies the type of section 2. Section types are defined in Table 5-4. If section 2 is not present, then the type field shall be cleared to 0.

5.7.2.8. Byte 21: Section 2 length

Section 2 is the third section in the extended parameter page and starts immediately following section 1. This field specifies the length of section 2. The length is specified in multiples of 16 bytes. Thus, a value of 1 corresponds to 16 bytes and a value of 2 corresponds to 32 bytes. If section 2 is not present, then the length field shall be cleared to 0.

5.7.2.9. Byte 22-31: Section 3 – 7 types and lengths

Bytes 22-31 define the type and lengths for sections 3 – 7 in order, following the same definition and layout as section 0 and 1 type and length definitions. If a section is not present, then the type and length fields for that section shall be cleared to 0.

5.7.2.10. Byte 32 – (end): Section information

Section 0 begins at byte offset 32 and is a multiple of 16 bytes. If there are additional sections (section 1, 2, 3, etc), each section starts immediately following the previous section and is a multiple of 16 bytes.

5.8. Read Unique ID Definition

The Read Unique ID function is used to retrieve the 16 byte unique ID (UID) for the device. The unique ID when combined with the device manufacturer shall be unique.

The UID data may be stored within the Flash array. To allow the host to determine if the UID is without bit errors, the UID is returned with its complement, as shown in Table 5-8. If the XOR of the UID and its bit-wise complement is all ones, then the UID is valid.

Bytes	Value
0-15	UID
16-31	UID complement (bit-wise)

Table 5-8 UID and Complement

To accommodate robust retrieval of the UID in the case of bit errors, sixteen copies of the UID and the corresponding complement shall be stored by the target. For example, reading bytes 32-63 returns to the host another copy of the UID and its complement.

Read Status Enhanced shall not be used during execution of the Read Unique ID command.

Figure 5-14 defines the Read Unique ID behavior. The host may use any timing mode supported by the target in order to retrieve the UID data.

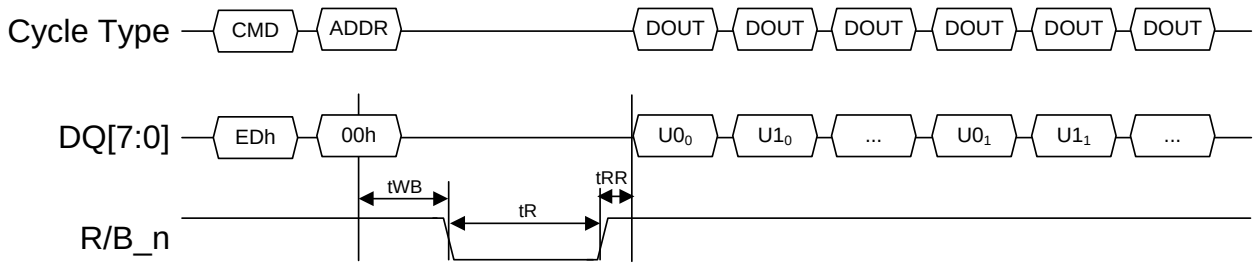


Figure 5-14 Read Unique ID command timing

$U0_k$-Un_k The kth copy of the UID and its complement. Sixteen copies are stored. Reading beyond 512 bytes returns indeterminate values.

5.9. Block Erase Definition

The Block Erase function erases the block of data identified by the block address parameter on the LUN specified. A Block Erase operation shall be considered successful if SR[0] returns a zero after completion of the Block Erase operation. SR[0] is valid for this command after SR[6] transitions from zero to one until the next transition of SR[6] to zero. Figure 5-15 defines the Block Erase behavior and timings.

If the host attempts to erase a factory marked bad block, then the device shall not proceed with the requested operation and shall set the FAIL bit to one for the operation.

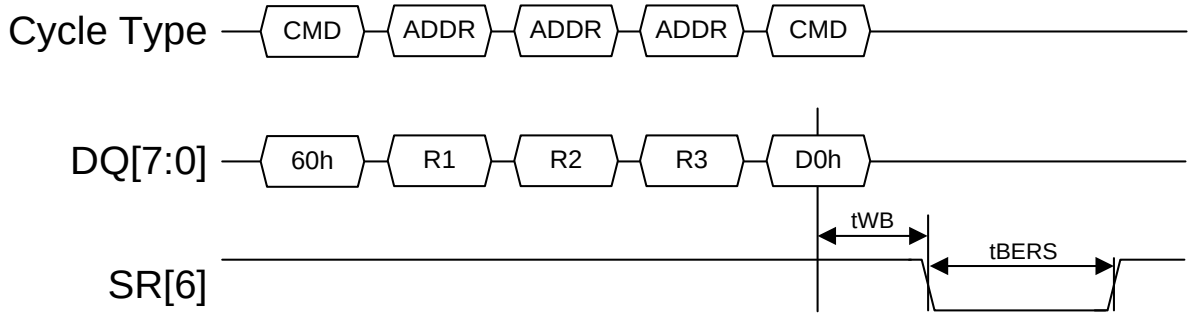


Figure 5-15 Block Erase timing

R1-R3 The row address of the block to be erased. R1 is the least significant byte in the row address.

5.10. Read Status Definition

In the case of non-multi-plane operations, the Read Status function retrieves a status value for the last operation issued. If multiple multi-plane operations are in progress on a single LUN, then Read Status returns the composite status value for status register bits that are independent per plane address. Specifically, Read Status shall return the combined status value of the independent status register bits according to Table 5-9. See section 5.13 for status register bit definitions.

Status Register bit	Composite status value
Bit 0, FAIL	OR
Bit 1, FAILC	OR
Bit 3, CSP	OR

Table 5-9 Composite Status Value

When issuing Read Status in the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface, each data byte is received twice. The host shall only latch one copy of each data byte. See section 4.4.

Figure 5-16 defines the Read Status behavior and timings.

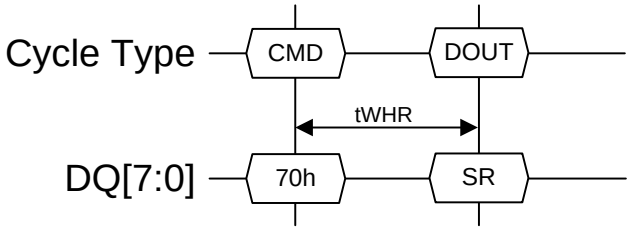


Figure 5-16 Read Status timing

SR Status value as defined in section 5.13.

The Read Status command may be issued using either the SDR, NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interfaces. The timing parameters for each data interface are shown in Figure 5-17, Figure 5-18, and Figure 5-19.

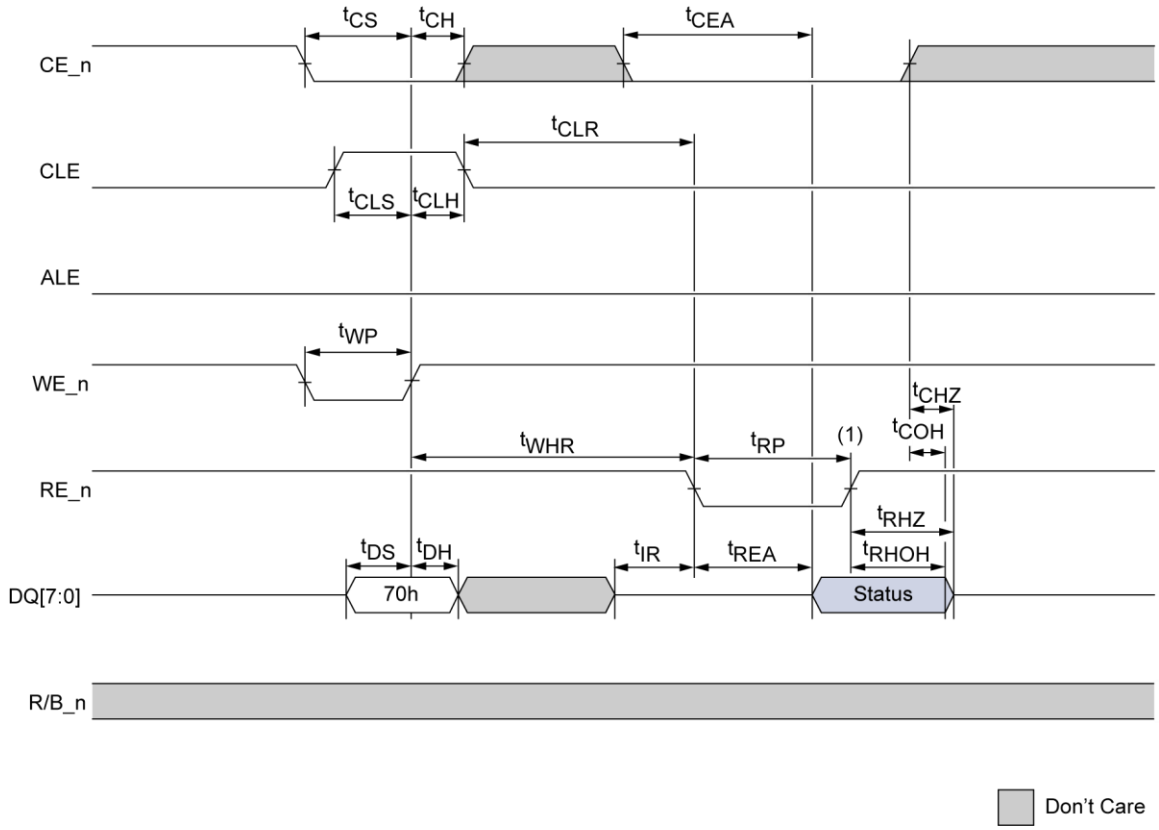


Figure 5-17 Read Status command using SDR data interface

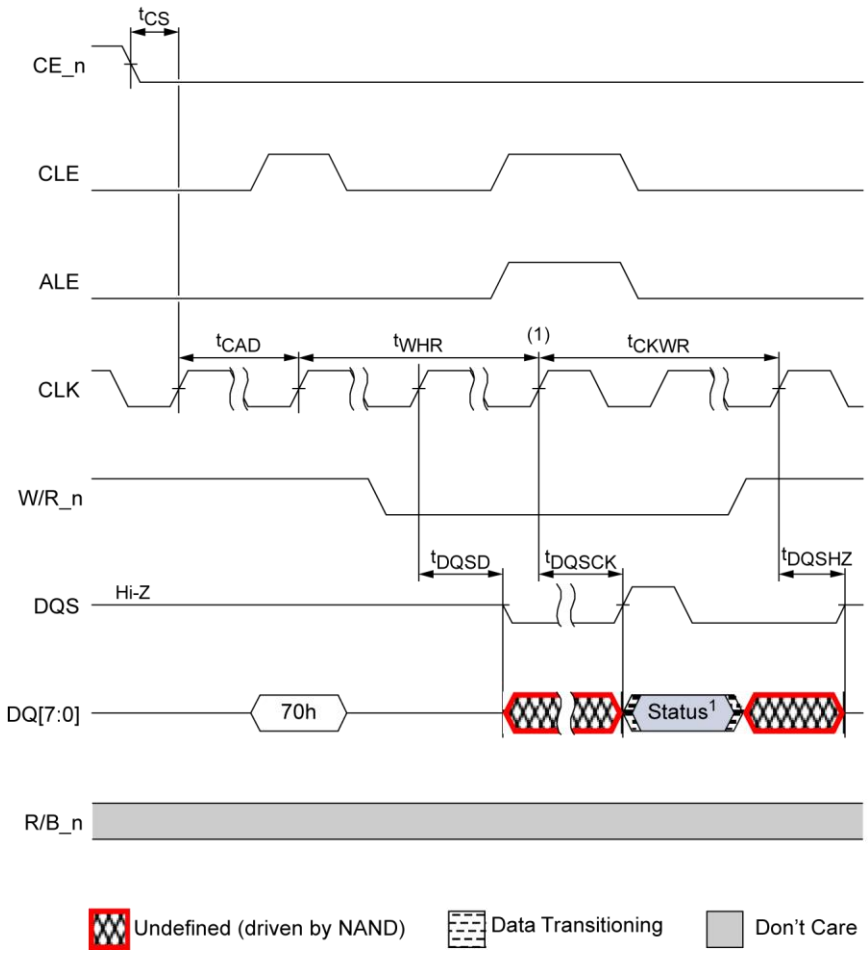


Figure 5-18 Read Status command using NV-DDR data interface

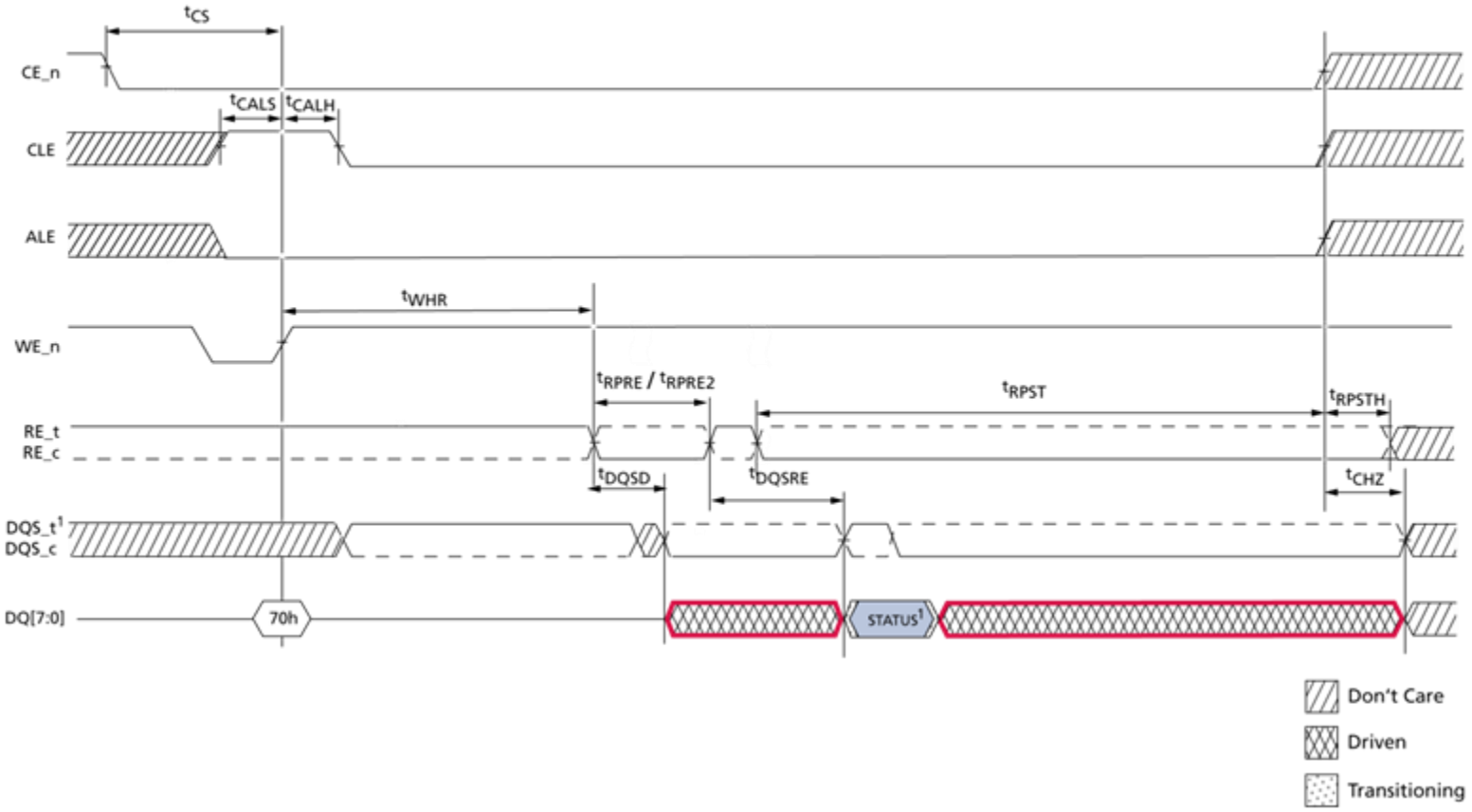


Figure 5-19 Read Status command using NV-DDR2/3 and NV-LPDDR4 data interface

NOTE 1: For the SDR data interface, status may be continually read by pulsing RE_n or leaving RE_n low. For the NV-DDR interface, status may continually be read by leaving ALE/CLE at a value of 11b. For the NV-DDR2/3 and NV-LPDDR4 interface, it is optional for the device to update status while RE_n is held low. If the device supports updating status while RE_n is held low, then the host may continually read updated status as the DQ[7:0] data values are updated. However, DQS only transitions based on RE_n transitions. If the device does not support updating status while RE_n is held low, then the status will be updated based on RE_n transitions. In Figure 5-19, when the bus state is not a data input or data output cycle, if ALE, CLE and CE_n are all low (i.e. Idle state) then DQS (DQS_t) shall be held high by the host to prevent the device from enabling ODT. If ODT is disabled, then DQS is a don't care during Idle states.

5.11. Read Status Enhanced Definition

The Read Status Enhanced function retrieves the status value for a previous operation on the particular LUN and plane address specified. Figure 5-20 defines the Read Status Enhanced behavior and timings. If the row address entered is invalid, the Status value returned has an indeterminate value. The host uses Read Status Enhanced for LUN selection (refer to section 3.1.2). Note that Read Status Enhanced has no effect on which page register is selected for data output within the LUN.

When issuing Read Status Enhanced in the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface, each data byte is received twice. The host shall only latch one copy of each data byte. See section 4.4.

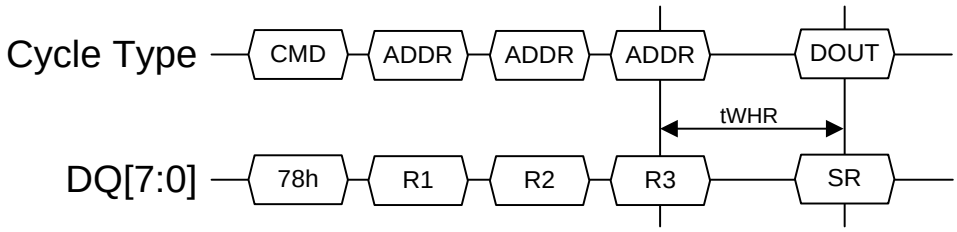


Figure 5-20 Read Status Enhanced timing

R1-R3 Row address that contains the LUN and plane address to retrieve status for. Row address bits not associated with the LUN and plane address are not used. R1 is the least significant byte.

SR Status value as defined in section 5.13.

5.12. Read Status and Read Status Enhanced required usage

In certain sequences only one status command shall be used by the host. This section outlines situations in which a particular status command is required to be used.

If a command is issued to a LUN while R/B_n is cleared to zero, then the next status command shall be Read Status Enhanced. Read Status Enhanced causes LUNs that are not selected to turn off their output buffers. This ensures that only the LUN selected by the Read Status Enhanced commands responds to a subsequent toggle of the RE_n input signal.

When the host has issued Read Page commands to multiple LUNs at the same time, the host shall issue Read Status Enhanced before reading data from either LUN. Read Status Enhanced causes LUNs that are not selected to turn off their output buffers. This ensures that only the LUN

selected by the Read Status Enhanced commands responds to a subsequent toggle of the RE_n input signal after data output is selected with the 00h command (NOTE: Some NAND vendors may require the use of Change Read Column sequence instead of 00h command to output data from the NAND, see vendor datasheet) . Refer to section 3.1.3 for additional requirements if a Change Read Column (Enhanced) command is used as part of a multiple LUN read sequence.

During and after Target level commands, the host shall not issue the Read Status Enhanced command. In these sequences, the host uses Read Status to check for the status value. The only exception to this requirement is if commands were outstanding to multiple LUNs when a Reset was issued. In this case, the Read Status Enhanced command shall be used to determine when each active LUN has completed Reset.

5.13. Status Field Definition

The returned status register byte value (SR) for Read Status and Read Status Enhanced has the format described below. If the RDY bit is cleared to zero, all other bits in the status byte (except WP_n) are invalid and shall be ignored by the host.

Value	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Status Register	WP_n	RDY	ARDY	VSP	VSP	VSP	FAILC	FAIL

FAIL If set to one, then the last command failed. If cleared to zero, then the last command was successful. This bit is only valid for program and erase operations. During program cache operations, this bit is only valid when ARDY is set to one. In devices that support ZQ calibration, this bit is set to one if the ZQ calibration operation failed.

FAILC If set to one, then the command issued prior to the last command failed. If cleared to zero, then the command issued prior to the last command was successful. This bit is only valid for program cache operations. This bit is not valid until after the second 15h command or the 10h command has been transferred in a Page Cache Program sequence. When program cache is not supported, this bit is not used and shall be cleared to zero.

ARDY If set to one, then there is no array operation in progress. If cleared to zero, then there is a command being processed (RDY is cleared to zero) or an array operation in progress. When overlapped multi-plane operations or cache commands are not supported, this bit is not used.

RDY If set to one, then the LUN or plane address is ready for another command and all other bits in the status value are valid. If cleared to zero, then the last command issued is not yet complete and SR bits 5:0 are invalid and shall be ignored by the host. This bit impacts the value of R/B_n, refer to section 2.18.2. When caching operations are in use, then this bit indicates whether another command can be accepted, and ARDY indicates whether the last operation is complete.

WP_n If set to one, then the device is not write protected. If cleared to zero, then the device is write protected. This bit shall always be valid regardless of the state of the RDY bit.

R Reserved (0)

VSP Vendor Specific

5.14. Read Definition

The Read function reads a page of data identified by a row address for the LUN specified. The page of data is made available to be read from the page register starting at the column address specified. Figure 5-21 defines the Read behavior and timings. Reading beyond the end of a page results in indeterminate values being returned to the host.

While monitoring the read status to determine when the tR (transfer from Flash array to page register) is complete, the host shall re-issue a command value of 00h to start reading data (NOTE: Some NAND vendors may require the use of Change Read Column sequence instead of 00h command to output data from the NAND, see vendor datasheet). Issuing a command value of 00h will cause data to be returned starting at the selected column address.

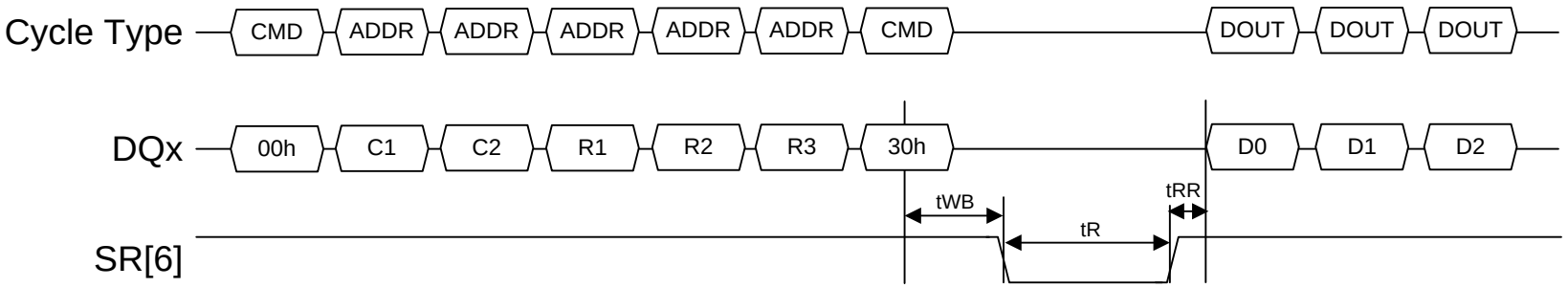


Figure 5-21 Read timing

C1-C2 Column address of the page to retrieve. C1 is the least significant byte.

R1-R3 Row address of the page to retrieve. R1 is the least significant byte.

Dn Data bytes read from the addressed page.

5.15. Read Cache Definition

The Read Cache Sequential and Read Cache Random functions permit a page to be read from the page register while another page is simultaneously read from the Flash array for the selected LUN. A Read Page command, as defined in section 5.14, shall be issued prior to the initial Read Cache Sequential or Read Cache Random command in a read cache sequence. A Read Cache Sequential or Read Cache Random command shall be issued prior to a Read Cache End (3Fh) command being issued.

The Read Cache (Sequential or Random) function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Read Cache (Sequential or Random) function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Read Cache (Sequential or Random) function. Issuing an additional Read Cache (Sequential or Random) function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command. The host may begin to read data from the page register when SR[6]is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array.

The host shall not issue a Read Cache Sequential (31h) command after the last page of a block is read. If commands are issued to multiple LUNs at the same time, the host shall execute a Read Status Enhanced (78h) command to select the LUN prior to issuing a Read Cache Sequential (31h) or Read Cache End (3Fh) command for that LUN.

Figure 5-22 defines the Read Cache Sequential behavior and timings for the beginning of the cache operations subsequent to a Read command being issued to the target. Figure 5-23 defines the Read Cache Random behavior and timings for the beginning of the cache operations subsequent to a Read command being issued to the target. In each case, SR[6] conveys whether the next selected page can be read from the page register.

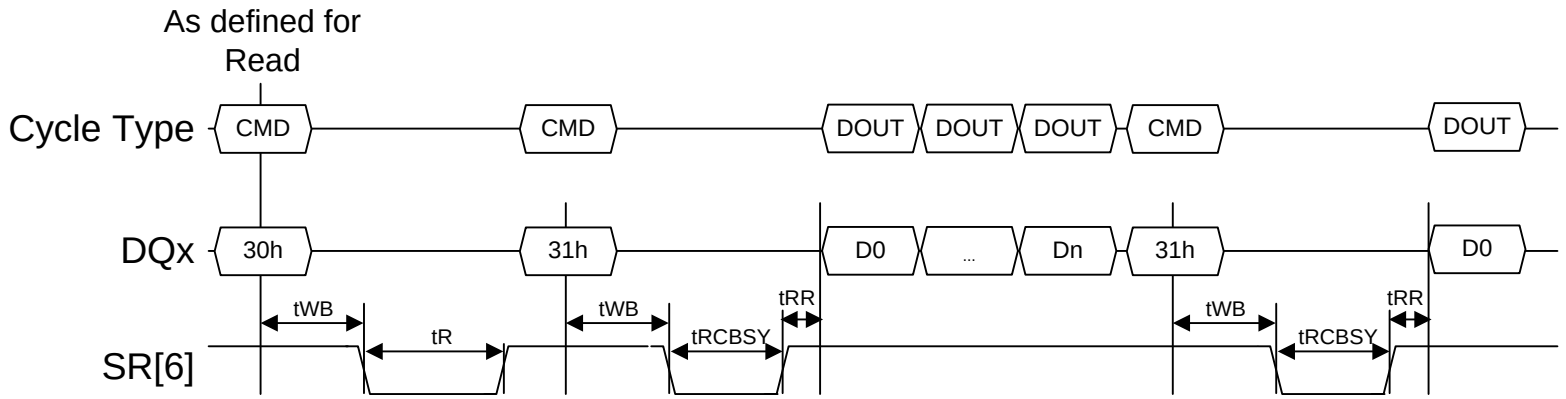


Figure 5-22 Read Cache Sequential timing, start of cache operations

D0-Dn Data bytes/words read from page requested by the original Read or the previous cache operation.

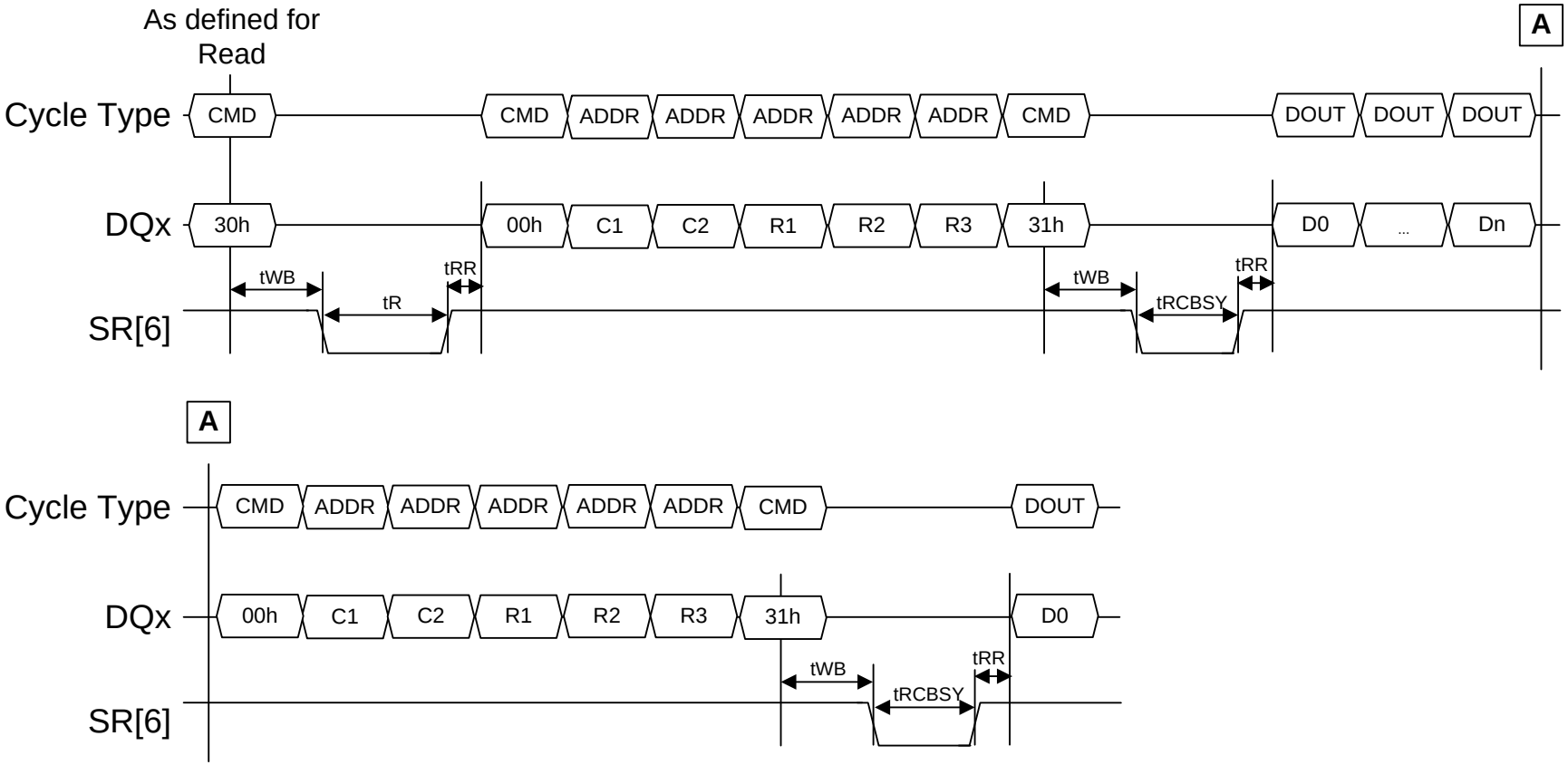


Figure 5-23 Read Cache Random timing, start of cache operations

C1-C2 Column address of the page to retrieve. C1 is the least significant byte. The column address is ignored.

R1-R3 Row address of the page to retrieve. R1 is the least significant byte.

D0-Dn Data bytes/words read from page requested by the original Read or the previous cache operation

Figure 5-24 defines the Read Cache (Sequential or Random) behavior and timings for the end of cache operations. This applies for both Read Cache Sequential and Read Cache Random. A command code of 3Fh indicates to the target to transfer the final selected page into the page register, without beginning another background read operation.

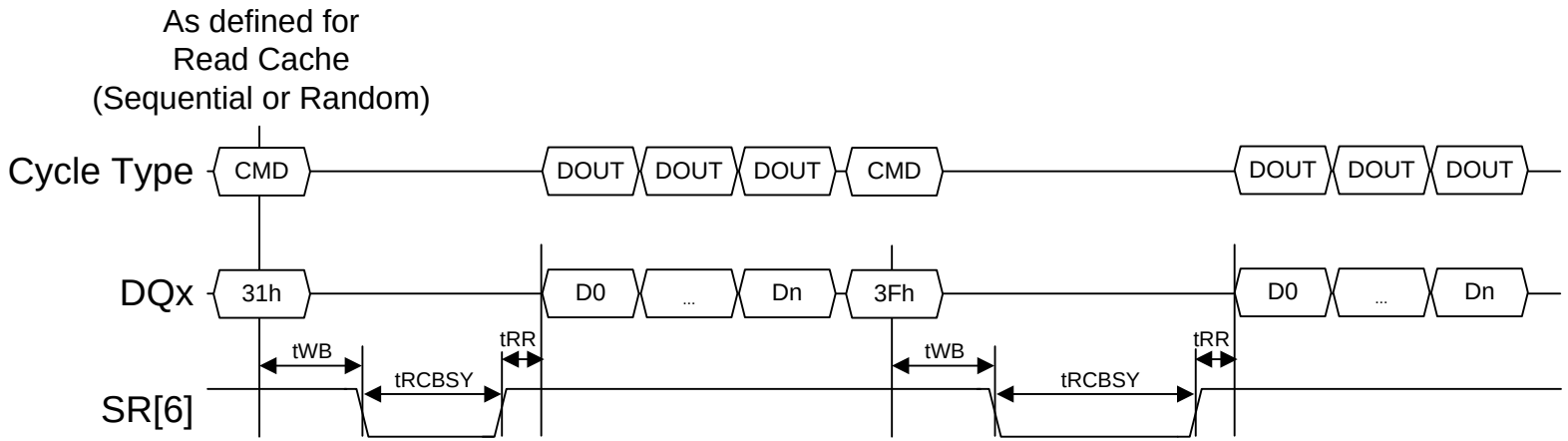


Figure 5-24 Read Cache timing, end of cache operations

D0-Dn Data bytes/words read from page requested by the previous cache operation.

5.16. Page Program Definition

The Page Program command transfers a page or portion of a page of data identified by a column address to the page register. The contents of the page register are then programmed into the Flash array at the row address indicated. SR[0] is valid for this command after SR[6] transitions from zero to one until the next transition of SR[6] to zero. Figure 5-25 defines the Page Program behavior and timings. Writing beyond the end of the page register is undefined.

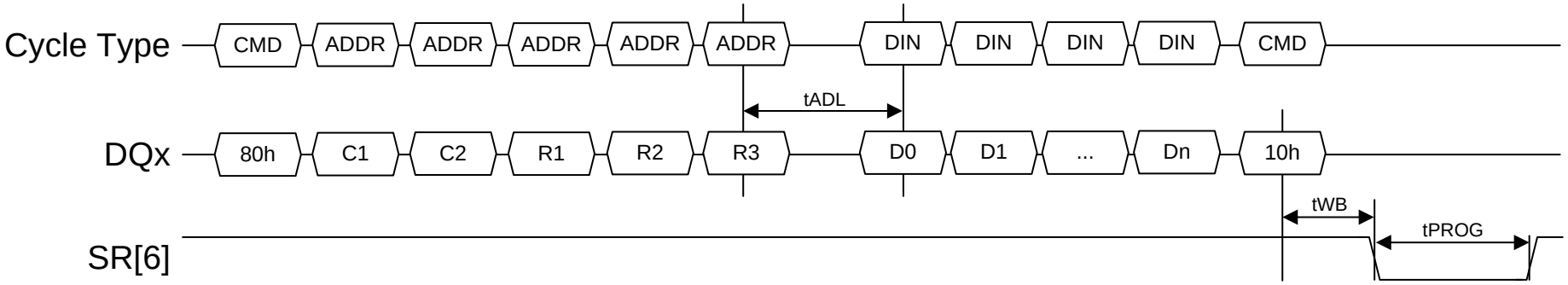


Figure 5-25 Page Program timing

C1-C2 Column address of the starting buffer location to write data to. C1 is the least significant byte.

R1-R3 Row address of the page being programmed. R1 is the least significant byte.

D0-Dn Data bytes/words to be written to the addressed page.

5.17. Page Cache Program Definition

The Page Cache Program function permits a page or portion of a page of data to be written to the Flash array for the specified LUN in the background while the next page to program is transferred by the host to the page register. Figure 5-26, Figure 5-27, and Figure 5-28 define the Page Cache Program behavior and timings.

The 10h command may be used to end the Page Cache Program sequence. After the 10h command is issued, all data is written to the Flash array prior to when SR[5] (ARDY) and SR[6] (RDY) transition from zero to one within tPROG time (see Figure 5-27).

The 15h command may also be used to end the Page Cache Program sequence. If a 15h command is used to end the Page Cache Program sequence, SR[6] (RDY) transitions from zero to one within tPCBSY time, but SR[5] (ARDY) transitions from zero to one within tPROG time (see Figure 5-28).

NAND devices may support both or only one of 10h and 15h commands to end the Page Cache Program Sequence. Please refer to the vendor datasheet for information on what Page Cache Program sequence ending command/s is/are supported by a device.

SR[0] (FAIL) is valid after SR[5] (ARDY) transitions from zero to one until the next transition. SR[1] (FAILC) is valid after SR[6] (RDY) transitions from zero to one, and this is not the first operation.

Note that tPROG at the end of the caching operation may be longer than typical as this time also accounts for completing the programming operation for the previous page. Writing beyond the end of the page register is undefined.

If the program page register clear enhancement is supported, then the host may choose to only clear the page register for the selected LUN and plane address when a Program (80h) command is received. Refer to section 5.31.1 for details on how to enable this feature.

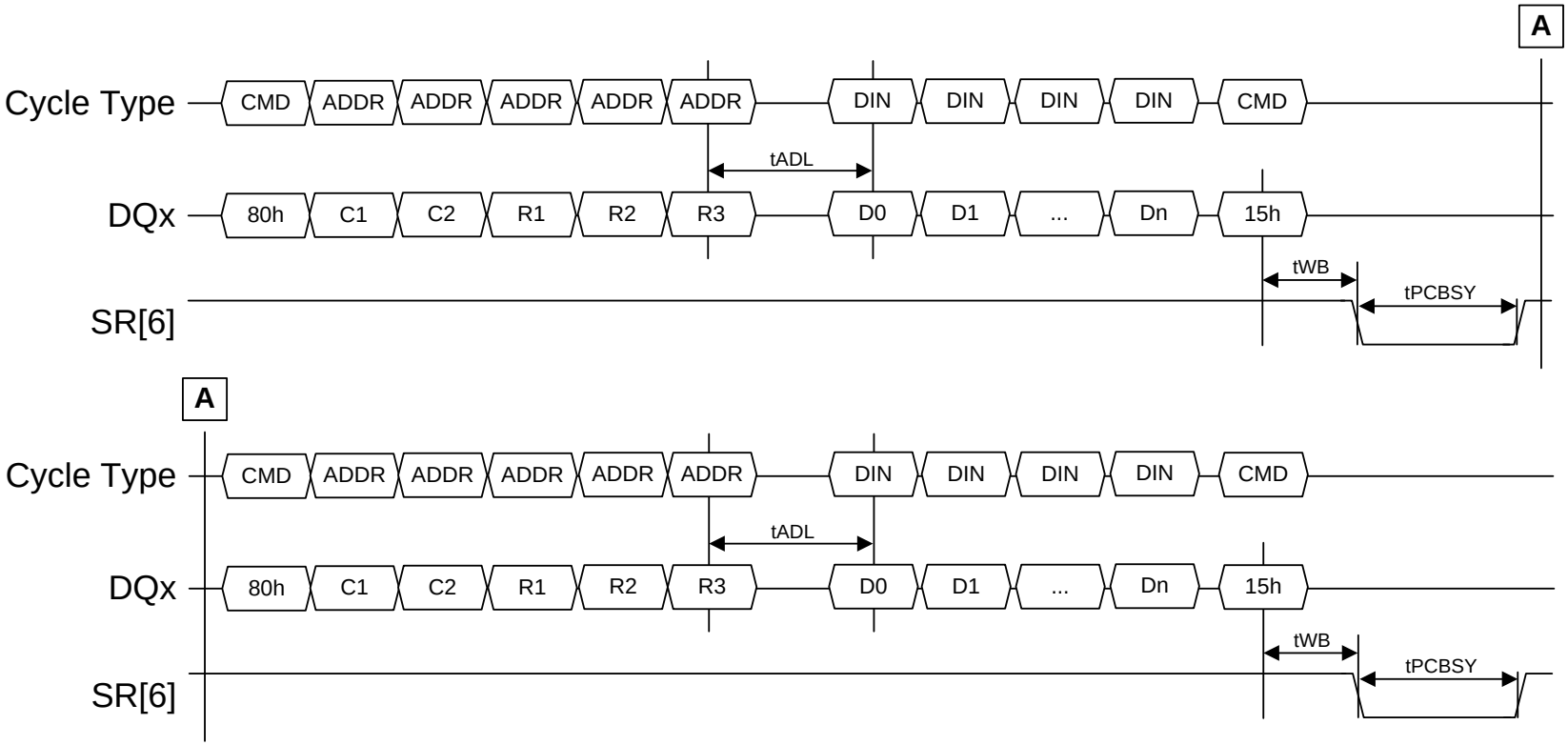


Figure 5-26 Page Cache Program timing, start of operations

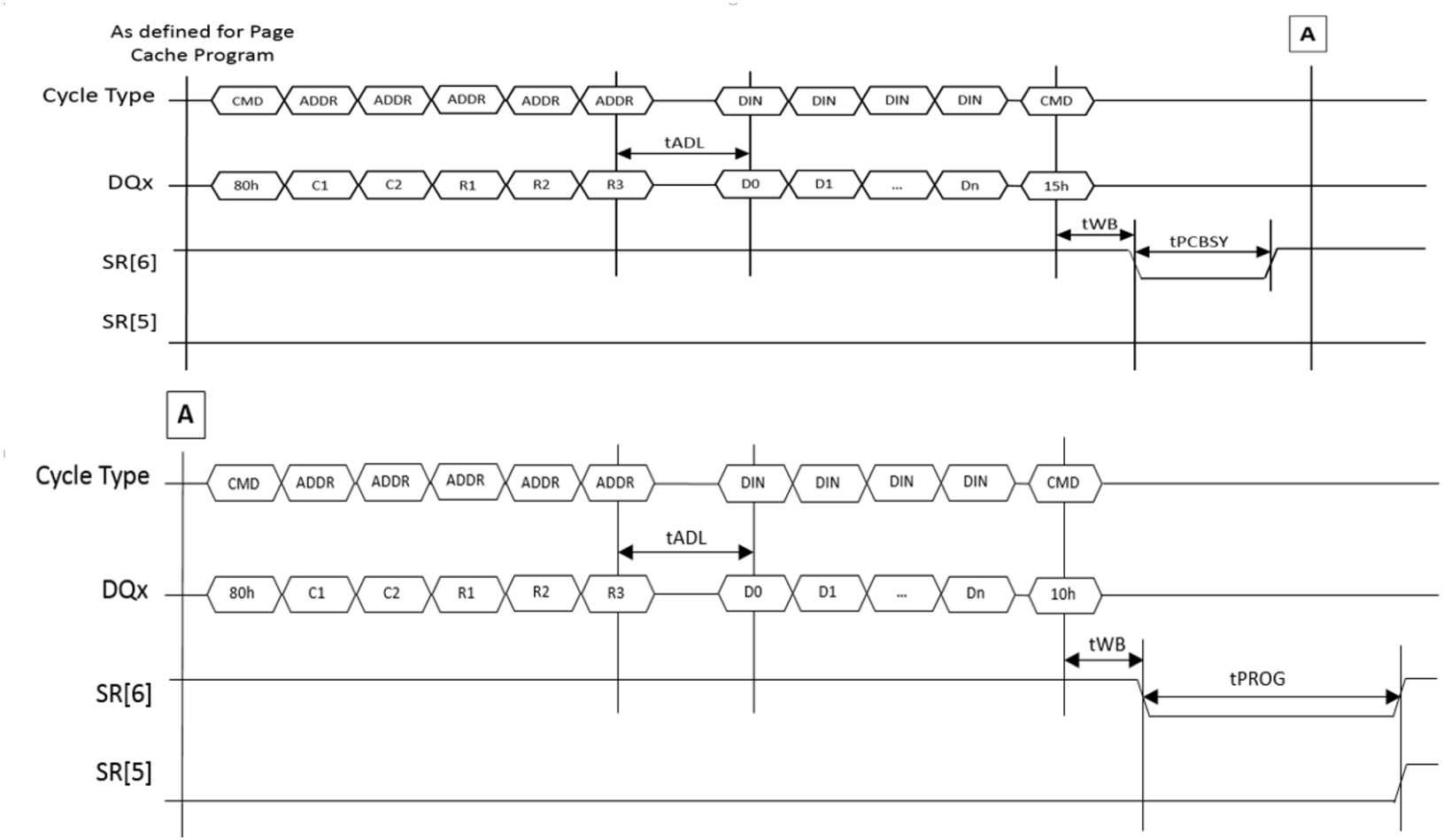


Figure 5-27 Page Cache Program timing, end of operations using 10h

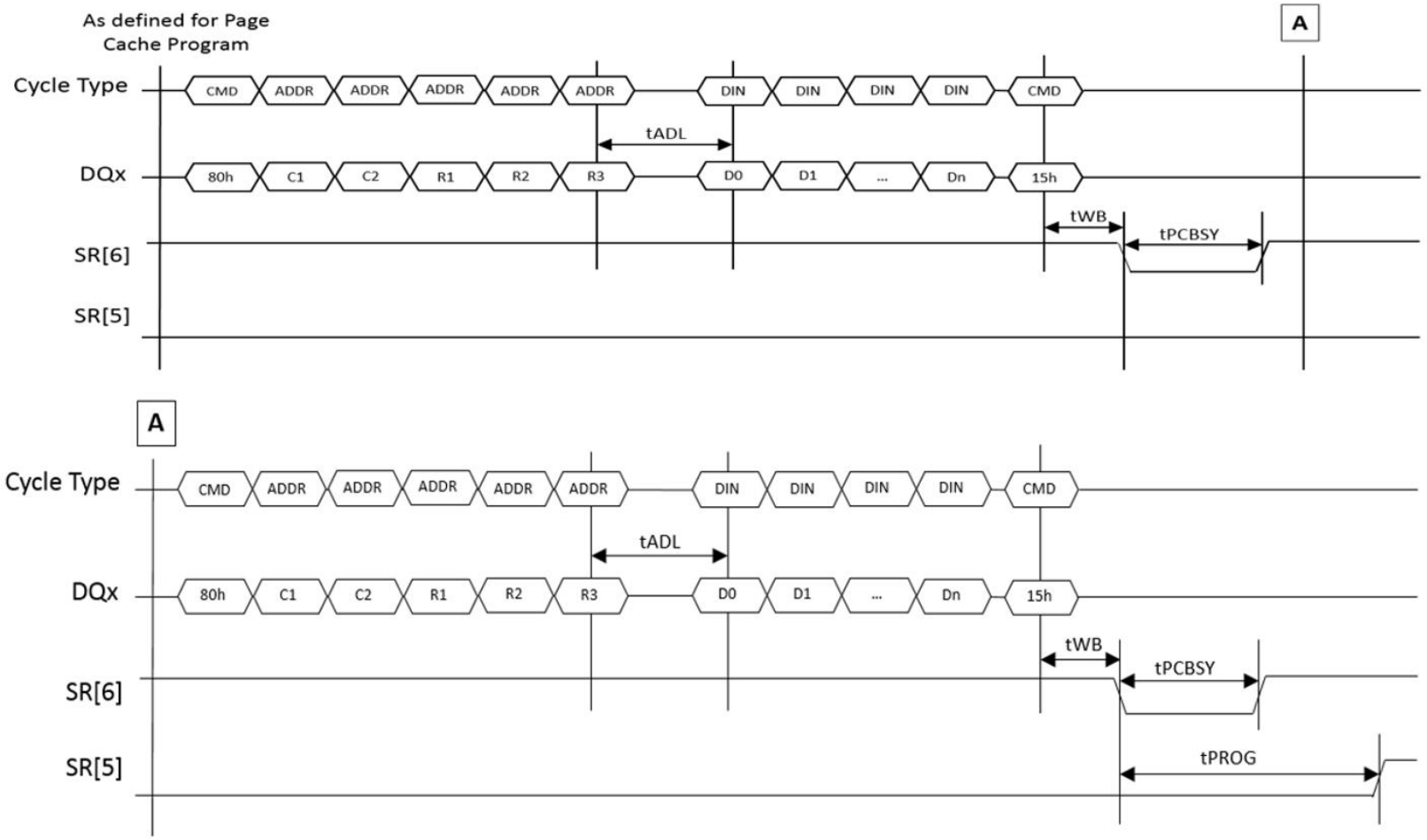


Figure 5-28 Page Cache Program timing, end of operations using 15h

C1-C2 Column address of the starting buffer location to write data to. C1 is the least significant byte.

R1-R3 Row address of the page being programmed. R1 is the least significant byte.

D0-Dn Data bytes/words to be written to the addressed page.

5.18. Copyback Definition

The Copyback function reads a page of data from one location and then moves that data to a second location on the same LUN. Refer to the parameter page to determine the destinations support for Copyback. The data read from the first location may be read by the host, including use of Change Read Column. After completing any data read out and issuing Copyback Program, the host may perform data modification using Change Write Column as needed. Figure 5-29 defines the Copyback behavior and timings.

Copyback uses a single page register for the read and program operation.

When multi-plane addressing is supported, the multi-plane address for Copyback Read and Copyback Program for a non-multi-plane Copyback operation shall be the same.

Copyback may also have odd/even page restrictions. Specifically, when reading from an odd page, the contents may need to be written to an odd page. Alternatively, when reading from an even page, the contents may need to be written to an even page. Refer to section 5.7.1.3.

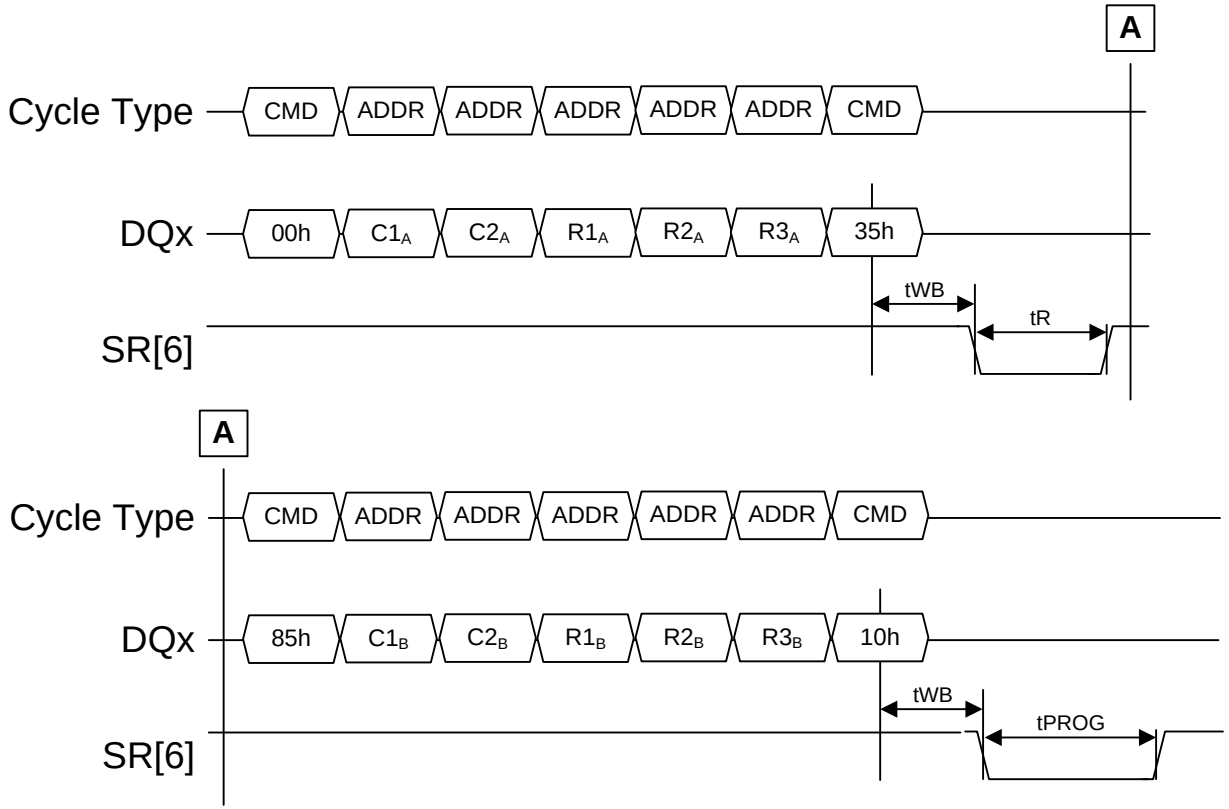


Figure 5-29 Copyback timing

$C1_A$-$C2_A$	Column address of the page to retrieve. $C1_A$ is the least significant byte.
$R1_A$-$R3_A$	Row address of the page to retrieve. $R1_A$ is the least significant byte.
$C1_B$-$C2_B$	Column address of the page to program. $C1_B$ is the least significant byte.
$R1_B$-$R3_B$	Row address of the page to program. $R1_B$ is the least significant byte.

Figure 5-30 and Figure 5-31 define Copyback support for data output and data modification.

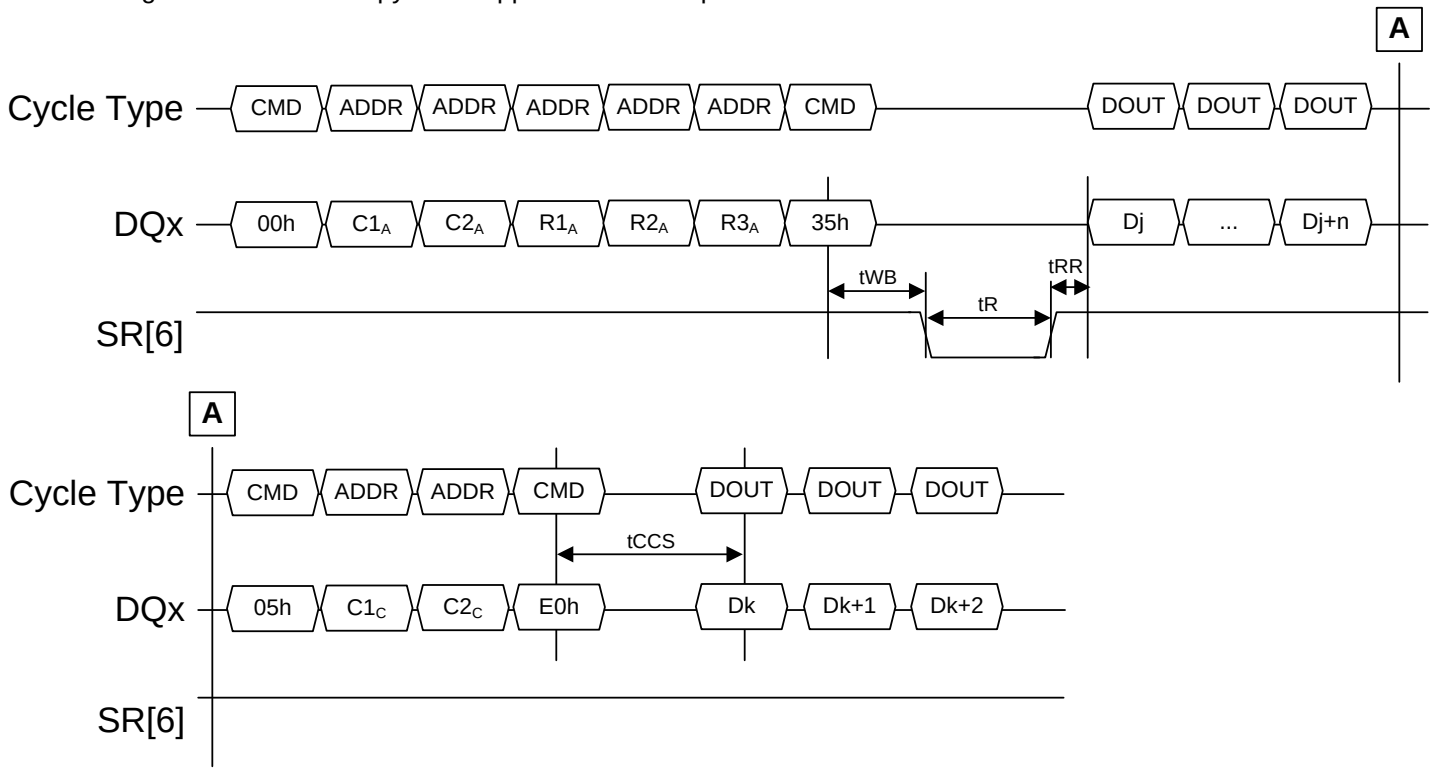


Figure 5-30 Copyback Read with data output

C1 A-C2A Column address of the page to retrieve. C1A is the least significant byte.

R1 A-R3A Row address of the page to retrieve. R1A is the least significant byte.

Dj-(Dj+n) Data bytes read starting at column address specified in C1-C2A.

C1 C-C2C Column address of new location (k) to read out from the page register. C1C is the least significant byte.

Dk-Dk+n Data bytes read starting at column address specified in C1-C2C.

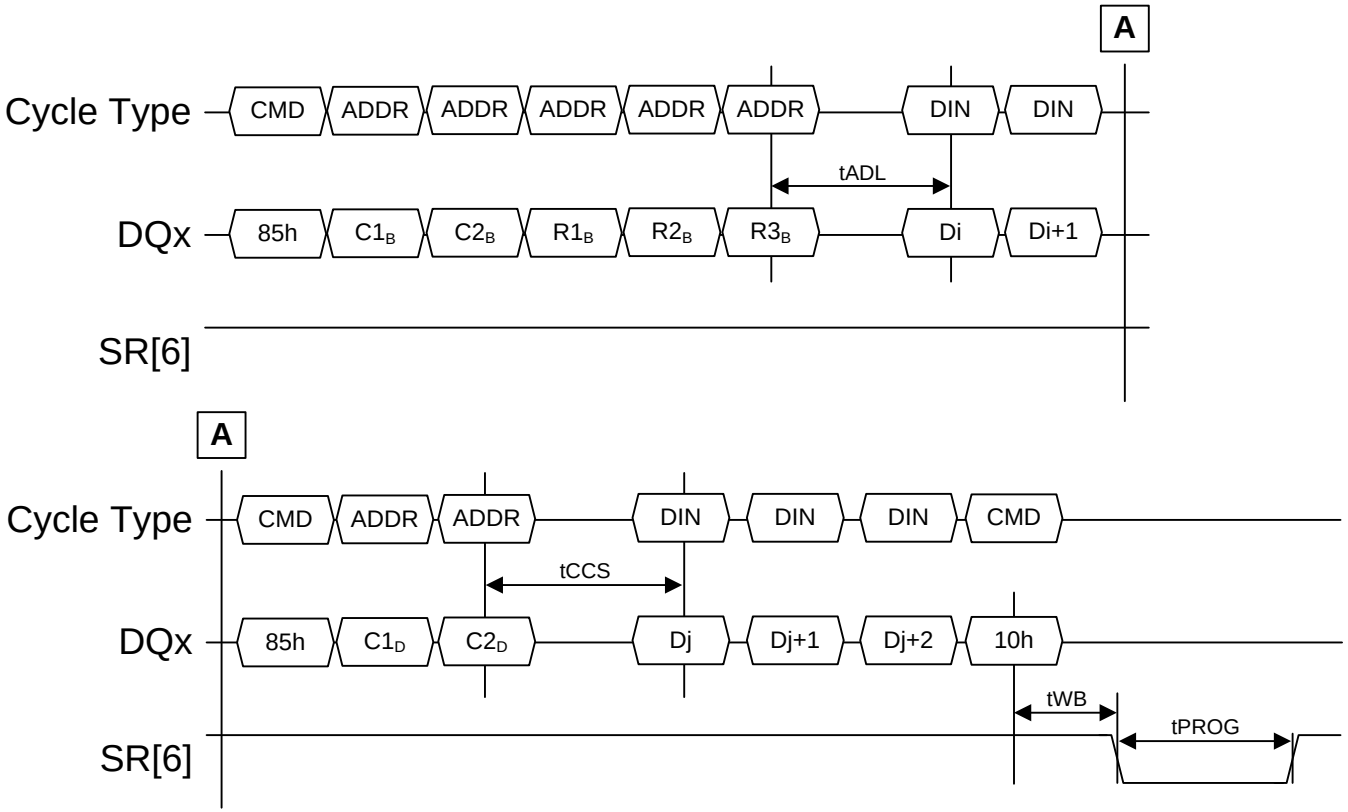


Figure 5-31 Copyback Program with data modification

$C1_B$-$C2_B$ Column address of the page to program. $C1_B$ is the least significant byte.

$R1_B$-$R3_B$ Row address of the page to program. $R1_B$ is the least significant byte.

Di-Di+n Data bytes overwritten in page register starting at column address specified in C1-$C2_B$.

$C1_D$-$C2_D$ Column address of new location (j) to overwrite data at in the page register. $C1_D$ is the least significant byte.

Dj-Dj+n Data bytes overwritten starting at column address specified in C1-$C2_D$

5.19. Small Data Move

If the Small Data Move command is supported, as indicated in the parameter page, then the host may transfer data to the page register in increments that are less than the page size of the device for both Program and Copyback operations (including multi-plane Program and Copyback operations). The host may also read data out as part of the operation. If the Small Data Move is a program operation with no data output, then the 80h opcode may be used for the first cycles. For Copyback and program operations that include data output, the 85h opcode shall be used for the first cycles.

Figure 5-32 defines the data modification portion of a Program or Copyback Program with small data moves; this sequence may be repeated as necessary to complete the data transfer. Figure 5-33 defines the final program operation that is used to complete the Program or Copyback Program with small data move operation. The row address ($R1_B$ – $R3_B$) shall be the same for all program portions of the sequence destined for the same plane address. The function of the 11h command in a small data move operation is to flush any internal data pipeline in the device prior to resuming data output.

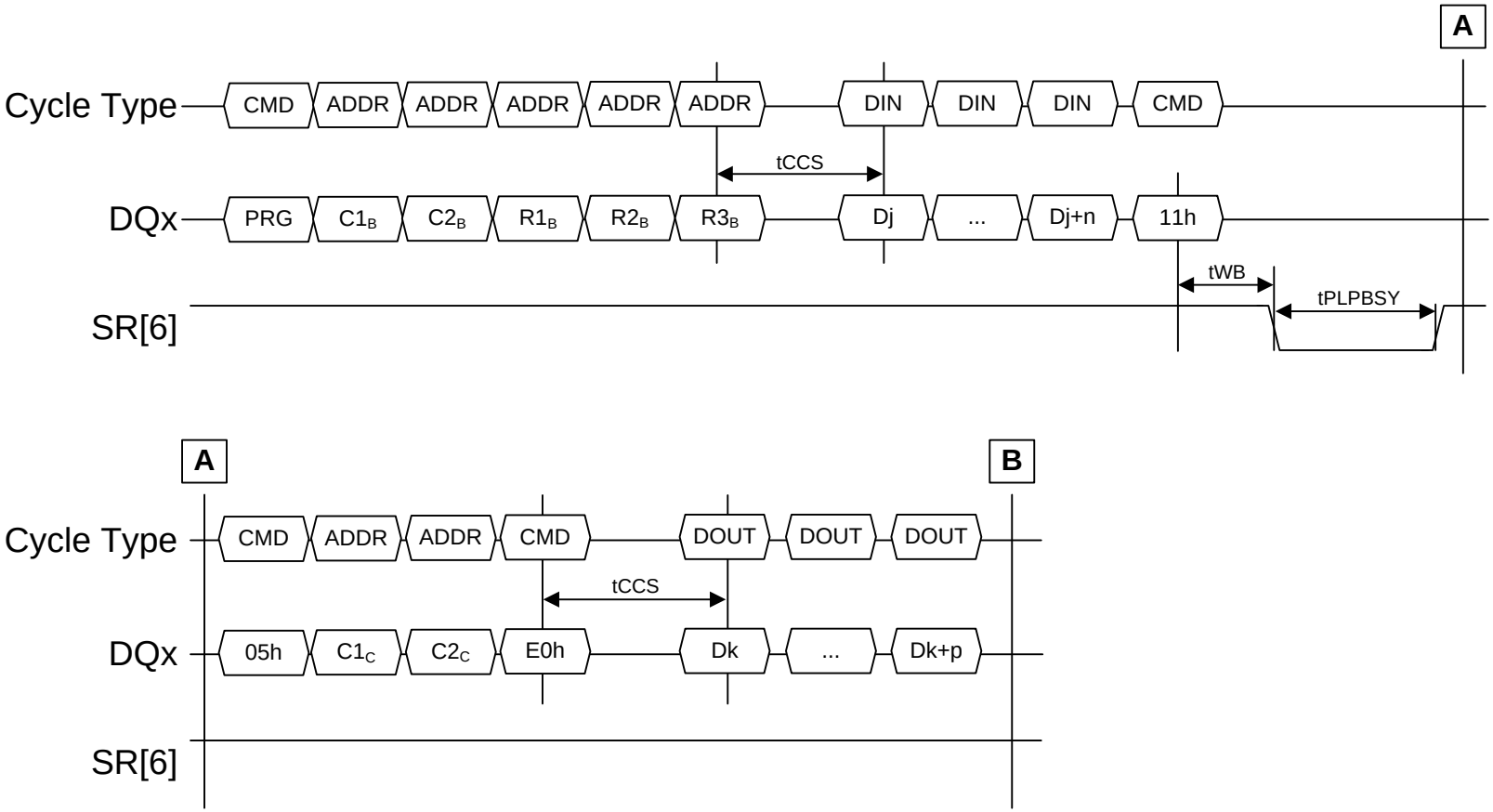


Figure 5-32 Small data moves, data modification

PRG Program command, either 80h or 85h. Following any data output, the command shall be 85h.

C1-C2$_B$ Column address to write to in the page register. C1$_B$ is the least significant byte.

R1-R3$_B$ Row address of the page to program. R1$_B$ is the least significant byte.

Dj-(Dj+n) Data bytes to update in the page register starting at column address specified in C1-C2$_B$.

C1-C2$_C$ Column address of the byte/word in the page register to retrieve. C1$_C$ is the least significant byte.

Dk-(Dk+p) Data bytes read starting at column address specified in C1-C2$_C$.

NOTE: If Change Read Column Enhanced is supported, this command may be substituted for Change Read Column in Figure 5-32. Use of the Change Read Column (Enhanced) command and data output in this flow is optional; this flow may be used to incrementally transfer data for a Program or Copyback Program.

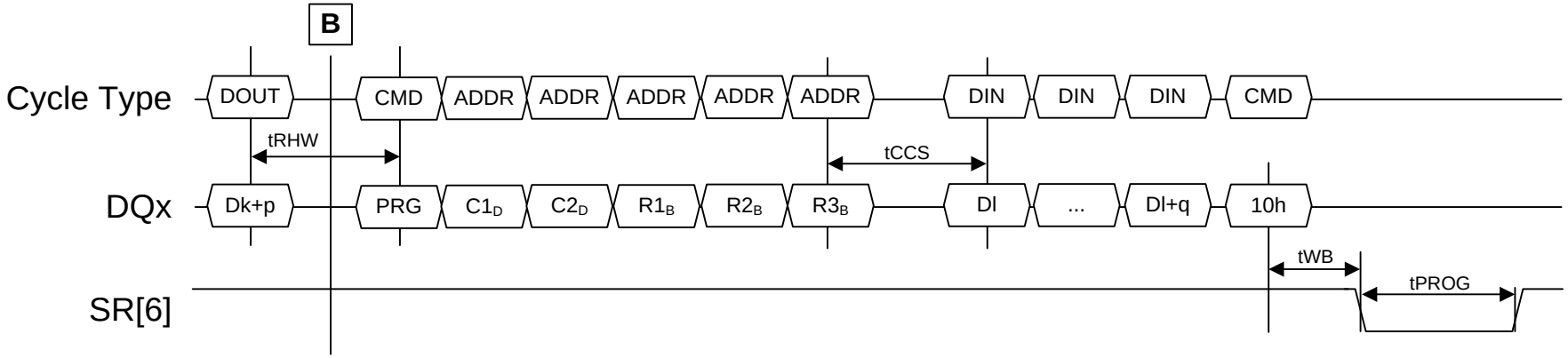


Figure 5-33 Small data moves, end

PRG Program command, either 80h or 85h. 85h shall be used if there is any data output as part of the command.

C1-$C2_D$ Column address to write to in the page register. $C1_D$ is the least significant byte.

R1-$R3_B$ Row address of the page to program. $R1_B$ is the least significant byte.

Dl-(Dl+q) Data bytes to update in the page register starting at column address specified in C1-$C2_D$.

5.20. Change Read Column Definition

The Change Read Column function changes the column address from which data is being read in the page register for the selected LUN. Change Read Column shall only be issued when the LUN is in a read idle condition. Figure 5-34 defines the Change Read Column behavior and timings.

The host shall not read data from the LUN until tCCS ns after the E0h command is written to the LUN. Refer to Figure 5-34.

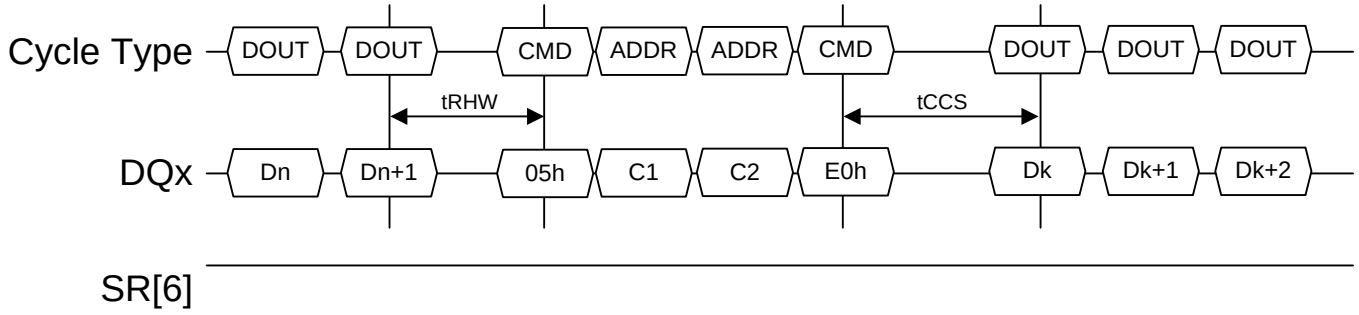


Figure 5-34 Change Read Column timing

Dn Data bytes read prior to the column address change.

C1-C2 New column address to be set for subsequent data transfers. C1 is the least significant byte.

Dk Data bytes being read starting with the new addressed column.

5.21. Change Read Column Enhanced Definition

The Change Read Column Enhanced function changes the LUN address, plane address and column address from which data is being read in a page previously retrieved with the Read command. This command is used when independent LUN operations or multi-plane operations are being performed such that the entire address for the new column needs to be given. Figure 5-35 defines the Change Read Column Enhanced behavior and timings.

The Change Read Column Enhanced command shall not be issued by the host unless it is supported as indicated in the parameter page. Change Read Column Enhanced shall not be issued while Target level data output commands (Read ID, Read Parameter Page, Read Unique ID, Get Features) are executing or immediately following Target level commands.

Change Read Column Enhanced causes idle LUNs (SR[6] is one) that are not selected to turn off their output buffers. This ensures that only the LUN selected by the Change Read Column Enhanced command responds to subsequent data output. If unselected LUNs are active (SR[6] is zero) when Change Read Column Enhanced is issued, then the host shall issue a Read Status Enhanced (78h) command prior to subsequent data output to ensure all LUNs that are not selected turn off their output buffers.

The ONFI-JEDEC Joint Taskgroup has defined a modified version of Change Read Column Enhanced, often referred to as Random Data Out. In that definition a 00h command is given to specify the row address (block and page) for the data to be read, and then a normal Change Read Column command is issued to specify the column address. This definition is shown in Figure 5-36. Refer to the parameter page to determine if the device supports this version.

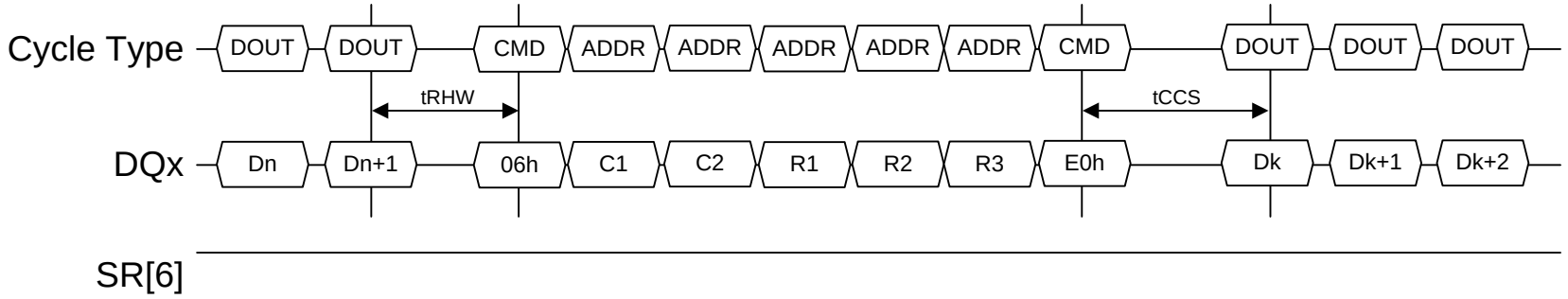


Figure 5-35 Change Read Column Enhanced timing

Dn Data bytes read prior to the row and column address change.

C1-C2 New column address to be set for subsequent data transfers. C1 is the least significant byte.

R1-R3 New row address to be set for subsequent data transfers. R1 is the least significant byte.

Dk Data bytes being read starting with the new addressed row and column.

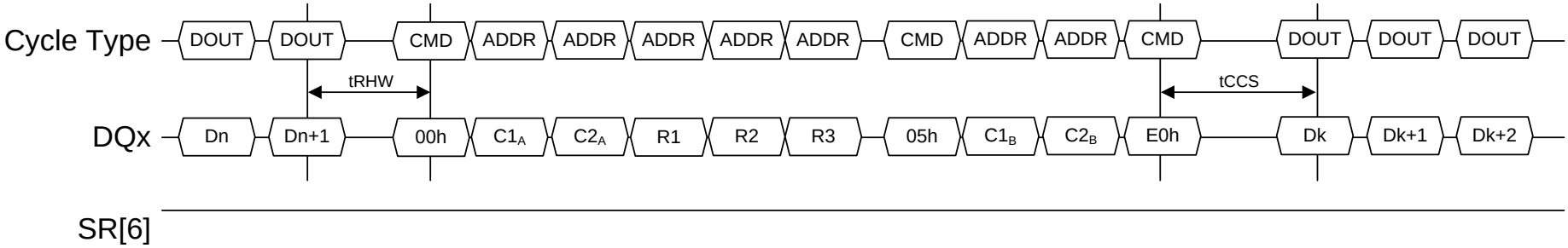


Figure 5-36 Change Read Column Enhanced timing, ONFI-JEDEC Joint Taskgroup primary definition

Dn	Data bytes read prior to the row and column address change.
$C1_A$-$C2_A$	Column address specified as part of 00h sequence; not used. $C1_A$ is the least significant byte.
R1-R3	New row address to be set for subsequent data transfers. R1 is the least significant byte.
$C1_B$-$C2_B$	New column address to be set for subsequent data transfers. $C1_B$ is the least significant byte.
Dk	Data bytes being read starting with the new addressed row and column.

5.22. Change Write Column Definition

The Change Write Column function changes the column address being written to in the page register for the selected LUN. Figure 5-37 defines the Change Write Column behavior and timings.

The host shall not write data to the LUN until tCCS ns after the last column address is written to the LUN. Refer to Figure 5-34.

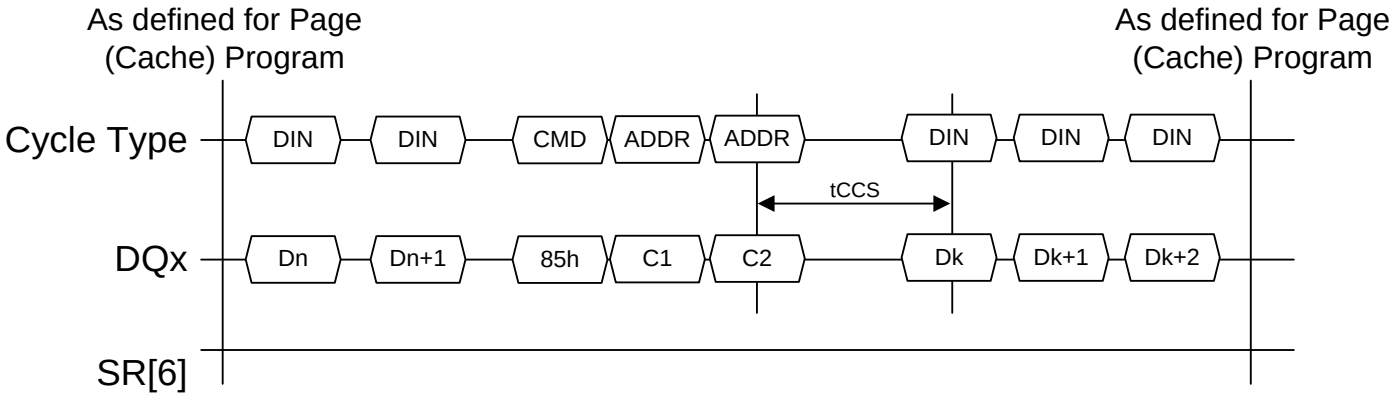


Figure 5-37 Change Write Column timing

C1-C2 New column address to be set for subsequent data transfers. C1 is the least significant byte.

Dn Data bytes being written to previous addressed column

Dk Data bytes being written starting with the new addressed column

5.23. Change Row Address Definition

The Change Row Address function changes the row and column address being written to for the selected LUN. This mechanism may be used to adjust the block address, page address, and column address for a Program that is in execution. The LUN and plane address shall be the same as the Program that is in execution. Figure 5-38 defines the Change Row Address behavior and timings.

The host shall not write data to the LUN until tCCS ns after the last row address is written to the LUN. Refer to Figure 5-38.

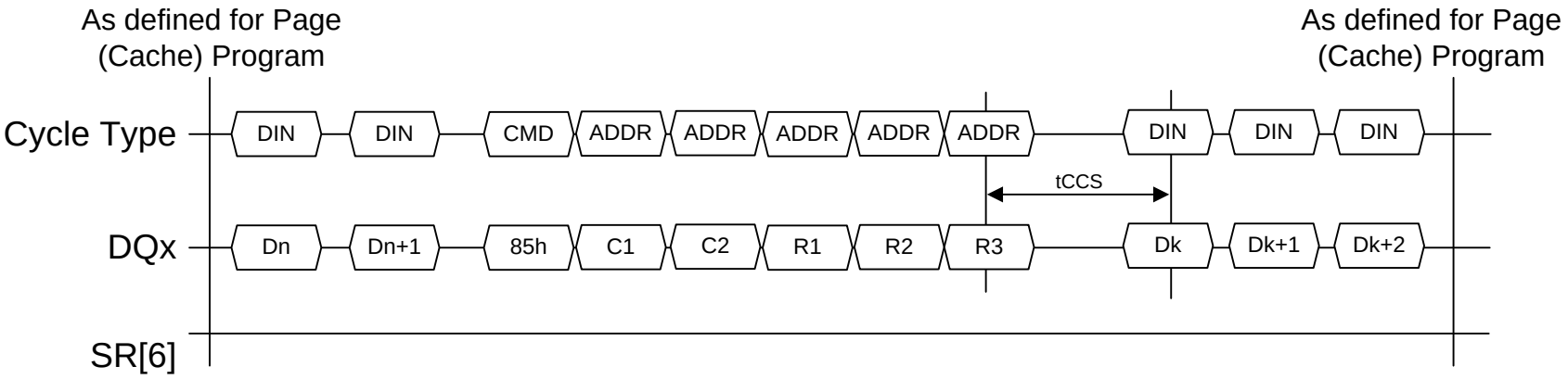


Figure 5-38 Change Row Address timing

C1-C2 New column address to be set for subsequent data transfers. C1 is the least significant byte.

R1-R3 Row address of the page being programmed. The LUN address and plane address shall be the same as the Program in execution. R1 is the least significant byte.

Dn Data bytes being written prior to row address change; will be written to new row address

Dk Data bytes being written to the new block and page, starting with the newly addressed column

5.24. Volume Select Definition

The Volume Select function is used to select a particular Volume based on the address specified. Volume Select is required to be used when CE_n pin reduction is used or when matrix termination is used.

This command is accepted by all NAND Targets that are connected to a particular Host Target (refer to section 2.20). The command may be executed with any LUN on the Volume in any state. The Volume Select command may only be issued as the first command after CE_n is pulled low; CE_n shall have remained high for tCEH in order for the Volume Select command to be properly received by all NAND Targets connected to the Host Target. DQS (DQS_t) shall remain high for the entire Volume Select command sequence.

If Volumes that share a Host Target are configured to use different data interfaces, then the host shall issue the Volume Select command using the SDR data interface.

When the Volume Select command is issued, all NAND Targets that have a Volume address that does not match the address specified shall be deselected to save power (equivalent behavior to CE_n pulled high). If one of the LUNs in an unselected Volume is an assigned terminator for the selected Volume, then that LUN will enter the Sniff state. Refer to Table 4-59 for a description of LUN states for on-die termination.

If the Volume address specified does not correspond to any appointed volume address, then all NAND Targets shall be deselected until a subsequent Volume Select command is issued. If the Volume Select command is not the first command issued after CE_n is pulled low, then the NAND Targets revert to their previously selected, deselected, or sniff states. For Volume reversion behavior, refer to section 3.2.4.

The Volume address is retained across all reset commands, including Reset (FFh). Figure 5-39 defines the Volume Select behavior and timings. Table 5-10 defines the Volume Address field specified as part of the command.

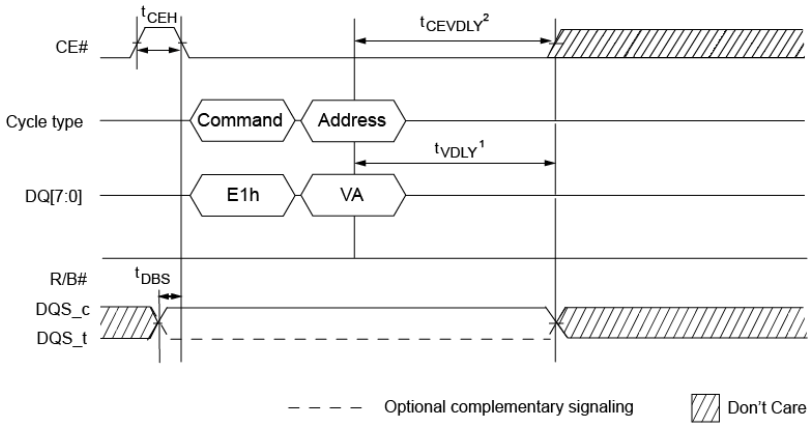


Figure 5-39 Volume Select timing diagram

Notes:

1. The host shall not issue new commands to any LUN on any Volume until after tVDLY. This delay is required to ensure the appropriate Volume is selected for the next command issued. During a data input operation, Volume Select command may be issued prior to the 10h, 11h, or 15h command if the next command to the Volume in data input mode is Change Row Address. In this case, the host shall wait tCCS before issuing the Change Row Address command.
2. The host shall not bring CE_n high on any Volume until after tCEVDLY. This delay is required to ensure the appropriate Volume is selected based on the previously issued Volume Select command.

Volume Address	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VA	Reserved (0)				Volume Address			

Table 5-10 Volume Address

Volume Address Specifies the Volume to select.

5.25. ODT Configure Definition

The ODT Configure command is used to configure on-die termination when using matrix termination. Specifically, ODT Configure specifies whether a particular LUN is a terminator for a Volume(s) and the Rtt settings. If the LUN is specified as a terminator for one or more Volumes, then the LUN shall enable on-die termination when either data input or data output cycles are executed on the Volume(s) it is acting as a terminator for.

If ODT Configure is used to specify the Rtt settings for any LUN, then it shall be used to specify the Rtt settings for LUNs on all Volumes. In this case, ODT Configure shall be issued to at least one LUN on each Volume. When an ODT Configure command is issued to at least one LUN on a Volume, the Volume shall begin using the ODT Configuration Matrix for all LUNs on that Volume. The default value for the ODT Matrix is 0000h, i.e., termination is disabled.

When issuing ODT Configure in the SDR data interface the host shall wait 40ns after Data Input cycle for Rtt2 before issuing next command cycle.

When issuing ODT Configure in the NV-DDR2 NV-DDR3 or NV-LPDDR4 data interface, each data byte is transmitted twice. The device shall only latch one copy of each data byte. This command shall not be issued when using the NV-DDR data interface. See section 4.4.

When this command is issued and the NV-DDR2 or NV-DDR3 data interface is enabled, then the updated termination settings take effect immediately. The host should take care when modifying these settings to avoid any signal integrity issues. If issues occur when the NV-DDR2 interface is enabled, then it is recommended to transition to the SDR data interface, make the appropriate updates to the termination settings, and then transition back to the NV-DDR2 data interface. If issues occur when either the NV-DDR3 or NV-LPDDR4 interface is enabled, then it is recommended to transition to a slower timing mode, make the appropriate updates to the termination settings, and then transition back to the faster NV-DDR3 or NV-LPDDR4 timing mode.

The on-die termination settings are retained across all reset commands, including Reset (FFh). Figure 5-40 defines the ODT Configure behavior and timings.

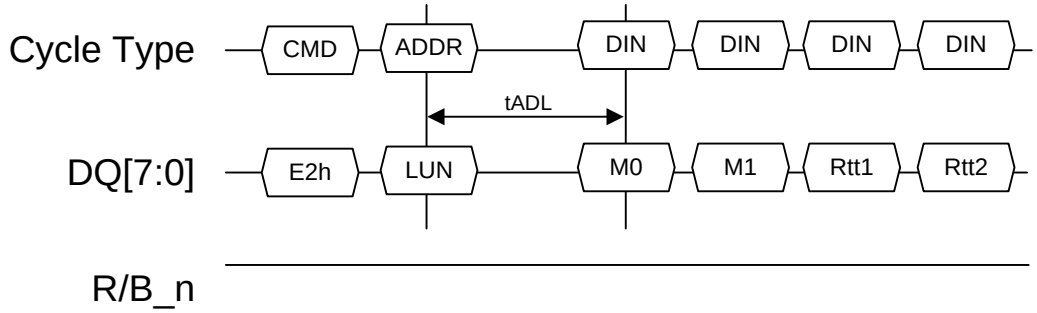


Figure 5-40 ODT Configure timing diagram

LUN	Specifies the LUN that acts as a terminator. This field is formatted in the same manner as the row address byte that contains the LUN address. Refer to section 3.1. Note that the LUN address may require more than one address cycle if the LUN address spans more than one row address byte. See vendor device datasheet for the number of LUN address cycles needed for this command.
M0	Lower byte of the ODT configuration matrix.
M1	Upper byte of the ODT configuration matrix.
Rtt1	Termination settings for DQ[7:0]/DQS.
Rtt2	Termination settings for RE_n
R	Reserved (0h)

Table 5-11 defines the ODT Configuration Matrix specified as part of the command. If a bit is set to one, then the LUN shall act as the terminator for the corresponding Volume (Vn) where n corresponds to the Volume address.

Volume Address	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
M0	V7	V6	V5	V4	V3	V2	V1	V0
M1	V15	V14	V13	V12	V11	V10	V9	V8

Table 5-11 ODT Configuration Matrix

Table 5-12 defines the on-die termination settings specified as part of the command, including the Rtt values for DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c.

Rtt Settings	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Rtt1	DQ[7:0]/DQS Rtt & ODT Enable for Data Output				DQ[7:0]/DQS Rtt & ODT Enable for Data Input			
Rtt2	Reserved				RE_n Rtt & ODT Enable			

Table 5-12 On-die Termination Settings

DQ[7:0]/DQS Rtt & ODT Enable for Data Input

This field controls the on-die termination settings for the DQ[7:0], DQS_t and DQS_c signals for data input operations (i.e. writes to the device).

The values are:

0h = ODT disabled
1h = ODT enabled with Rtt of 150 Ohms
2h = ODT enabled with Rtt of 100 Ohms
3h = ODT enabled with Rtt of 75 Ohms
4h = ODT enabled with Rtt of 50 Ohms
5h = ODT enabled with Rtt of 30 Ohms (Optional)
6h-Fh Reserved

DQ[7:0]/DQS Rtt & ODT Enable for Data Output

This field controls the on-die termination settings for the DQ[7:0], DQS_t and DQS_c signals for data output operations (i.e. reads from the device).

The values are:

0h = ODT disabled
1h = ODT enabled with Rtt of 150 Ohms
2h = ODT enabled with Rtt of 100 Ohms
3h = ODT enabled with Rtt of 75 Ohms
4h = ODT enabled with Rtt of 50 Ohms
5h = ODT enabled with Rtt of 30 Ohms (Optional)
6h-Fh Reserved

RE_n Rtt & ODT Enable

This field controls the on-die termination settings for the RE_t and RE_c signals.

The values are:

0h = ODT disabled
1h = ODT enabled with Rtt of 150 Ohms
2h = ODT enabled with Rtt of 100 Ohms
3h = ODT enabled with Rtt of 75 Ohms

4h = ODT enabled with Rtt of 50 Ohms
5h = ODT enabled with Rtt of 30 Ohms (Optional)
6h-Fh Reserved

5.26. ODT Disable/Enable

ODT termination causes signal swing on the channel to be smaller than that of an unterminated channel. Once the NV-LPDDR4 interface has been enabled, the NAND and controller internal VrefQ will still be at an untrained state and the smaller signal swing with ODT can cause failure of Set Feature or Read Status and Get Feature sequences. NAND devices and host shall support ODT disable and enable using using 1Bh/1Ch commands.

- 1Bh disables target and non-target ODT operations
- 1Ch enables target and non-target ODT operations

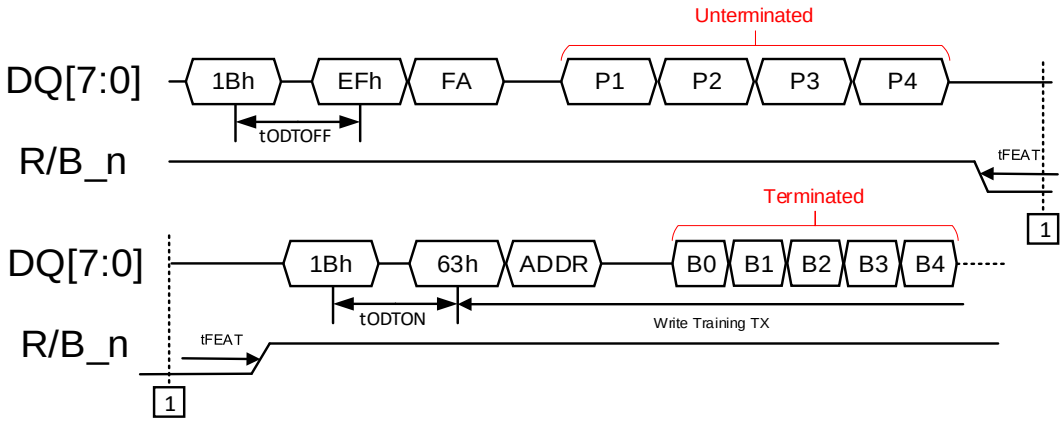


Figure 5-41 ODT Disable/Enable Timing

5.27. ZQ Calibration Long

The ZQ CALIBRATION LONG (ZQCL) command is used to perform the initial calibration during a power-up initialization or reset sequence. Writing F9h to the command register, followed by one row address cycle containing the LUN address performs ZQCL on the selected die. This command may be issued at any time by the controller, depending on the system environment. The ZQCL command triggers the calibration engine inside the NAND. After calibration is achieved, the calibrated values are transferred from the calibration engine to the NAND I/O, which are reflected as updated RON and Rtt values.

During ZQCL operation, no array operations are allowed on the NAND device that is performing the ZQCL operation. Array operations are allowed on any of the other NAND devices that share the ZQ signal with the NAND device that is performing the ZQCL operation.

The NAND is allowed a timing window defined by tZQCL to perform a full calibration and transfer of values. When ZQCL is issued the timing parameter tZQCL must be satisfied.

When ZQCL operation is complete, the host shall check status. If the FAIL bit is set (i.e. SR[0]=1), then the calibration procedure failed and user should check the RZQ resistor connection. If the ZQCL operation fails, the device will revert to a vendor specific value. If RESET

operation is executed during the ZQCL operation, the NAND device will revert to factory settings for output driver strength and ODT values (e.g. as if no ZQ calibration was performed).

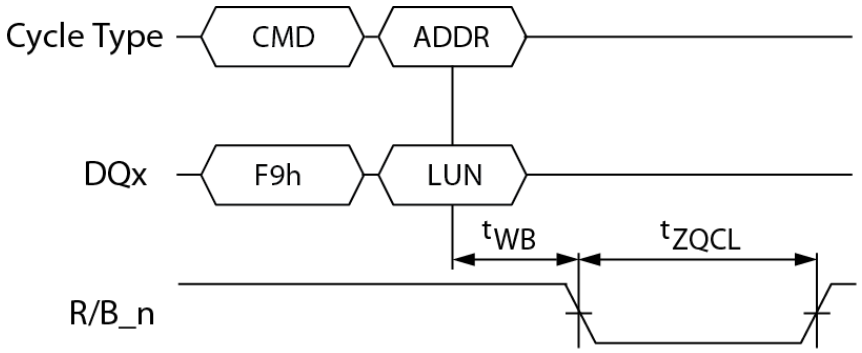


Figure 5-42 ZQ Calibration Long

5.28. ZQ Calibration Short

The ZQ CALIBRATION SHORT (ZQCS) command is used to perform periodic calibrations to account for small voltage and temperature variations. Writing D9h to the command register, followed by one row address cycles containing the LUN address, performs ZQCS on the selected die. A shorter timing window is provided to perform the reduced calibration and transfer of values as defined by timing parameter tZQCS. A ZQCS command can effectively correct a minimum of 1.5% RON and Rtt impedance error within tZQCS, assuming the maximum sensitivities specified in Table 4-41 and Table 4-58.

During ZQCS operation, no array operations are allowed on the NAND device that is performing the ZQCS operation. Array operations are allowed on any of the other NAND devices that share the ZQ signal with the NAND device that is performing the ZQCS operation.

When ZQCS operation is complete, the host shall check status. If the FAIL bit is set (i.e. SR[0]=1), then the calibration procedure failed and user should follow vendor specific instructions. If the ZQCS operation fails, the device will revert to a vendor specific value.

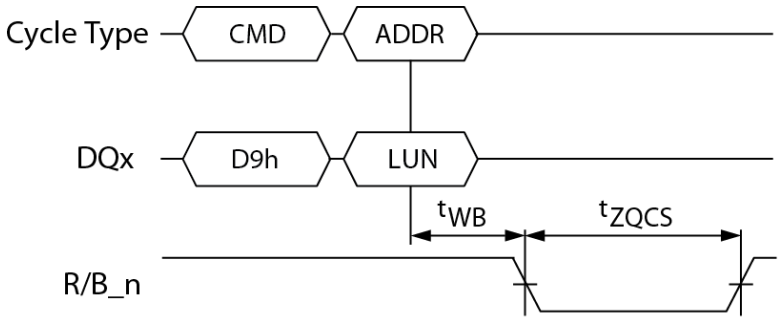


Figure 5-43 ZQ Calibration Short

5.29. Set Features Definition

The Set Features function modifies the settings of a particular feature. For example, this function can be used to enable a feature that is disabled at power-on. Parameters are always transferred on the lower 8-bits of the data bus. Figure 5-44 defines the Set Features behavior and timings.

When issuing Set Features in the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface, each data byte is transmitted twice. The device shall only latch one copy of each data byte. See section 4.4.

Set Features is used to change the timing mode and data interface type. When changing the timing mode, the device is busy for tITC, not tFEAT. During the tITC time the host shall not poll for status.

The LUN Set Features (D5h) command functions the same as the target level Set Features (EFh) command except only the addressed LUNs settings are modified. It shall be assumed that wherever Set Features command is mentioned in this document that LUN Set Features functions the same except where differences are explicitly stated.

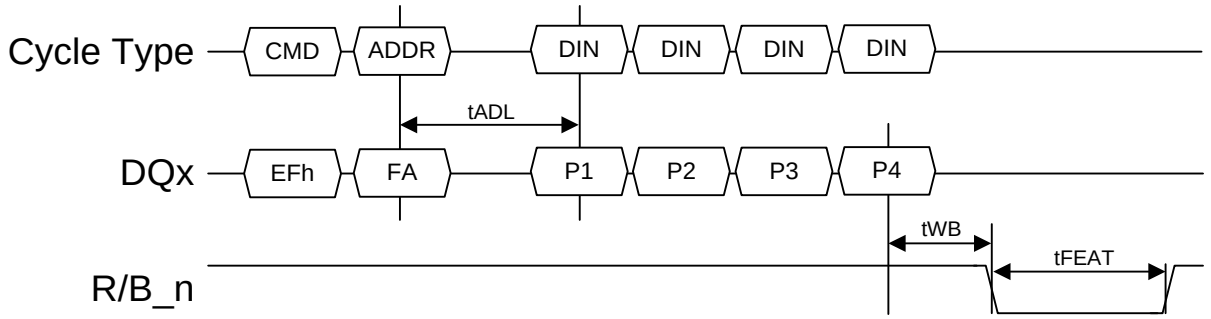


Figure 5-44 Set Features timing

* **NOTE:** Busy time is tITC when setting the timing mode.

FA Feature address identifying feature to modify settings for.

P1-P4 Parameters identifying new settings for the feature specified.

P1	Sub feature parameter 1
P2	Sub feature parameter 2
P3	Sub feature parameter 3
P4	Sub feature parameter 4

Refer to section 5.31 for the definition of features and sub feature parameters.

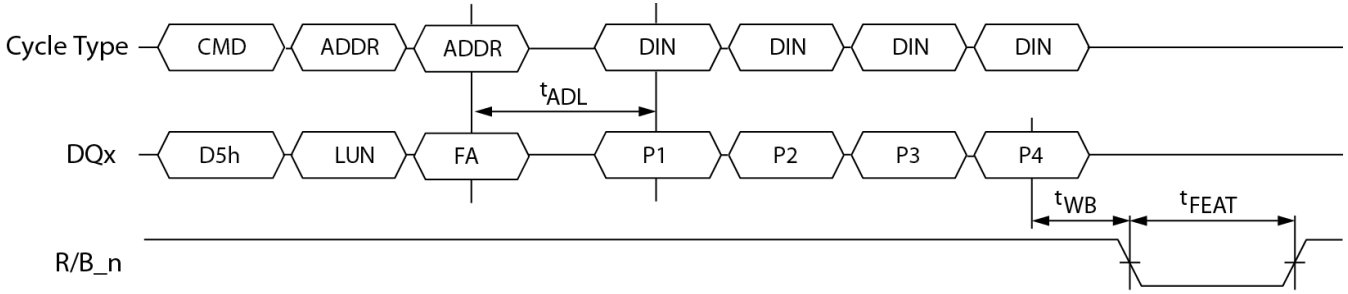


Figure 5-45 LUN Set Features timing

* **NOTE:** Busy time is tITC when setting the timing mode.

LUN LUN Address. LA0 = bit 0, LA1 = bit1, LA2 = bit 2. (i.e. LUN 0 = 00h, LUN 1 = 01h)
FA Feature address identifying feature to modify settings for.

P1-P4 Parameters identifying new settings for the feature specified.

P1 Sub feature parameter 1
P2 Sub feature parameter 2
P3 Sub feature parameter 3
P4 Sub feature parameter 4

Refer to section 5.31 for the definition of features and sub feature parameters

5.30. Get Features Definition

The Get Features function is the mechanism the host uses to determine the current settings for a particular feature. This function shall return the current settings for the feature (including modifications that may have been previously made with the Set Features function). Parameters are always transferred on the lower 8-bits of the data bus. After reading the first byte of data, the host shall complete reading all desired data before issuing another command (including Read Status or Read Status Enhanced). Figure 5-46 defines the Get Features behavior and timings.

When issuing Get Features in the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface, each data byte is received twice. The host shall only latch one copy of each data byte. See section 4.4.

If Read Status is used to monitor when the tFEAT time is complete, the host shall issue a command value of 00h to begin transfer of the feature data starting with parameter P1.

The LUN Get Features (D4h) command functions the same as the target level Get Features (EEh) command except only the addressed LUNs settings are returned. It shall be assumed that wherever Get Features command is mentioned in this document that LUN Get Features functions the same except where differences are explicitly stated.

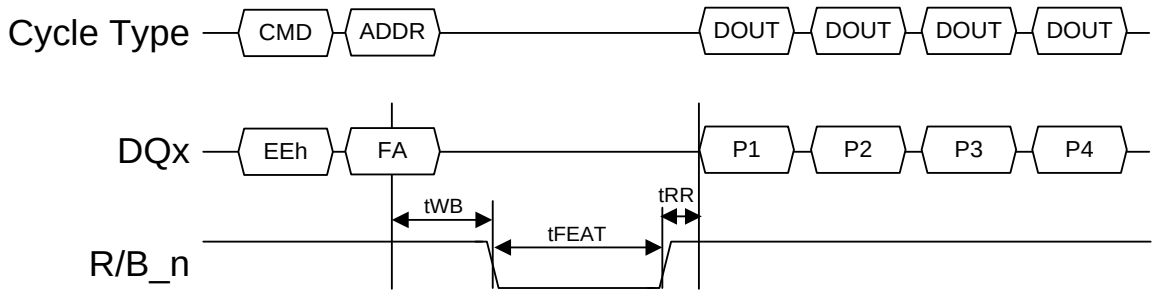


Figure 5-46 Get Features timing

FA Feature address identifying feature to return parameters for.

P1-P4 Current settings/parameters for the feature identified by argument P1

P1	Sub feature parameter 1 setting
P2	Sub feature parameter 2 setting
P3	Sub feature parameter 3 setting
P4	Sub feature parameter 4 setting

Refer to section 5.31 for the definition of features and sub feature parameters.

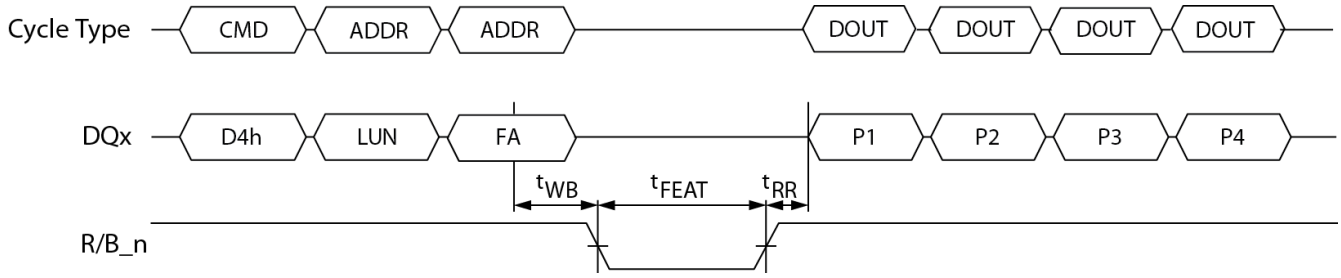


Figure 5-47 LUN Get Features timing

LUN LUN Address. LA0 = bit 0, LA1 = bit1, LA2 = bit 2. (i.e. LUN 0 = 00h, LUN 1 = 01h, etc.)

FA Feature address identifying feature to return parameters for.

P1-P4 Current settings/parameters for the feature identified by argument P1

- P1 Sub feature parameter 1 setting
- P2 Sub feature parameter 2 setting
- P3 Sub feature parameter 3 setting
- P4 Sub feature parameter 4 setting

Refer to section 5.31 for the definition of features and sub feature parameters

5.31. Feature Parameter Definitions

If the Set Features and Get Features commands are not supported by the target, then no feature parameters are supported. Additionally, the target only supports feature parameters defined in ONFI specification revisions that the target complies with.

Feature settings are volatile across power cycles. For each feature setting, whether the value across resets is retained is explicitly stated.

Feature Address	Description
00h	Reserved
01h	Timing Mode
02h	NV-DDR2/NV-DDR3/NV-LPDDR4 Configuration
03h-0Fh	Reserved
10h	I/O Drive Strength
11h-1Fh	Reserved
20h	DCC, Read, Write Tx Training
21h	Write Training RX
22h	Channel ODT configuration for NV-LPDDR4
23h	Internal VrefQ value
24h	Write Duty Cycle Adjustment (WDCA)
25h-2Fh	Reserved
30h	External Vpp Configuration
31h-3Fh	Reserved
40h	Per-Pin Vrefq Training
41h	Per-Pin Vrefq Training
42h	Per-Pin Vrefq Training
43h-4Fh	Reserved
50h	Reserved
51h-57h	Reserved
58h	Volume Configuration
59h-5Fh	Reserved
60h	Reserved
61h	Reserved
62h-7Fh	Vendor specific
80h-FFh	Vendor specific

Table 5-13 Feature Parameter Addresses

5.31.1. Timing Mode – FA 01h

This setting shall be supported if the target complies with ONFI specification revision 1.0.

When the SDR, NV-DDR, or NV-DDR2 data interface is enabled, the Data Interface setting and Timing Mode Number are not retained across Reset (FFh); after a Reset (FFh) the Data Interface shall be SDR and Timing Mode Number 0. All other settings for the timing mode are retained across Reset (FFh), Synchronous Reset (FCh), and Reset LUN (FAh) commands. If the Reset (FFh) command is issued when the Data Interface is configured as NV-DDR or NV-DDR2, then the host shall use the SDR data interface with Timing Mode 0 until a new data interface and/or timing mode is selected with Set Features. Hosts shall only set a timing mode that is explicitly shown as supported in the Read Parameter Page.

The results of the host using Set Features to transition from either the NV-DDR or NV-DDR2 data interface to the SDR data interface is indeterminate. To transition to the SDR data interface, the host should use the Reset (FFh) command.

When VccQ=1.2V the interface can operate in NV-DDR3 or NV-LPDDR4 mode. The host must initialize the interface as described in section 4.5.4. Switching from the NV-DDR3 or NV-LPDDR4 interface to the SDR, NV-DDR or NV-DDR2 interfaces is not allowed. If sub feature parameter P1 Data Interface bits [4:5] are changed the device will remain in NV-DDR3 or NV-LPDDR4 interface. Devices may indicate to the host that the NV-DDR3 data interface is enabled by having a default power-on value of “11b” on Data Interface bits [4:5]. If the Reset (FFh) command is

issued when the Data Interface is NV-DDR3, the host shall continue to use the NV-DDR3 data interface. If the Reset (FFh) command is issued when the Data Interface is NV-LPDDR4, the host shall continue to use the NV-LPDDR4 data interface. It is recommended after the host issues Reset (FFh) that Timing Mode 0 be used until the host reconfigures the device to support faster Timing Modes.

Sub Feature Parameter	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P1	TMN[4]	PC(1)	Data Interface		Timing Mode Number TMN[3:0]			
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							
Note: 1. Vendor Specific								

Table 5-14 Feature Address 01h

Timing Mode Number (TMN)
Set to the hexadecimal value (e.g. 0Ah=TM10) of the maximum timing mode in use by the host. Default power-on value is 00h

Data Interface
00b = SDR (optional default power-on value, see vendor datasheet)
01b = NV-DDR
10b = NV-DDR2
11b = Optional NV-DDR3 operation power-on default value, see vendor datasheet. These bits do not enable NV-DDR3 mode operation but may serve to indicate that the NV-DDR3 interface is enabled.

PC
The Program Clear bit controls the program page register clear enhancement which defines the behavior of clearing the page register when a Program (80h) command is received. If cleared to zero, then the page register(s) for each LUN that is part of the target is cleared when the Program (80h) command is received. If set to one, then only the page register for the LUN and interleave address selected with the Program (80h) command is cleared and the tADL time for Program commands is as reported in the parameter page. This bit is vendor specific. Please see vendor datasheet for support of the program clear feature

Reserved / R
Reserved values shall be cleared to zero by the host. Targets shall not be sensitive to the value of reserved fields.

5.31.2. NV-DDR2, NV-DDR3, NV-LPDDR4 Configuration – FA 02h

This setting shall be supported if the target supports the NV-DDR2 NV-DDR3 or NV-LPDDR4 data interface. This setting controls differential signaling, basic on-die termination configuration, and warmup cycles for data input and output. For the NV-DDR2 interface, these settings are not retained across Reset (FFh) and the power-on values are reverted to. For the NV-DDR3 and NV-LPDDR4 data interface, these settings are retained across Reset (FFh). For the NV-DDR2, NV-

DDR3 and NV-LPDDR4 interfaces, these settings are retained across Synchronous Reset (FCh) and Reset LUN (FAh) commands. The power-on default is 0h for all fields.

The NV-DDR2 data interface shall be enabled in the Timing Mode feature for these settings to take effect. It is recommended that this feature be configured prior to enabling the NV-DDR2 data interface.

When this feature is changed and the NV-DDR2 NV-DDR3 or NV-LPDDR4 data interface is enabled, then the updated settings may take effect immediately. The host should take care when modifying these settings while NV-DDR2 NV-DDR3 or NV-LPDDR4 is enabled to avoid any signal integrity issues. If issues occur while NV-DDR2 is enabled, then it is recommended to transition to the SDR data interface, make the appropriate updates to this feature, and then transition back to the NV-DDR2 data interface. If issues occur while the NV-DDR3 or NV-LPDDR4 interface is enabled, then it is recommended to transition to Timing Mode 0, make the appropriate updates to this feature, and then transition back to the desired Timing Mode. If these settings are modified the host should take care to ensure appropriate settings are applied in a manner that avoids signal integrity issues.

Sub Feature Parameter	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P1	DQ/DQS/RE_n ODT Enable				R	CMPR	CMPD	VEN
P2	Warmup DQS cycles for Data Input				Warmup RE_n and DQS cycles for Data Output			
P3	(R)	VOH.LTT	DBI.WR	DBI.RD	Internal VREFQ Range		Interface	
P4	Reserved (R)							

Table 5-15 Feature Address 02h

VEN — If set to one, then external VREFQ is used as a reference for the input and I/O signals. If cleared to zero, then internal VREFQ is used as an input reference. CE_n and WP_n are CMOS signals. Implementations may use CMOS or SSTL_18 (NV-DDR2), or NV-DDR3 input levels for WE_n, ALE, and CLE. Note: RE_t, DQS_t only use VREFQ when CMPD, CMPR are cleared to zero.

CMPD — If set to one, then the complementary DQS (DQS_c) signal is enabled. If cleared to zero, then the complementary DQS (DQS_c) signal is not used.

CMPR — If set to one, then the complementary RE_n (RE_c) signal is enabled. If cleared to zero, then the complementary RE_n (RE_c) signal is not used.

DQ/DQS/RE_n ODT Enable

This field controls the on-die termination settings for the DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c signals. The values are:

0h = ODT disabled
1h = ODT enabled with Rtt of 150 Ohms
2h = ODT enabled with Rtt of 100 Ohms (Optional)
3h = ODT enabled with Rtt of 75 Ohms
4h = ODT enabled with Rtt of 50 Ohms
5h = ODT enabled with Rtt of 30 Ohms (Optional)

Note: Rtt settings may be specified separately for DQ[7:0]/DQS and the RE_n signals. The DQ[7:0]/DQS may be specified separately for data input versus data output operation. Refer to the definition of the ODT Configure command in section 5.25. If values are specified with the ODT Configure command, then this field is not used. Get Features returns the previous value set in this field, regardless of the Rtt settings specified using ODT Configure.

Warmup RE_n and DQS cycles for Data Output

This field indicates the number of warmup cycles of RE_n and DQS that are provided for data output. These are the number of initial “dummy” RE_t/RE_c cycles at the start of data output operations. There are corresponding “dummy” DQS_t/DQS_c cycles to the “dummy” RE_t/RE_c cycles that the host shall ignore. The values are:

0h = 0 cycles, feature disabled
1h = 1 warmup cycle
2h = 2 warmup cycles
3h = 4 warmup cycles
4h-FFh = Reserved

Warmup DQS cycles for Data Input

This field indicates the number of warmup cycles of DQS that are provided for data input. These are the number of initial “dummy” DQS_t/DQS_c cycles at the start of data input operations. The values are:

0h = 0 cycles, feature disabled
1h = 1 warmup cycle
2h = 2 warmup cycles
3h = 4 warmup cycles
4h-FFh = Reserved

Interface

This field controls whether the interface used when VccQ=1.2V

0h = NV-DDR3
1h = NV-LPDDR4
2h = Reserved
3h = Reserved

Internal VrefQ Range (Read Only)

This field indicates the range and step size of the internal VrefQ settings

0h = Range/Step Size Type 1/Value 1
1h = Range/Step Size Type 2/Value 2
2h = Range/Step Size Type 3/Value 3
3h = Reserved

DBI.RD

This field controlls the DBI usage for Read data transfers. If set to 1 then DBI is enabled, if cleared to 0 then DBI is disabled for Read data transfers.

DBI.WR

This field controlls the DBI usage for Write data transfers. If set to 1 then DBI is enabled, if cleared to 0 then DBI is disabled for Write data transfers.

VOH.LTT (optional, NV-LPDDR4 only)
This field controlls the VOH nominal voltage for NV-LPDDR4. If set to 1 then VOH.LTT nominal is VccQ/2.5, if cleared to 0 then VOH.LTT nominal is VccQ/3.

Reserved (R) Reserved values shall be cleared to zero by the host. Targets shall not be sensitive to the value of reserved fields.

5.31.3. I/O Drive Strength – FA 10h

This setting shall be supported if the target supports the NV-DDR, NV-DDR2, NV-DDR3, or NV-LPDDR4 data interface. The I/O drive strength setting shall be retained across Reset (FFh), Synchronous Reset (FCh), and Reset LUN (FAh) commands. For NV-DDR, NV-DDR2, NV-DDR3, and NV-LPDDR4 the power-on default drive strength value is either 35 Ohm (010b) or 37.5 Ohm (010b or 100b) setting as specified in the parameter page or vendor datasheet. For devices which support both 35 Ohms and 37.5 Ohms I/O drive strength, the 010b setting shall be 35 Ohms only, the 100b setting shall be 37.5 Ohms and the power-on default will be the 35 Ohm setting (010b).
For the NV-LPDDR4 interface, FA10h P1[3:0] control only the output drive strength of the pull-down device while the output drive strength of the pull-up device is controlled by FA22h P1[3:0] Channel ODT settings.

Sub Feature Parameter	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P1	Reserved (0)				Drive Strength			
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Table 5-16 Feature Address 10h

Drive strength
0000b: 18 Ohm (Optional, not supported for NV-DDR3)
0001b: 25 Ohm (Optional)
0010b: 35 Ohm or 37.5 Ohm (as specified in the parameter page or vendor datasheet)
0011b: 50 Ohm
0100b: 37.5 Ohm (power-on default if no 35 Ohm support)

Reserved Reserved values shall be cleared to zero by the host. Targets shall not be sensitive to the value of reserved fields.

5.31.4. DCC, Read, Write Tx, Vrefq, WDCA Training – FA 20h/21h/23h/40h/41h/42h/24h

Training features shown in this section shall be supported by NAND devices operating over 800MT/s in heavily loaded systems.

DCC Training is the feature for the NAND to compensate duty cycle mismatch of RE_t/c signal. Read/Write DQ Training is the feature for the host to align DQS and DQ signals caused by un-matched DQS path.

Figure 5-48 Training flow after power-onshows when each training shall be done after power-on. I/F Initialization shall be done before training at slower interface speeds such as High Speed Interface setting, Driver Strength setting and ZQ calibration. The host shall operate DCC training before Read/Write DQ training. If the host uses the NAND device over 800MT/s, the host shall complete all the trainings defined in this section when training is required.
For the NV-DDR3 and NV-LPDDR4 interface configuration and training flows after power-on, refer to section 4.5.4 NV-DDR3/NV-LPDDR4 Initialization.

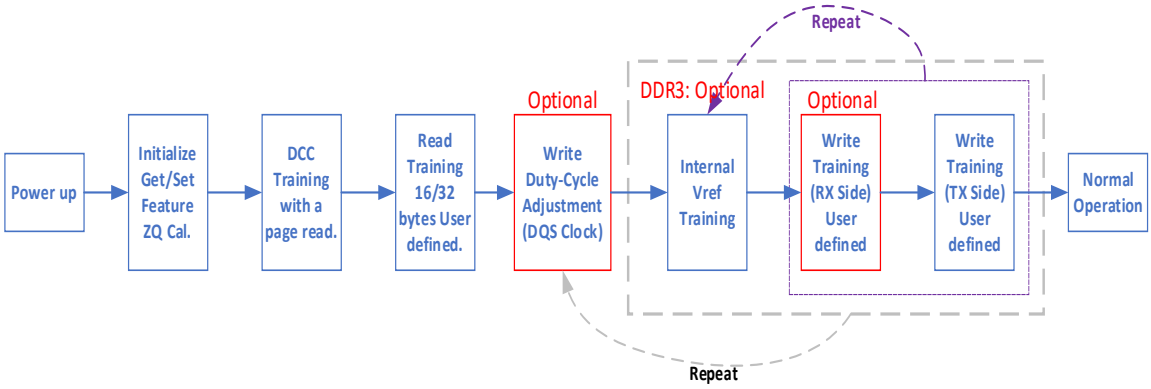


Figure 5-48 Training flow after power-on

The following Sub Feature parameters are to be used for DCC training and Write Training (Tx side)

Sub Feature Parameter	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P1	Reserved (0)					DCC Factory setting	DCCI _EN	DCCE_ EN
P2	Reserved (0)							
P3	Reserved (0)			Read training defined pattern length		Write Training Tx Data Size		
P4	Reserved (0)							

Table 5-17 Feature Address 20h

DCCE_EN

This field controls explicit DCC training setting. If set to 1 then DCC training is enabled, if cleared to 0 then DCC training is disabled.

DCCI_EN

This field controls implicit DCC training during warm up cycles setting. If set to 1 then DCC training is enabled, if cleared to 0 then DCC training is disabled. A host can disable DCCI_EN if the host doesn't need DCC with low frequency operation.

DCC Factory setting

This is an optional function for the NAND device, please refer to the vendor datasheet if DCC factory setting is supported or not. If set to a 1, then the factory DCC settings would be used by the LUN. If cleared to 0, then the DCC calibrated settings would be used by the LUN.

Write Training Tx Data Size (Read Only)

This field indicates the data size for write training (Tx side) (up to 128bytes). NAND devices may support a Write Training (Tx side) data size less than or greater than the value specified on these bits. See vendor data sheet for details on the vendor implementation of these bits.

0000b: 08 Bytes
0001b: 16 Bytes
0010b: 24 Bytes
0011b: 32 Bytes
0100b: 40 Bytes
0101b: 48 Bytes
0110b: 56 Bytes
0111b: 64 Bytes
1000b: 72 Bytes
1001b: 80 Bytes
1010b: 88 Bytes
1011b: 96 Bytes
1100b: 104 Bytes
1101b: 112 Bytes
1110b: 120 Bytes
1111b: 128 Bytes

Read Training Defined pattern length (Read Only)

This field indicates the data pattern length for read training
1b: 32 Bytes
0b: 16 Bytes

Reserved

Reserved values shall be cleared to zero by the host. Targets shall not be sensitive to the value of reserved fields.

The following Sub Feature parameters are to be used for Write Training (Rx side)

Sub Feature Parameter	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P1	Reserved (0)					Internal VrefQ Training	All LUN	Factory setting
P2	St_dq3[1:0]		St_dq2[1:0]		St_dq1[1:0]		St_dq0[1:0]	
P3	St_dq7[1:0]		St_dq6[1:0]		St_dq5[1:0]		St_dq4[1:0]	
P4	Reserved (0)							

Table 5-18 Feature Address 21h

Factory setting

This field controls the input path settings as determined by training/reset or factory settings.

	1b: factory setting 0b: trained value
All LUN	This is an optional function for the NAND device, please refer to the vendor datasheet if All LUN Write Training (Rx side) is supported or not. If this bit is set to 1 prior to write training RX, then the LUN address cycle is ignored, and the write training is performed on all LUNs.
Internal VrefQ Training	This is an optional function for the NAND device, please refer to the vendor datasheet if internal Vrefq Training during Write Training (Rx side) is supported or not. Setting this bit to 1 enables Write Training (Rx side) with internal VrefQ Training. Clearing the bit to 0 enables normal Write Training (Rx side).
St_dq (Read Only)	These fields indicate the status of the Rx side Write Training (DQ[3:0] in sub parameter P2, DQ[7:4] in sub parameter P3). 00b: Centering of dqs to dq0 data eye is successful. 01b: Centering of dqs/dqsn to dq0 data eye failed with dq0 being too slow with respect to dqs/dqsn 10b: Centering of dqs/dqsn to dq0 data eye failed with dq0 being too fast with respect to dqs/dqsn 11b: Centering of dqs/dqsn to dq0 data eye failed for unknown reasons
Reserved	Reserved values shall be cleared to zero by the host. Targets shall not be sensitive to the value of reserved fields.

5.31.4.1. DCC Training

DCC Training shall be performed after the ZQ calibration is completed. This section defines two types of DCC. One is explicit DCC and the other is implicit DCC.

Explicit DCC is initiated by the host to issue specific command sequence defined in section 5.31.4.1.1 or 5.31.4.1.2. Either or both of Explicit DCC shall be supported by the NAND devices operating over 800MT/s.

Implicit DCC is optional feature for the NAND devices and is initiated by the host to set DCCI_EN enable which is assigned in B0[1] of Feature Address 20h. If DCCI_EN is enabled, the NAND device carries out DCC training to update the training result during warm up cycles where “warm up cycles” is sometimes referred to “DQS latency”. Implicit DCC may require specific number of warm up cycles to be set and it shall be given by vendor datasheet. Since DCC Training is performed before Read Training, it is recommended that the DQS falling edge or the successive DQS rising edge is used to capture the read status data.

5.31.4.1.1. DCC (RE_t/c) Training using Set Feature

DCC training using Set Feature is initiated by the host to set DCCE_EN enable which is assigned in B0[0] of Feature Address 20h. When this is enabled, DCCI_EN which is assigned in B0[1] is “don’t care”. On power-up, DCCE_EN shall be disabled. The host shall enable it to perform DCC Training. Refer to Feature Address description for more information.

After Set Feature, the host shall issue the Random Data Out command with the address information based on the Set Feature command used to enable the DCC training feature and calibrate RE_t and RE_c by sending those signals for a page size. (Page size shall be given by vendor datasheet.). If the Set Feature command used was an EFh command, then the addresses for the Random Data Out command sequence shall be filled with 00h. If the Set Feature command used was the D5h (Set Feature for Each LUN) command, then the addresses for the Random Data Out command sequence must have the same LUN address that was used during the D5h command. If LUN address is not used in the Random Data Out sequence, then fix all column address to “00h”. The host shall then calibrate RE_t and RE_c by sending those signals for a page size. During the data output cycles produced by these RE_t and RE_c toggles, the DQ and DQS of the LUNs under training may be driven or Hi-Z depending on the NAND vendor DCC Training implementation. Refer to the NAND vendor datasheet to see if DQ and DQS are driven or Hi-Z during this time. The data for these data output cycles shall be invalid and ignored by the host. Care should be taken to avoid bus contention during these data output cycles, especially for multi-LUN DCC training cases where the NAND vendor DCC Training implementation drives the DQ and DQS signals.

After sending RE_t and RE_c for page size length, Status Check shall be performed to confirm whether DCC is Pass or Fail via SR[0]. If fail, the host shall issue Random Data Out command and resend RE_t and RE_c signals to calibrate again. If EFh is used, all the LUNs under the Target perform DCC (All LUN DCC). If D5h command is used, selected LUN under the Target performs DCC (Single LUN DCC). The device may support either or both of All LUN DCC and Single LUN DCC. See vendor’s datasheet. After completing Explicit DCC using Set Feature, DCCE_EN shall be set to 0.

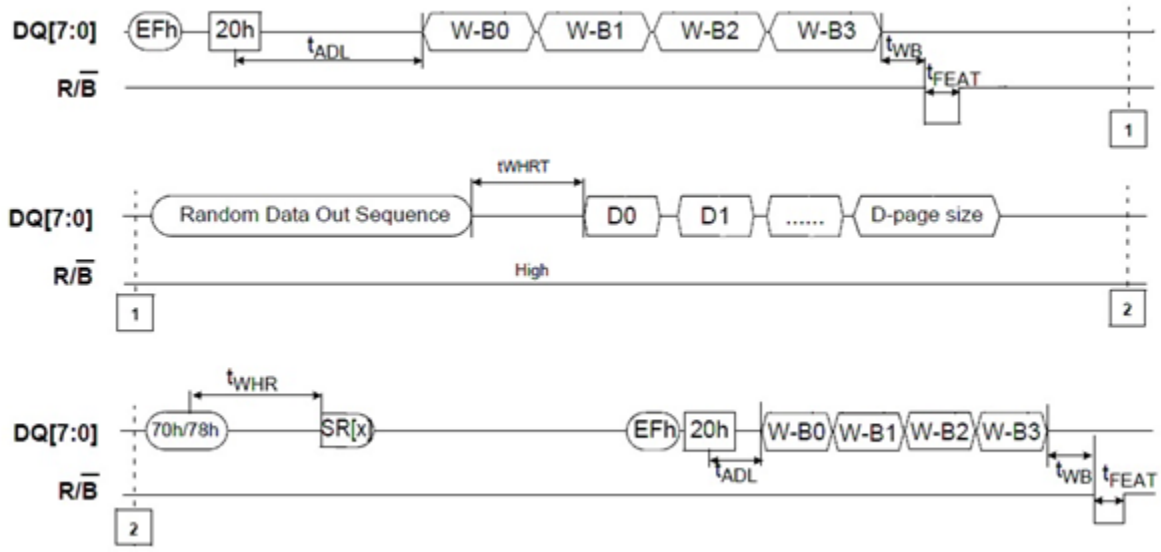


Figure 5-49 DCC (RE_t/c) Training using Set Feature

5.31.4.1.2. DCC (RE_t/c) Training using Command (Optional)

DCC training using a command can be initiated using CMD18h followed by LUN Address. After issuing LUN address, the host shall calibrate RE_t and RE_c by toggling these signals for a page size. (Page size shall be given by vendor datasheet). The data returned by the device is vendor specific data pattern so that there is no impact of data pattern on DCC training. After sending the required number of RE_t and RE_c signals, Status Check shall be performed to confirm whether DCC is Pass or Fail. If status is a Fail, user has to issue RESET command (FFh) wait for the RESET command to execute and then re-issue the Command based DCC sequence.

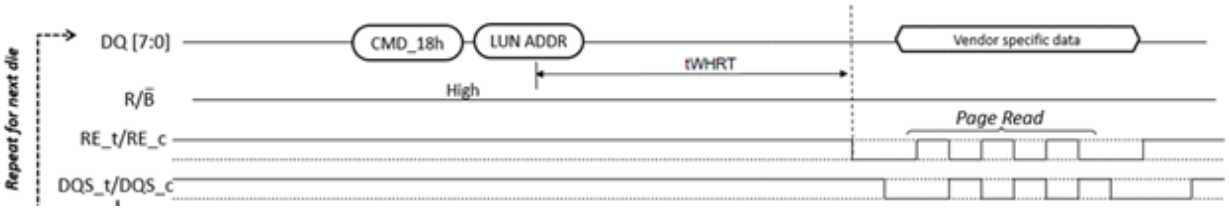


Figure 5-50 DCC (RE_t/c) Training using Command (Optional)

Timing specs of RE_t/RE_c during DCC page read will follow normal Read timing as per vendor datasheet.

5.31.4.2. Read DQ Training

Read DQ Training is the function that outputs a 16 bit user-defined pattern on each of the DQ pins. It means a total of 16 bytes is output by the NAND device (note some vendors may provide a 32 byte pattern).

Read DQ Training is initiated by issuing a [Read DQ Training] command 62h followed by LUN Address then three address cycles. Three address cycles are 1st address (8bit invert mask), 2nd address (first eight bit pattern) and 3rd address (second eight bit pattern). The following table shows example data pattern (i.e. 1st 35h, 2nd 5Ah, 3rd 82h address).

Pin	Inverse Setting		0~15																16~31 (Optional)														
	(Mask)		1st Input DATA : 5Ah								2nd Input DATA : 82h								Swap 1st,2nd data of DQ4~7 ↔ DQ0~3 (Optional)															
DQ0	1 (Inverse)	35h	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ1	0		0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ2	1 (Inverse)		1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1
DQ3	0		0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1
DQ4	1 (Inverse)		1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ5	1 (Inverse)		1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1
DQ6	0		0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ7	0		0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1

Figure 5-51 Example of user defined pattern for Read training

If ’1’ is indicated by a bit in 1st address, DQx corresponding to a bit shall be inverted and the NAND device outputs data pattern designated by 2nd and 3rd addresses masked I/O following in invert mask indicated by 1st address by RE, /RE toggling, the data will inversed by masked I/O.

If host issue RE, /RE toggling for more than the vendor defined pattern length, data will be wrapped.

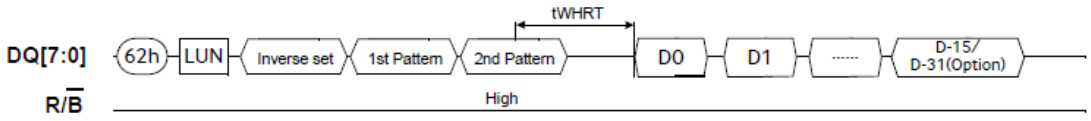


Figure 5-52 Read DQ Training

5.31.4.3. Write DQ Training (Tx Side)

To perform Write training at Tx side, the controller shall issue 63h command followed LUN address. After issuing LUN address, the host shall input data pattern and confirm whether the input is successfully done by checking the output by NAND in following sequence.

Data sizes for Write DQ is pre-defined by NAND. The host shall recognize the data sizes by Get Feature (Feature Address = 20h, B2) and shall input and output the data based on the size.

After writing data to the NAND with 63h command, the data can be read back with 64h command followed by LUN address and the results shall be compared with “expected” data to see if further training (DQ delay) is needed.
If fewer data than pre-defined data bytes are written, then unwritten registers will have un-defined data when read back. If over pre-defined data bytes read were executed, the data are also un-defined and invalid.

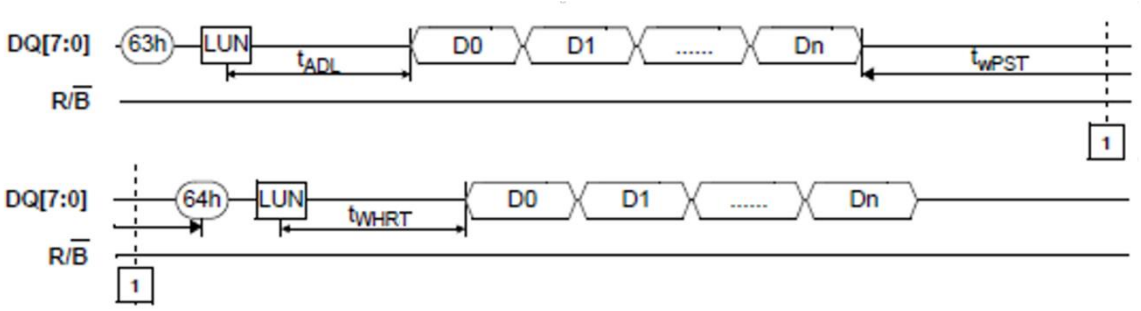
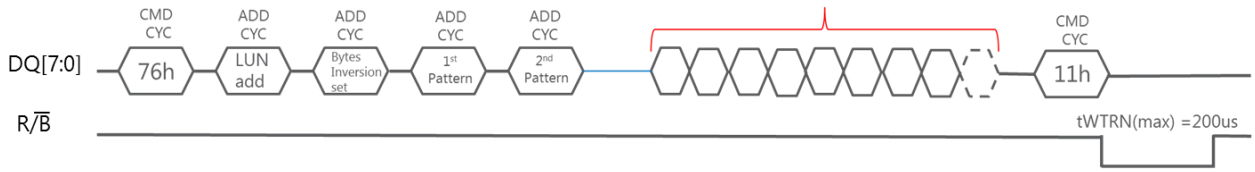


Figure 5-53 Write DQ Training (Tx side)

5.31.4.4. Write DQ Training (Rx Side, Optional)

To perform Write training at Rx side, the controller shall issue 76h command followed by LUN address. After issuing LUN address, the host shall issue 3 address cycles for data pattern format. The definition of these 3 address cycles are the same as the ones mentioned in read training. After the 3 address cycles, the host shall issue data input with the same pattern determined by the 3 address cycles for 1 full page. The input data shall be wrapped around the data pattern length (16 or 32) until a full page data is issued. The training sequence shall be ended by 11h command and the NAND will perform write training during the R/B_ time (tWTRN). The host may poll the R/B_ status by status command to check the completion of the training operation. The status of the training for each DQ can be checked by issuing Get Feature by LUN with address 21h (B1 and B2). The complete byte definition is given in the Feature Address 21h table below.

DIN Burst



DIN Burst: Data Input with the same pattern specified in 3 address cycle wrapping around the data pattern length (16 or 32) for 1 full page

Figure 5-54 Write DQ Training (Rx side) Optional

If Write Training (Rx side) passes, then the host may skip Write Training (Tx side).

The following flow chart is an example of the process for doing Write Training on the Rx side.

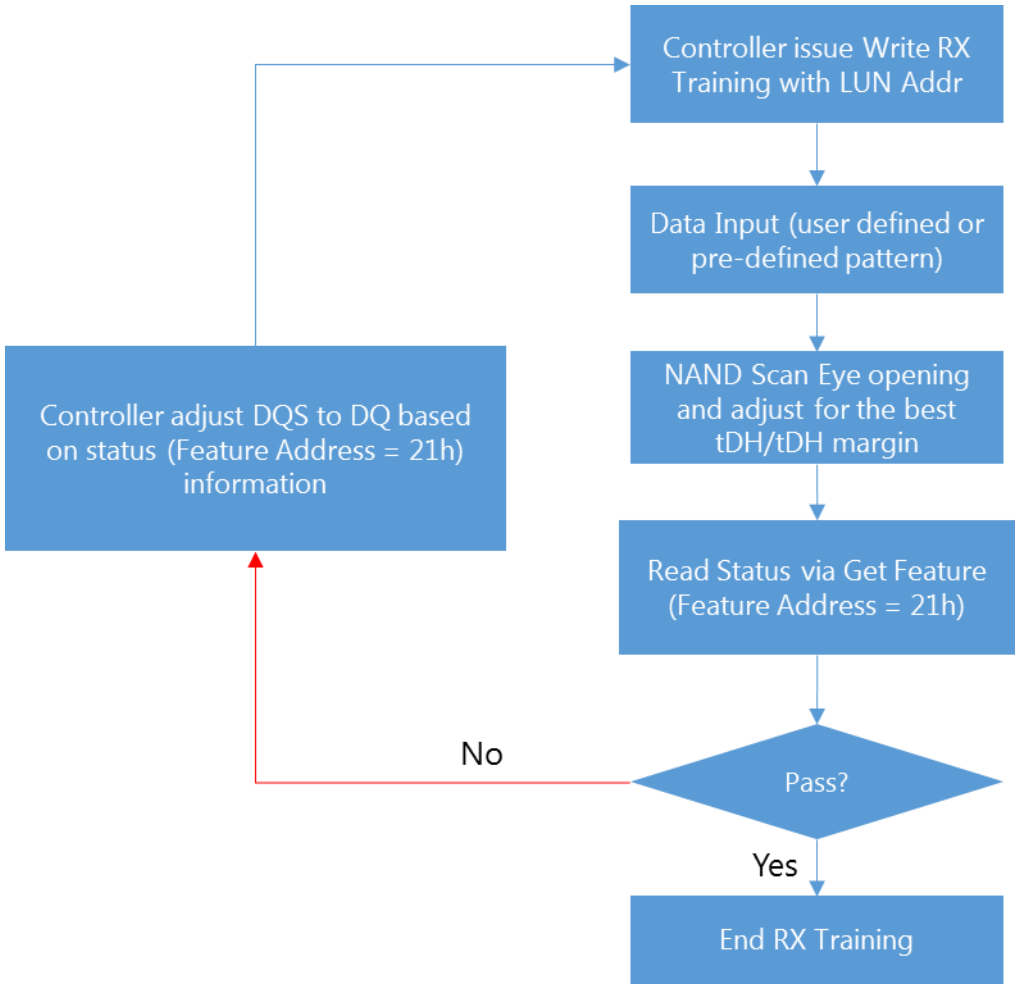


Figure 5-55 Flow chart for Write DQ Training (Rx side)

5.31.4.5. Write Duty Cycle Adjustment (WDCA, Optional)

Write Duty Cycle Adjustment (WDCA) is an optional feature that provides a way to compensate for input DQS duty cycle loss at the NAND device. The WDCA feature is controlled via FA24h.

The diagram below shows the NAND interface training flow with WDCA. The controller repeats between configuring WDCA settings and performing Write Training sequence to find the optimum WDCA setting. The tFEAT time for Feature address 24h is vendor specific.

The following Sub Feature (24h) parameters are to be used for WDCA

Sub Feature Parameter	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P1				WDCA Step Control				
P2	Reserved							
P3	Reserved							
P4	Reserved							

Table 5-19 Feature Address 24h, WDCA

P1[4:0] for WDCA Step Control

00000b: 0step (default)
00001b: +1step
00010b: +2steps
00011b: +3steps
00100b ~ 01111b: +4steps ~ +15steps (Optional)
10000b: 0step
10001b: -1step
10001b: -2steps
10011b: -3steps
10100b ~ 11111b: -4steps ~ -15steps (Optional)

5.31.4.6. Write Training Monitor (Optional)

With voltage and temperature changes on the system, there is a need for a method to monitor whether the last obtained optimum training settings are still sufficient to produce low error rates on the interface. A method to monitor sufficiency of the last obtained optimum settings is described below

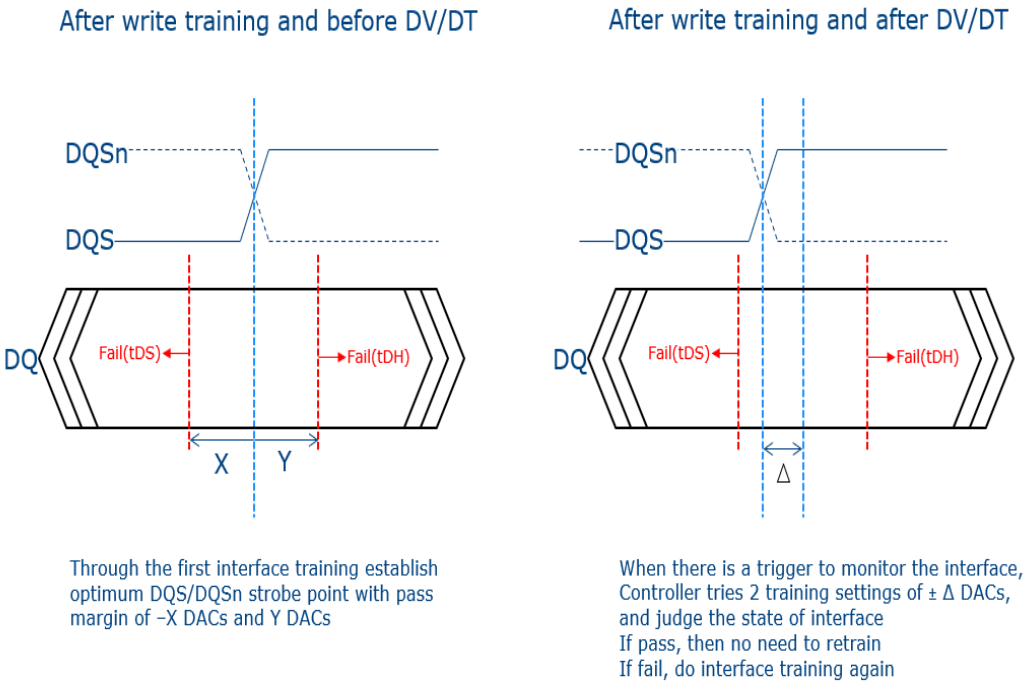


Figure 5-56 Write Training Monitoring Method

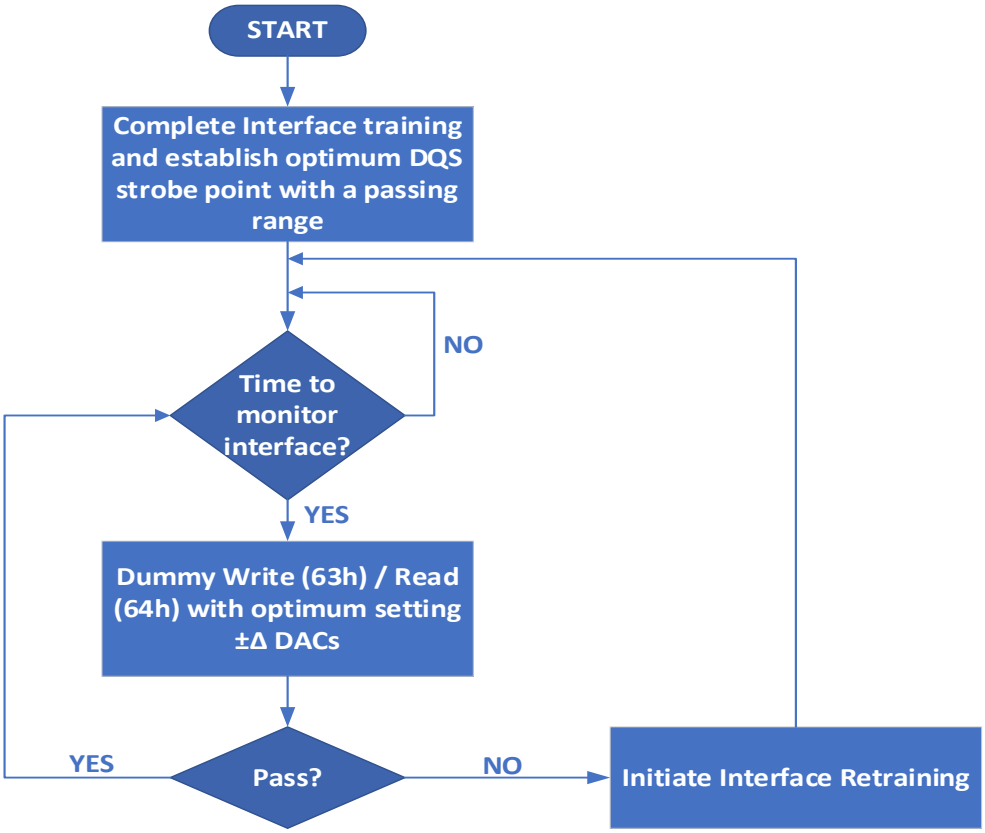


Figure 5-57 Write Training Monitor Flowchart

5.31.5. Channel ODT – FA 22h

The channel ODT (CH_ODT) setting shall be supported if the target supports the NV-LPDDR4 data interface. When the NV-LPDDR4 interface is enabled, the channel ODT setting controls the strength of the output pull-up device on the NAND. Using the channel ODT setting the host tells the NAND the ODT strength on the channel during NAND data output operations and the NAND adjusts the strength of its output pull-up devices accordingly to support the VOH,nom value. The channel ODT setting values that are supported are vendor specific. The channel ODT setting shall be retained across Reset (FFh), Synchronous Reset (FCh), and Reset LUN (FAh) commands. The power-on default channel ODT value is 50 Ohm (0110b).

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved (0)				Channel ODT (CH_ODT)			
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Table 5-20 Feature Address 22h

Channel ODT setting
0000b: Reserved
0001b: Reserved
0010b: 150 Ohms

0011b: 100 Ohms
0100b: 75 Ohms
0101b: 60 Ohms
0110b: 50 Ohms (default)
0111b: 37.5 Ohms
1000b: 25 Ohms
1001b-1111b Reserved

Reserved — Reserved values shall be cleared to zero by the host. Targets shall not be sensitive to the value of reserved fields.

5.31.6. Internal VrefQ Value – FA 23h

This setting shall be supported if the target supports the NV-LPDDR4 data interface. The internal VrefQ value setting shall be retained across Reset (FFh), Synchronous Reset (FCh), and Reset LUN (FAh) commands. The power-on default internal VrefQ value is 35% of VccQ (46h).

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Internal VrefQ Value							Reserved
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Table 5-21 Feature Address 23h

Internal VrefQ Value — This field controls the voltage level of the internal VrefQ.

Reserved — Reserved values shall be cleared to zero by the host. Targets shall not be sensitive to the value of reserved fields.

Internal VrefQ Value	VrefQ (% of VccQ)	Internal VrefQ Value	VrefQ (% of VccQ)	Internal VrefQ Value	VrefQ (% of VccQ)	Internal VrefQ Value	VrefQ (% of VccQ)	Internal VrefQ Value	VrefQ (% of VccQ)	Internal VrefQ Value	VrefQ (% of VccQ)	Internal VrefQ Value	VrefQ (% of VccQ)	Internal VrefQ Value	VrefQ (% of VccQ)
00h	0.0	10h	8.0	20h	16.0	30h	24.0	40h	32.0	50h	40.0	60h	48.0	70h	56.0
01h	0.5	11h	8.5	21h	16.5	31h	24.5	41h	32.5	51h	40.5	61h	48.5	71h	56.5
02h	1.0	12h	9.0	22h	17.0	32h	25.0	42h	33.0	52h	41.0	62h	49.0	72h	57.0
03h	1.5	13h	9.5	23h	17.5	33h	25.5	43h	33.5	53h	41.5	63h	49.5	73h	57.5
04h	2.0	14h	10.0	24h	18.0	34h	26.0	44h	34.0	54h	42.0	64h	50.0	74h	58.0
05h	2.5	15h	10.5	25h	18.5	35h	26.5	45h	34.5	55h	42.5	65h	50.5	75h	58.5
06h	3.0	16h	11.0	26h	19.0	36h	27.0	46h	35.0	56h	43.0	66h	51.0	76h	59.0
07h	3.5	17h	11.5	27h	19.5	37h	27.5	47h	35.5	57h	43.5	67h	51.5	77h	59.5
08h	4.0	18h	12.0	28h	20.0	38h	28.0	48h	36.0	58h	44.0	68h	52.0	78h	60.0
09h	4.5	19h	12.5	29h	20.5	39h	28.5	49h	36.5	59h	44.5	69h	52.5	79h	60.5

0Ah	5.0	1Ah	13.0	2Ah	21.0	3Ah	29.0	4Ah	37.0	5Ah	45.0	6Ah	53.0	7Ah	61.0
0Bh	5.5	1Bh	13.5	2Bh	21.5	3Bh	29.5	4Bh	37.5	5Bh	45.5	6Bh	53.5	7Bh	61.5
0Ch	6.0	1Ch	14.0	2Ch	22.0	3Ch	30.0	4Ch	38.0	5Ch	46.0	6Ch	54.0	7Ch	62.0
0Dh	6.5	1Dh	14.5	2Dh	22.5	3Dh	30.5	4Dh	38.5	5Dh	46.5	6Dh	54.5	7Dh	62.5
0Eh	7.0	1Eh	15.0	2Eh	23.0	3Eh	31.0	4Eh	39.0	5Eh	47.0	6Eh	55.0	7Eh	63.0
0Fh	7.5	1Fh	15.5	2Fh	23.5	3Fh	31.5	4Fh	39.5	5Fh	47.5	6Fh	55.5	7Fh	63.5

Table 5-22 Internal Vrefq Value Range/Step-Size for Type1 or Value1 Settings

For NAND devices that support Type3/Value3 settings (Vendor Specific, See Vendor datasheet) Table 5-23 Internal Vrefq Value Range/Step-Size for Type3 or Value3 settings gives the Range/Step-size/Tolerance

Internal VrefQ Type3 Range/Step Size				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Default	Vendor Specific			VccQ
Vref_min	Vendor Specific			VccQ
Vref_max	Vendor Specific but has to be greater than NAND Minimum Internal VrefQ Allowable max values			VccQ
Vref_step	Vendor specific. Vendor can specify Vref_step Typ to be within 0.25% - 0.75% of VccQ			VccQ
Vref_Set_Tol	-1.75%	0%	1.75%	VccQ

Table 5-23 Internal Vrefq Value Range/Step-Size for Type3 or Value3 settings

- VREFI is the VrefQ voltage inside the NAND. VREFI is calculated in the following manner: VREFI = (VrefQ Setting)*Vref_step + Vref_min.
- VrefQ Setting can range from 0 ~ 255 (8b)
- If the calculated VREFI ≥ Vref_max, then actual VREFI = Vref_max

A table showing feature address register setting versus the expected actual VREFI value can be derived using the formula above and represented in the vendor datasheet

5.31.6.1. Per-Pin VREFQ Training

Per-pin VrefQ adjustment is an optional feature that allows NAND devices to compensate for pin-pin timing variation. Per-pin VrefQ adjustment may be implemented by NAND vendors in one of two ways: either Per-Pin VrefQ Adjustment via Offset or Per-Pin VrefQ Adjustment via Absolute Setting. NAND vendors shall select one of the defined implementations (See Vendor datasheets for per-pin vrefq training support as well as method of training)

5.31.6.1.1. Per-Pin VREFQ Training via Offset

With this implementation, the base NAND VrefQ setting is provided by FA23h while FA40h & FA41h provide the pin specific offset information. The final VrefQ setting for a pin is determined by the base setting from FA23h and the offset information from FA40h/41/42h. The internal VrefQ value setting shall be retained across Reset (FFh), Synchronous Reset (FCh), and Reset LUN (FAh) commands.

For NAND vendors that implement per-pin VrefQ adjustment via the offset method, the following sub Features FA40h, FA41h and FA42h parameter definitions are used

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Vrefq Offset for DQ1				Vrefq Offset for DQ0			
P2	Vrefq Offset for DQ3				Vrefq Offset for DQ2			
P3	Vrefq Offset for DQ5				Vrefq Offset for DQ4			
P4	Vrefq Offset for DQ7				Vrefq Offset for DQ6			

Table 5-24 Feature Address 40h, Per-Pin Vrefq Adjustment DQ0-DQ7

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved (0)				Vrefq Offset for DBI			
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Table 5-25 Feature Address 41h, Per-Pin Vrefq Adjustment DBI

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved							
P2	Reserved							
P3	Reserved							
P4	Reserved							

Table 5-26 Feature Address 42h

For each Vrefq Offset setting in FA40h and FA41h

0000b: 0 step offset (default)
0001b: +1 step offset
0010b: +2 steps offset
0011b: +3 steps offset
0100b – 0111b: +4 ~ +7 steps offset
1000b: 0 step offset
1001b: -1 step offset
1010b: -2 steps offset
1011b: -3 steps offset
1100b – 1111b: -4 ~ -7 steps offset

Reserved — Reserved values shall be cleared to zero by the host. Targets shall not be sensitive to the value of reserved fields.

5.31.6.1.2. Per-Pin VREFQ Training via Absolute Setting

With this implementation, the pin specific final NAND VrefQ setting is provided by FA40h, FA41h & FA42h directly based on vendor choosing Type-1/Value-1 or Type-3/Value-3 definition. The internal VrefQ value setting shall be retained across Reset (FFh), Synchronous Reset (FCh), and Reset LUN (FAh) commands.

For NAND vendors that implement per-pin VrefQ adjustment via the absolute setting method, the following sub features FA40h, FA41h and FA42h parameter definitions are used

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Vrefq Setting for DQ0							
P2	Vrefq Setting for DQ1							
P3	Vrefq Setting for DQ2							
P4	Vrefq Setting for DQ3							

Table 5-27 Feature Address 40h, Per-Pin Vrefq adjustment DQ0-DQ3

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Vrefq Setting for DQ4							
P2	Vrefq Setting for DQ5							
P3	Vrefq Setting for DQ6							
P4	Vrefq Setting for DQ7							

Table 5-28 Feature Address 41h, Per-Pin Vrefq adjustment DQ4-DQ7

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Vrefq Setting for DBI							
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Table 5-29 Feature Address 42h, Per-Pin Vrefq adjustment DBI

Reserved — Reserved values shall be cleared to zero by the host. Targets shall not be sensitive to the value of reserved fields.

5.31.7. External Vpp Configuration – FA 30h

This setting shall be supported if the target supports external Vpp as specified in the parameter page. This setting controls whether external Vpp is enabled. These settings are retained across Reset (FFh), Synchronous Reset (FCh) and Reset LUN (FAh) commands. The power-on default is 0h for all fields.

Vpp must be valid prior to the Set Feature that enables Vpp.

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved (0)							Vpp
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Table 5-30 Feature Address 30h, VPP COnfiguration

Vpp — 0b = External Vpp is disabled
1b = External Vpp is enabled

Reserved	Reserved values shall be cleared to zero by the host. Targets shall not be sensitive to the value of reserved fields.

5.31.8. Volume Configuration – FA 58h

This setting is used to configure the Volume Address and shall be supported for NAND Targets that indicate support for Volume Addressing in the parameter page. After the Volume Address is appointed, the ENo pin for that Volume is set to one, the ENi pin for that Volume is ignored until the next power cycle, and the Volume is deselected until a Volume Select command is issued that selects the associated Volume.

The host shall only set this feature once per power cycle for each Volume. The address specified is then used in Select Volume commands for accessing this NAND Target. This setting is retained across Reset (FFh), Synchronous Reset (FCh), and Reset LUN (FAh) commands. There is no default power-on value.

Sub Feature Parameter	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P1	Reserved				Volume Address			
P2	Reserved							
P3	Reserved							
P4	Reserved							

Table 5-31 Feature Address 58h, Volume Address configuration

Volume Address	Specifies the Volume address to appoint

6. Multi-plane Operations

A LUN may support multi-plane read, program and erase operations. Multi-plane operations are when multiple commands of the same type are issued to different blocks on the same LUN. Refer to section 5.7.1.28 for addressing restrictions with multi-plane operations. There are two methods for multi-plane operations: concurrent and overlapped.

When performing multi-plane operations, the operations/functions shall be the same type. The functions that may be used in multi-plane operations are:

- Page Program
- Copyback Read and Program
- Block Erase
- Read

6.1. Requirements

When supported, the plane address comprises the lowest order bits of the block address as shown in Figure 3-3. The LUN address is required to be the same. The block address (other than the plane address bits) may be required to be the same, refer to section 5.7.1.28. Some devices or multi-plane operations may require page addresses to be the same as other multi-plane operations in the multi-plane command sequence. Refer to the vendor datasheet for the multi-plane operation restrictions applicable to the device.

For copyback program operations, the restrictions are the same as for a multi-plane program operation. However, copyback reads shall be previously issued to the same plane addresses as those in the multi-plane copyback program operations. The reads for copyback may be issued non-multi-plane or multi-plane. If the reads are non-multi-plane then the reads may have different page addresses. If the reads are multi-plane then the reads shall have the same page addresses.

Multi-plane operations enable operations of the same type to be issued to other blocks on the same LUN. There are two methods for multi-plane operations: concurrent and overlapped. The concurrent multi-plane operation waits until all command, address, and data are entered for all plane addresses before accessing the Flash array. The overlapped multi-plane operation begins its operation immediately after the command, address and data are entered and performs it in the background while the next multi-plane command, address, and data are entered.

The plane address component of each address shall be distinct. A single multi-plane (cached) program operation is shown in Figure 6-1. Between “Multi-plane Op 1” and “Multi-plane Op n”, all plane addresses shall be different from each other. After the 10h or 15h (cached) command cycle is issued, previously issued plane addresses can be used in future multi-plane operations.

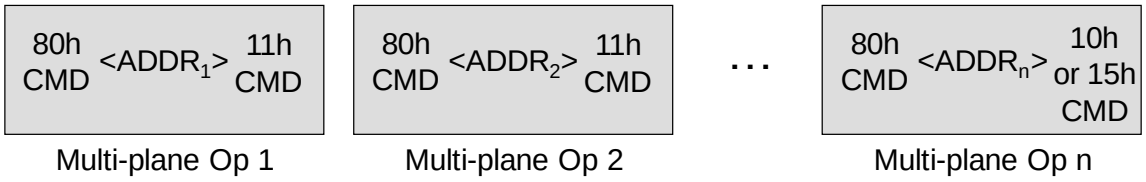


Figure 6-1 Multi-plane Program (Cache)

For multi-plane erase operations, the plane address component of each address shall be distinct. A single multi-plane erase operation is shown in Figure 6-2. Between “Multi-plane Op 1” and “Multi-plane Op n”, all plane addresses shall be different from each other. After the D0h command cycle is issued, previously issued plane addresses can be used in future multi-plane operations.

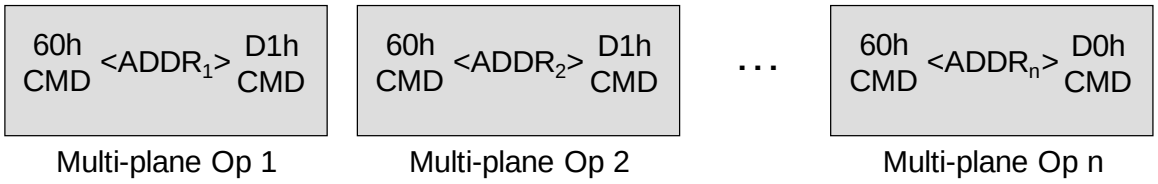


Figure 6-2 Multi-plane Erase

The plane address component of each address shall be distinct. A single multi-plane read (cache) operation is shown in Figure 6-3. Between “Multi-plane Op 1” and “Multi-plane Op n”, all plane addresses shall be different from each other. After the 30h or 31h (cached) command cycle is issued, previously issued plane addresses can be used in future multi-plane operations.

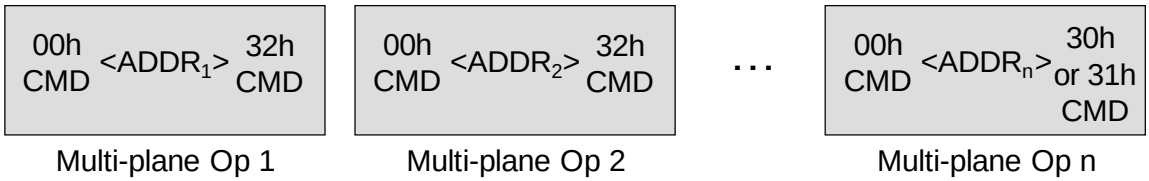


Figure 6-3 Multi-plane Read (Cache)

6.2. Status Register Behavior

Some status register bits are independent per plane address. Other status register bits are shared across the entire LUN. This section defines when status register bits are independent per plane address. This is the same for concurrent and overlapped operations.

For multi-plane program and erase operations, the FAIL/FAILC bits are independent per plane address. The RDY and ARDY bits may be independent per plane address, see vendor datasheet. Table 6-1 lists whether a bit is independent per plane address or shared across the entire LUN for multi-plane operations.

Value	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Status Register	WP_n	RDY	ARDY	VSP	VSP	VSP	FAILC	FAIL
Independent	N	VSP	VSP	N	N	N	Y	Y

Table 6-1 Independent Status Register bits

6.3. Multi-plane Page Program

The Page Program command transfers a page or portion of a page of data identified by a column address to the page register. The contents of the page register are then programmed into the Flash array at the row address indicated. With a multi-plane operation, multiple programs can be issued back to back to the LUN, with a shorter busy time between issuance of the next program operation. Figure 6-4 defines the behavior and timings for two multi-plane page program commands.

Cache operations may be used when doing multi-plane page program operations, as shown, if supported by the target as indicated in the parameter page. Refer to section 5.7.1.27.

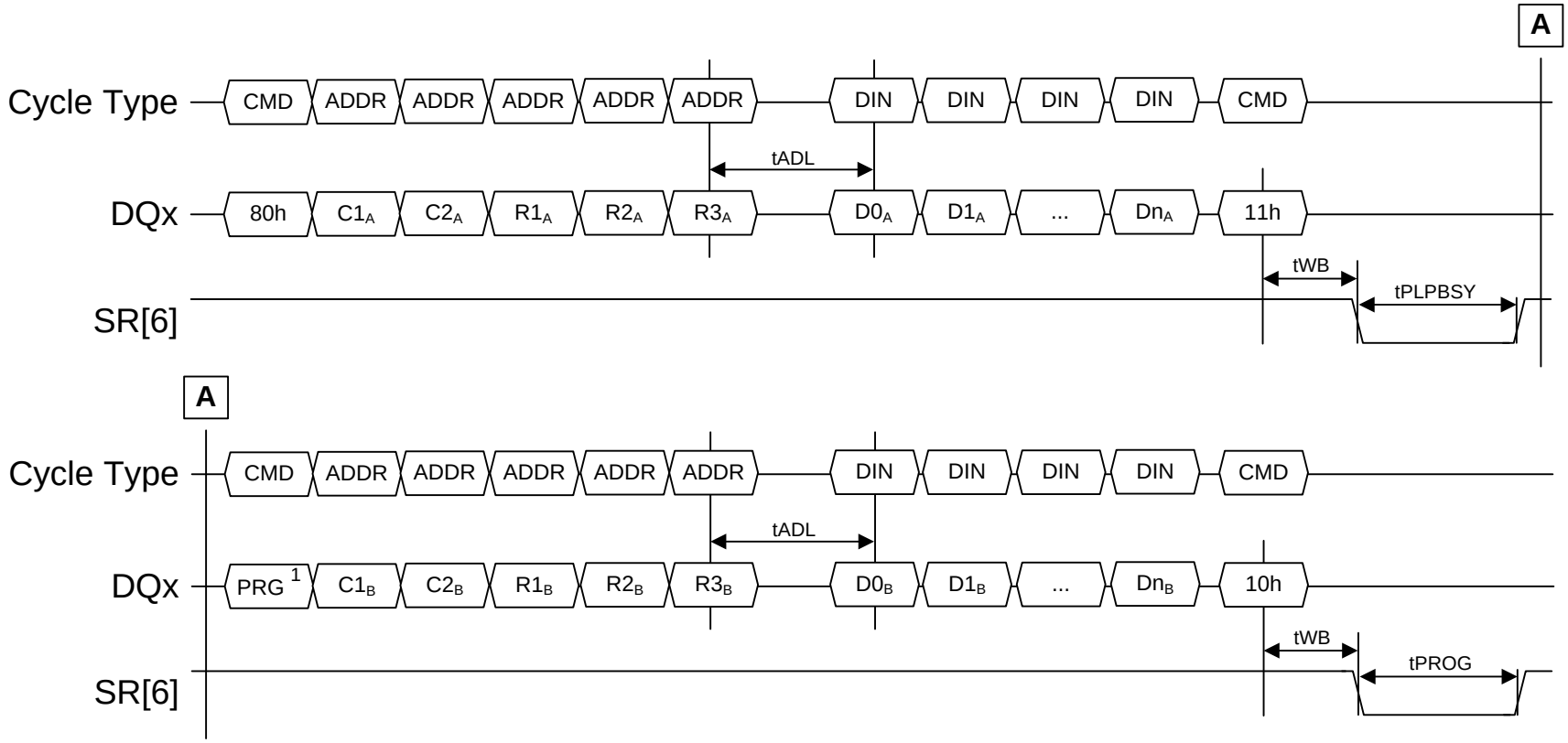


Figure 6-4 Multi-plane Page Program timing

Notes:

1. There are two forms of Multi-plane Page Program. ONFI 1.x and 2.x revisions have defined all first cycles for all program sequences in a Multi-plane Page Program as 80h. The ONFI-JEDEC Joint Taskgroup has defined the subsequent first cycles after the initial program sequence in a Multi-plane Page Program as 81h. Refer to the parameter page to determine if the device supports subsequent first cycles in a program sequence as 81h.

$C1_A$-$C2_A$ Column address for page A. $C1_A$ is the least significant byte.

$R1_A$-$R3_A$ Row address for page A. $R1_A$ is the least significant byte.

$D0_A$-Dn_A Data to program for page A.

PRG 80h or 81h. Refer to Note 1.

$C1_B$-$C2_B$ Column address for page B. $C1_B$ is the least significant byte.

$R1_B$-$R3_B$ Row address for page B. $R1_B$ is the least significant byte.

$D0_B$-Dn_B Data to program for page B.

The row addresses for page A and B shall differ in the plane address bits.

Finishing a multi-plane program with a command cycle of 15h rather than 10h indicates that this is a cache operation. The host shall only issue a command cycle of 15h to complete an multi-plane program operation if program cache is supported with multi-plane program operations, as described in section 5.7.1.27.

6.4. Multi-plane Copyback Read and Program

The Copyback function reads a page of data from one location and then moves that data to a second location. With a multi-plane operation, the Copyback Program function can be issued back to back to the target, with a shorter busy time between issuance of the next Copyback Program. Figure 6-5, Figure 6-6, and Figure 6-7 define the behavior and timings for two Copyback Program operations. The reads for the Copyback Program may or may not be multi-plane. Figure 6-5 defines the non-multi-plane read sequence and Figure 6-6 defines the multi-plane read sequence.

The plane addresses used for the Copyback Read operations (regardless of multi-plane) shall be the same as the plane addresses used in the subsequent multi-plane Copyback Program operations.

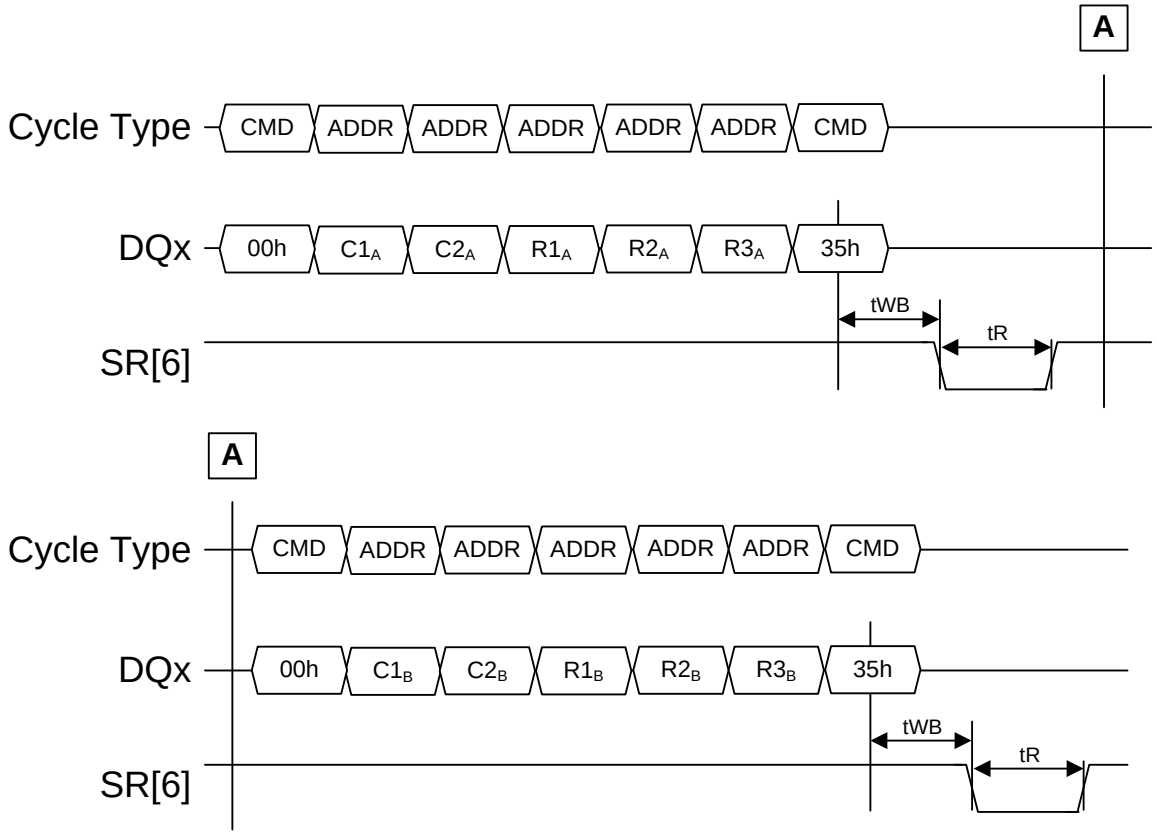


Figure 6-5 Non-multi-plane Copyback Read timing for multi-plane Copyback Program

$C1_A$-$C2_A$ Column address for source page A. $C1_A$ is the least significant byte.

$R1_A$-$R3_A$ Row address for source page A. $R1_A$ is the least significant byte.

$C1_B$-$C2_B$ Column address for source page B. $C1_B$ is the least significant byte.

$R1_B$-$R3_B$ Row address for source page B. $R1_B$ is the least significant byte.

The row addresses for all source pages shall differ in their plane address bits.

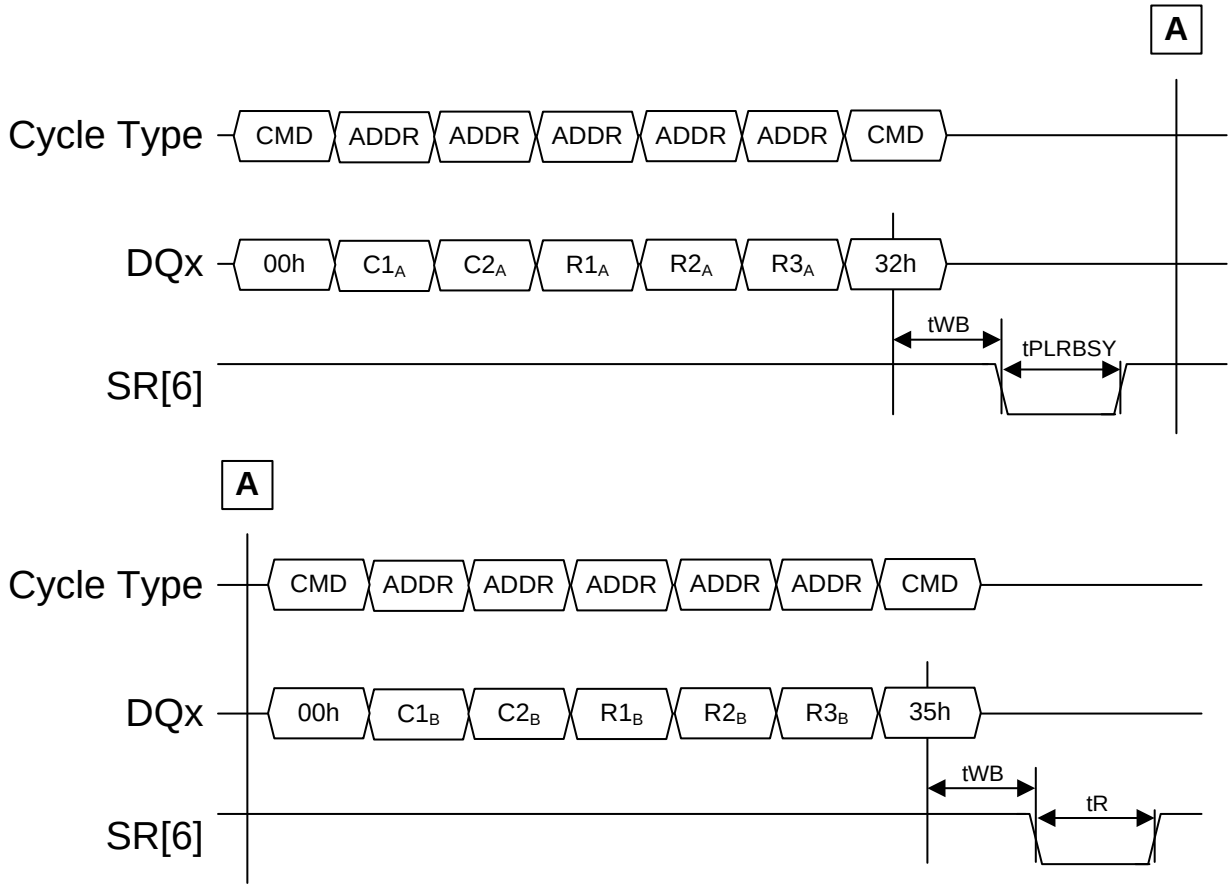


Figure 6-6 Multi-plane Copyback Read timing for Multi-plane Copyback Program

$C1_A$-$C2_A$	Column address for source page A. $C1_A$ is the least significant byte.
$R1_A$-$R3_A$	Row address for source page A. $R1_A$ is the least significant byte.
$C1_B$-$C2_B$	Column address for source page B. $C1_B$ is the least significant byte.
$R1_B$-$R3_B$	Row address for source page B. $R1_B$ is the least significant byte.

The row addresses for all source pages shall differ in their plane address bits. The source page addresses shall be the same for multi-plane reads.

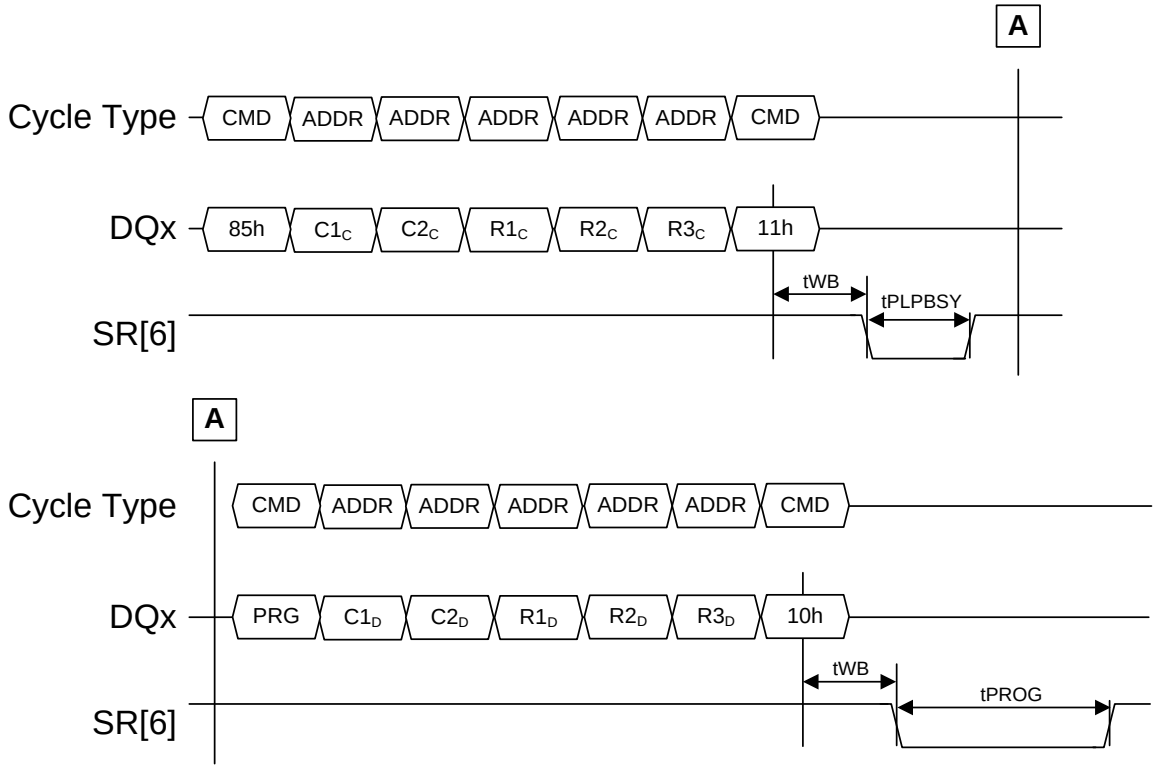


Figure 6-7 Multi-plane Copyback Program

Notes:

1. There are two forms of Multi-plane Copyback Program. ONFI 1.x and 2.x revisions have defined all first cycles for all program sequences in a Multi-plane Copyback Program as 85h. The ONFI-JEDEC Joint Taskgroup has defined the subsequent first cycles after the initial Copyback Program sequence in a Multi-plane Copyback Program as 81h. Refer to the parameter page to determine if the device supports subsequent first cycles in a Multi-plane Copyback Program sequence as 81h.

$C1_C$-$C2_C$ Column address for destination page C. $C1_C$ is the least significant byte.

$R1_C$-$R3_C$ Row address for destination page C. $R1_C$ is the least significant byte.

PRG 85h or 81h. Refer to Note 1.

$C1_D$-$C2_D$ Column address for destination page D. $C1_D$ is the least significant byte.

$R1_D$-$R3_D$ Row address for destination page D. $R1_D$ is the least significant byte.

The row addresses for all destination pages shall differ in their plane address bits. The page address for all destination addresses for multi-plane copyback operations shall be identical.

6.5. Multi-plane Block Erase

Figure 6-8 defines the behavior and timings for a multi-plane block erase operation. Only two operations are shown, however additional erase operations may be issued with a 60h/D1h sequence prior to the final 60h/D0h sequence depending on how many multi-plane operations the LUN supports.

The ONFI-JEDEC Joint Taskgroup has defined a modified version of multi-plane block erase, where subsequent row addresses specifying additional blocks to erase are not separated by D1h commands. This definition is shown in Figure 6-9. Refer to the parameter page to determine if the device supports not including the D1h command between block addresses.

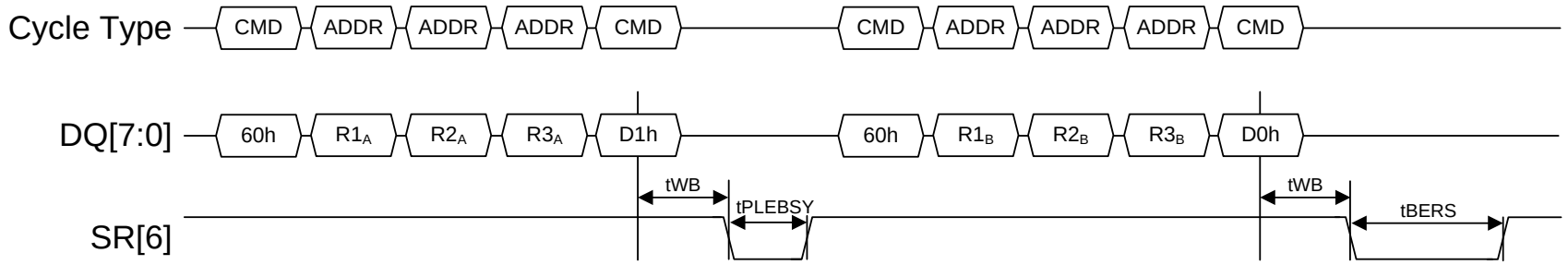


Figure 6-8 Multi-plane Block Erase timing

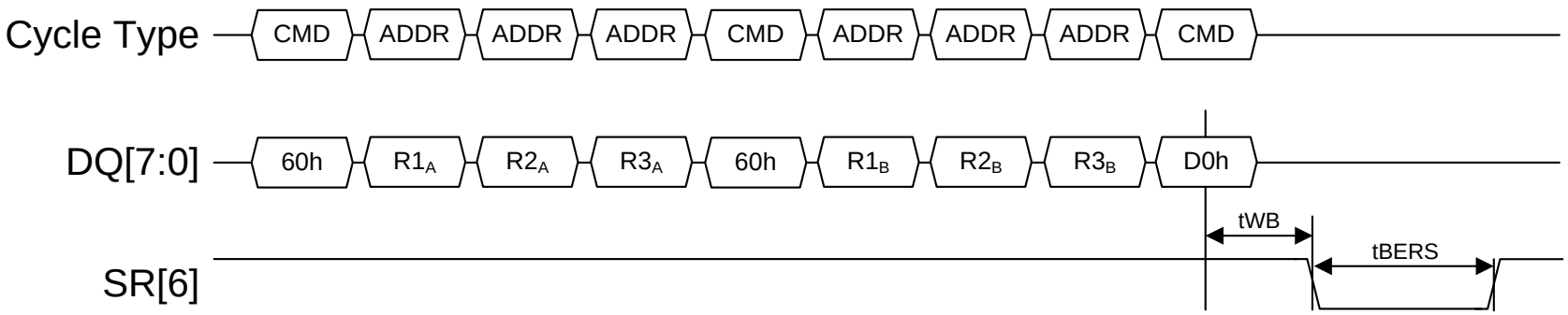


Figure 6-9 Multi-plane Block Erase timing, ONFI-JEDEC Joint Taskgroup primary definition

$R1_A$-$R3_A$ Row address for erase block A. $R1_A$ is the least significant byte.

$R1_B$-$R3_B$ Row address for erase block B. $R1_B$ is the least significant byte.

6.6. Multi-plane Read

The Read command reads a page of data identified by a row address for the LUN specified. The page of data is made available to be read from the page register starting at the column address specified. With a multi-plane operation, multiple reads can be issued back to back to the LUN, with a shorter busy time between issuance of the next read operation. Figure 6-10 defines the behavior and timings for issuing two multi-plane read commands. Figure 6-11 defines the behavior and timings for reading data after the multi-plane read commands are ready to return data.

Cache operations may be used when doing multi-plane read operations, as shown, if supported by the target as indicated in the parameter page. Refer to section 5.7.1.27.

Change Read Column Enhanced shall be issued prior to reading data from a LUN. If data is read without issuing a Change Read Column Enhanced, the output received is undefined.

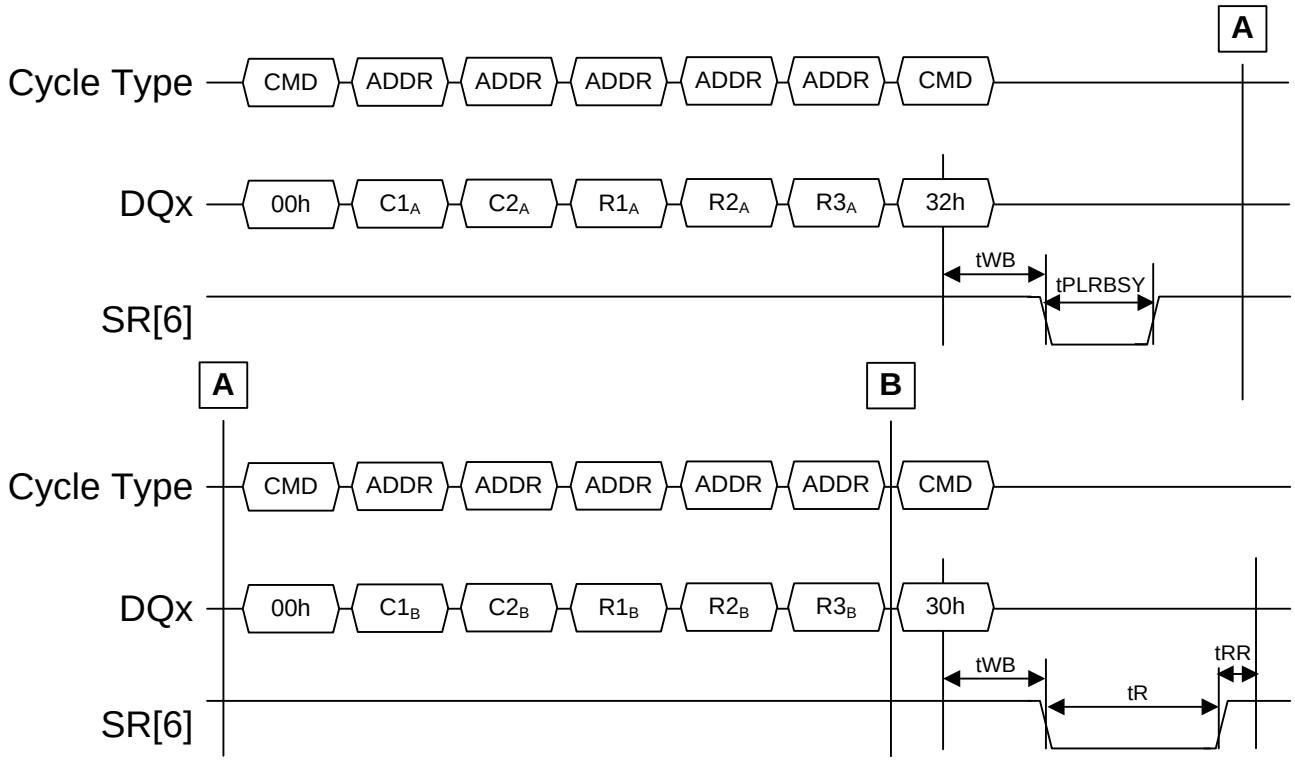


Figure 6-10 Multi-plane Read command issue timing

$C1_A$-$C2_A$ Column address for page A. $C1_A$ is the least significant byte.

$R1_A$-$R3_A$ Row address for page A. $R1_A$ is the least significant byte.

$C1_B$-$C2_B$ Column address for page B. $C1_B$ is the least significant byte.

$R1_B$-$R3_B$ Row address for page B. $R1_B$ is the least significant byte.

The row addresses for page A and B shall differ in the plane address bits.

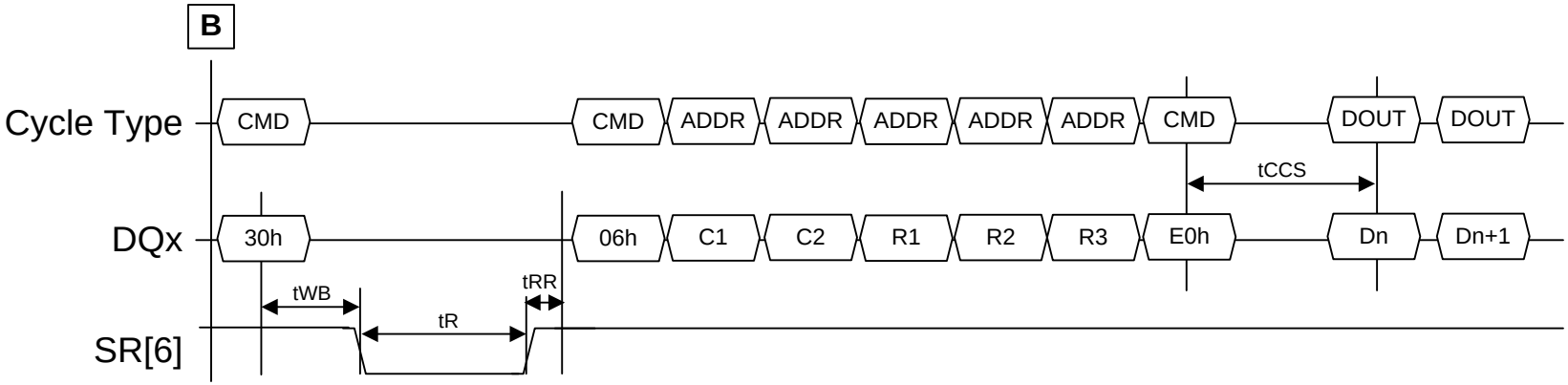


Figure 6-11 Multi-plane Read data output timing, continued from command issue

C1-C2 Column address to read from. C1 is the least significant byte.

R1-R3 Row address to read from (specifies LUN and plane address). R1 is the least significant byte.

Dn Data bytes read starting with addressed row and column.

The row address provided shall specify a LUN and plane address that has valid read data.

For Multi-plane Read Cache Sequential operations, the initial Multi-plane Read command issue is followed by a Read Cache confirmation opcode 31h, as shown in Figure 6-12.

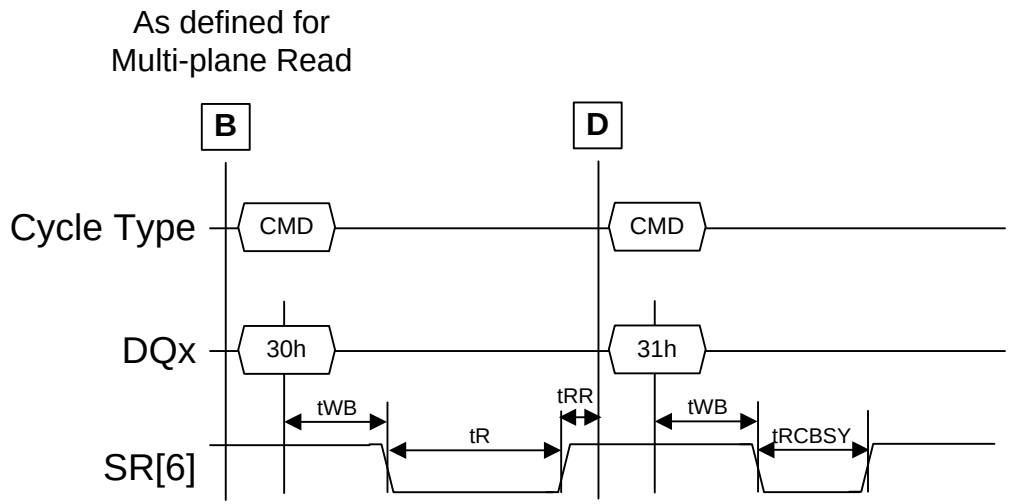


Figure 6-12 Multi-plane Read Cache Sequential command issue timing

For Multi-plane Read Cache Random operations, the initial multi-plane Read command issue is followed by another Read Multi-plane command sequence where the last confirmation opcode is 31h, as shown in Figure 6-13.

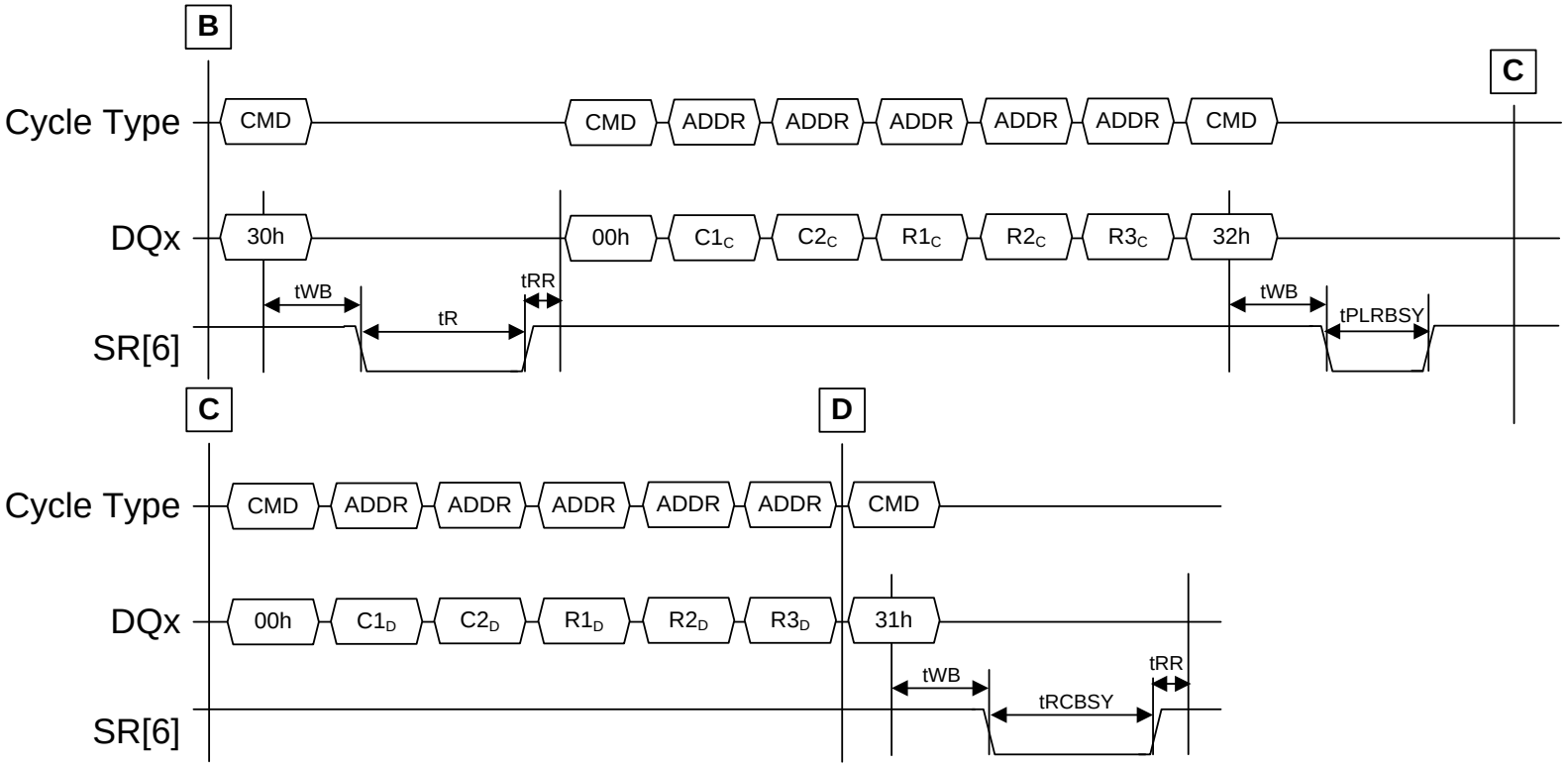


Figure 6-13 Multi-plane Read Cache Random command issue timing

$C1_C$-$C2_C$	Column address for page C. $C1_C$ is the least significant byte.
$R1_C$-$R3_C$	Row address for page C. $R1_C$ is the least significant byte.
$C1_D$-$C2_D$	Column address for page D. $C1_D$ is the least significant byte.
$R1_D$-$R3_D$	Row address for page D. $R1_D$ is the least significant byte.

The row addresses for page C and D shall differ in the plane address bits.

For Multi-plane Read Cache operations, two data output operations follow each Multi-plane Read Cache operation. The individual data output sequences are described in Figure 6-11. Prior to the last set (i.e. two) data output operations, a Read Cache End command (3Fh) should be issued by the host.

7. Behavioral Flows

7.1. Target behavioral flows

The Target state machine describes the allowed sequences when operating with the target. If none of the arcs are true, then the target remains in the current state.

7.1.1. Variables

This section describes variables used within the Target state machine.

tbStatusOut This variable is set to TRUE when a data read cycle should return the status value. The power-on value for this variable is FALSE.

tbChgCol This variable is set to TRUE when changing the column using Change Read Column is allowed. The power-on value for this variable is FALSE.

tbChgColEnh This variable is set to TRUE when changing the column using Change Read Column Enhanced is allowed. The power-on value for this variable is FALSE.

tCopyback This variable is set to TRUE if the Target is issuing a copyback command. The power-on value for this variable is FALSE.

tLunSelected This variable contains the LUN that is currently selected by the host. The power-on value for this variable is 0.

tLastCmd This variable contains the first cycle of the last command (other than 70h/78h) received by the Target.

tReturnState This variable contains the state to return to after status operations.

tbStatus78hReq This variable is set to TRUE when the next status operation shall be a 78h command (and not a 70h command). The power-on value for this variable is FALSE.

7.1.2. Idle states

T_PowerOn[1]	The target performs the following actions: 1. R/B_n is cleared to zero. 2. Each LUN shall draw less than 10 mA of power per staggered power-up requirement.

1. Target is ready to accept FFh (Reset) command[2]	→	T_PowerOnReady

NOTE:
1. This state is entered as a result of a power-on event when Vcc reaches Vcc_min.
2. This arc shall be taken within 1 millisecond of Vcc reaching Vcc_min.

T_PowerOnReady	The target performs the following actions: 1. R/B_n is set to one. 2. Each LUN shall draw less than 10mA of power per staggered power-up requirement.

1. Command cycle FFh (Reset) received	→	T_RST_PowerOn

T_Idle	tCopyback set to FALSE. tReturnState set to T_Idle.		
1.	WP_n signal transitioned	→	T_Idle_WP_Transition
2.	LUN indicates its SR[6] value transitioned	→	T_Idle_RB_Transition
3.	Command cycle received	→	T_Cmd_Decode

T_Cmd_Decode[1]	Decode command received. tbStatusOut is set to FALSE. If R/B_n is set to one and command received is not 70h (Read Status), then tbStatus78hReq is set to FALSE.		
1.	(Command 80h (Page Program) or command 60h (Block Erase) decoded) and WP_n is low	→	T_Idle
2.	Command FFh (Reset) decoded	→	T_RST_Execute
3.	Command FCh (Synchronous Reset) decoded	→	T_RST_Execute_Sync
4.	Command FAh (Reset LUN) decoded	→	T_RST_Execute_LUN
5.	Command 90h (Read ID) decoded	→	T_RID_Execute
6.	Command ECh (Read Parameter Page) decoded	→	T_RPP_Execute
7.	Command EDh (Read Unique ID) decoded	→	T_RU_Execute
8.	Command 80h (Page Program) decoded and WP_n is high	→	T_PP_Execute
9.	Command 60h (Block Erase) decoded and WP_n is high	→	T_BE_Execute
10.	Command 00h (Read) decoded	→	T_RD_Execute
11.	Command EFh (Set Features) decoded	→	T_SF_Execute
12.	Command EEh (Get Features) decoded	→	T_GF_Execute
13.	Command 70h (Read Status) decoded	→	T_RS_Execute
14.	Command 78h (Read Status Enhanced) decoded	→	T_RSE_Execute
15.	Command E1h (Volume Select) decoded	→	T_VS_Execute
16.	Command E2h (ODT Configure) decoded	→	T_ODTC_Execute
NOTE: 1. The host shall ensure R/B_n is set to one before issuing Target level commands (Reset, Read ID, Read Parameter Page, Read Unique ID, Set Features, Get Features).			

T_Idle_WP_Transition	Indicate WP_n value to all LUN state machines.		
1.	State entered from T_Idle_Rd	→	T_Idle_Rd
2.	Else	→	T_Idle

T_Idle_RB_Transition	R/B_n is set to the AND of all LUN status register SR[6] values.[1]		
1.	Unconditional	→	tReturnState
NOTE: 1. R/B_n may transition to a new value prior to the Target re-entering an idle condition when LUN level commands are in the process of being issued.			

7.1.3. Idle Read states

T_Idle_Rd	Wait for read request (data or status) or other action. tReturnState set to T_Idle_Rd.	
1. WP_n signal transitioned	→	T_Idle_WP_Transition
2. LUN indicates its SR[6] value transitioned	→	T_Idle_RB_Transition
3. Read request received and tbStatusOut set to TRUE	→	T_Idle_Rd_Status
4. Read request received and (tLastCmd set to 90h or EEh)	→	T_Idle_Rd_XferByte
5. Read request received and (tLastCmd set to ECh or EDh)	→	T_Idle_Rd_LunByte
6. Read request received and tbStatus78hReq set to FALSE[1]	→	T_Idle_Rd_LunData
7. Command cycle 05h (Change Read Column) received and tbChgCol set to TRUE	→	T_CR_Execute[2]
8. Command cycle 06h (Change Read Column Enhanced) received and tbChgColEnh set to TRUE	→	T_CRE_Execute[2]
9. Command cycle of 31h received and tbStatus78hReq set to FALSE	→	T_Idle_Rd_CacheCmd
10. Command cycle of 3Fh received and tLastCmd set to 31h and tbStatus78hReq set to FALSE	→	T_Idle_Rd_CacheCmd
11. Command cycle received	→	T_Cmd_Decode
NOTE: 1. When tbStatus78hReq is set to TRUE, a Read Status Enhanced (78h) command followed by a 00h command shall be issued by the host prior to reading data from a particular LUN. (NOTE: Some NAND vendors may require the use of Change Read Column sequence instead of 00h command to output data from the NAND, see vendor datasheet) 2. If there are reads outstanding on other LUNs for this target, a Change Read Column (Enhanced) shall be issued before transferring data. Refer to section 3.1.3 that describes multiple LUN operation restrictions.		

T_Idle_Rd_CacheCmd	Set tLastCmd to the command received. Pass command received to LUN tLunSelected	
1. Unconditional	→	T_Idle_Rd

T_Idle_Rd_XferByte	Return next byte of data.	
1. Unconditional	→	T_Idle_Rd

T_Idle_Rd_LunByte	Request byte of data from page register of LUN tLunSelected.	
1. Byte received from LUN tLunSelected	→	T_Idle_Rd_XferHost

T_Idle_Rd_LunData	Request byte (x8) or word (x16) of data from page register of LUN tLunSelected.

1. Byte or word received from LUN tLunSelected	→	T_Idle_Rd_XferHost

T_Idle_Rd_XferHost	Transfer data byte or word received from LUN tLunSelected to host.	
1. tReturnState set to T_RD_StatusOff and tCopyback set to TRUE	→	T_RD_Copyback
2. tReturnState set to T_RD_StatusOff	→	T_Idle_Rd
3. Else	→	tReturnState

T_Idle_Rd_Status	Request status from LUN tLunSelected.	
1. Status from LUN tLunSelected received	→	T_Idle_Rd_StatusEnd

T_Idle_Rd_StatusEnd	Transfer status byte received from LUN tLunSelected to host.	
1. Unconditional	→	tReturnState

T_CR_Execute	Wait for a column address cycle.	
1. Column address cycle received	→	T_CR_Addr

T_CR_Addr	Store the column address cycle received.	
1. More column address cycles required	→	T_CR_Execute
2. All column address cycles received	→	T_CR_WaitForCmd

T_CR_WaitForCmd	Wait for a command cycle.	
1. Command cycle E0h received	→	T_CR_ReturnToData

T_CR_ReturnToData	Request that LUN tLunSelected select the column in the page register based on the column address received.	
1. tReturnState set to T_PP_MplWait	→	T_PP_WaitForDataOut
2. tReturnState set to T_RD_Status_Off	→	T_Idle_Rd
3. Else	→	tReturnState

T_CRE_Execute	Wait for a column address cycle.	
1. Column address cycle received	→	T_CRE_ColAddr

T_CRE_ColAddr	Store the column address cycle received.	
1. More column address cycles required	→	T_CRE_Execute
2. All column address cycles received	→	T_CRE_RowAddrWait

T_CRE_RowAddrWait	Wait for a row address cycle.		
1. Row address cycle received		→	T_CRE_RowAddr

T_CRE_RowAddr	Store the row address cycle received.		
1. More row address cycles required		→	T_CRE_RowAddrWait
2. All row address cycles received		→	T_CRE_WaitForCmd

T_CRE_WaitForCmd	Wait for a command cycle.		
1. Command cycle E0h received		→	T_CRE_ReturnToData

T_CRE_ReturnToData	The target performs the following actions: 1. Set tLunSelected to LUN selected by row address received. 2. Request that LUN tLunSelected select the column in the page register based on the column address received. 3. Indicate plane address received to tLunSelected for use in data output. 4. Request all idle LUNs not selected turn off their output buffers.[1]		
1. tReturnState set to T_PP_MplWait		→	T_PP_WaitForDataOut
2. tReturnState set to T_RD_Status_Off		→	T_Idle_Rd
3. Else		→	tReturnState
NOTE: 1. LUNs not selected only turn off their output buffers if they are in an idle condition (SR[6] is one) when Change Read Column Enhanced is received. If LUNs are active (SR[6] is zero) when Change Read Column Enhanced is issued, then the host shall issue a Read Status Enhanced (78h) command prior to subsequent data output to ensure all LUNs that are not selected turn off their output buffers.			

7.1.4. Reset command states

T_RST_PowerOn	The target performs the following actions: 1. tLastCmd set to FFh. 2. tbStatusOut is set to FALSE. 3. The target sends a Reset request to each LUN.		
1. Unconditional		→	T_RST_PowerOn_Exec

T_RST_PowerOn_Exec	The target performs the following actions: 1. Target level reset actions are performed. 2. R/B_n is set to zero.		
1. Unconditional		→	T_RST_Perform

T_RST_Execute[1]	The target performs the following actions: 1. tLastCmd set to FFh. 2. The target selects the SDR data interface. 3. The target sends a Reset request to each LUN. 4. Set tbChgCol to FALSE. 5. Set tbChgColEnh to FALSE. 6. Request all LUNs invalidate page register(s).

1. Unconditional	→	T_RST_Perform

NOTE:
1. This state is entered as a result of receiving a Reset (FFh) command in any other state, except if this is the first Reset after power-on.

T_RST_Execute_Sync[1]	The target performs the following actions: 1. tLastCmd set to FCh. 2. tbStatusOut is set to FALSE. 3. The target sends a Reset request to each LUN. 4. Set tbChgCol to FALSE. 5. Set tbChgColEnh to FALSE. 6. Request all LUNs invalidate page register(s).

1. Unconditional	→	T_RST_Perform

NOTE:
1. This state is entered as a result of receiving a Synchronous Reset (FCh) command in any other state.

T_RST_Execute_LUN[1]	The target performs the following actions: 1. tLastCmd set to FAh. 2. tbStatusOut is set to FALSE. 3. Set tbChgCol to FALSE. 4. Set tbChgColEnh to FALSE. 5. Wait for an address cycle.

1. Unconditional	→	T_RST_LUN_Addr

T_RST_LUN_AddrWait	Wait for an address cycle.		
	1. Address cycle received	→	T_RST_LUN_Addr

T_RST_LUN_Addr	Store the address cycle received.		
	1. More address cycles required	→	T_RST_LUN_AddrWait
	2. All address cycles received	→	T_RST_LUN_Perform

T_RST_LUN_Perform	The target performs the following actions: 1. The target sends a Reset request to the addressed LUN. 2. R/B_n is cleared to zero. 3. Request the addressed LUN invalidate its page register.		
	1. Addressed LUN reset actions are complete and tbStatusOut is set to FALSE	→	T_Idle
	2. Addressed LUN reset actions are complete and tbStatusOut is set to TRUE	→	T_Idle_Rd

T_RST_Perform	The target performs the following actions: 1. Target level reset actions are performed. 2. R/B_n is set to zero. 3. tReturnState set to T_RST_Perform.		
	1. Target and LUN reset actions are complete	→	T_RST_End
	2. Command cycle 70h (Read Status) received	→	T_RS_Execute
	3. Read request received and tbStatusOut is set to TRUE	→	T_Idle_Rd_Status

T_RST_End	The target performs the following actions: 1. R/B_n is set to one.		
	1. tbStatusOut is set to FALSE	→	T_Idle
	2. tbStatusOut is set to TRUE	→	T_Idle_Rd

7.1.5. Read ID command states

T_RID_Execute	The target performs the following actions: 1. tLastCmd set to 90h. 2. Wait for an address cycle. 3. Set tbChgCol to FALSE. 4. Set tbChgColEnh to FALSE. 5. Request all LUNs invalidate page register(s).		
	1. Address cycle of 00h received	→	T_RID_Addr_00h
	2. Address cycle of 20h received	→	T_RID_Addr_20h

T_RID_Addr_00h	Wait for the read request.		
	1. Read byte request received	→	T_RID_ManufacturerID
	2. Command cycle received	→	T_Cmd_Decode

T_RID_ManufacturerID	Return the JEDEC manufacturer ID.		
	1. Read byte request received	→	T_RID_DeviceID
	2. Command cycle received	→	T_Cmd_Decode

T_RID_DeviceID	Return the device ID.[1]		
	1. Unconditional	→	T_Idle_Rd
	NOTE: 1. Reading bytes beyond the device ID returns vendor specific values.		

T_RID_Addr_20h	Wait for the read request.		
	1. Read byte request received	→	T_RID_Signature
	2. Command cycle received	→	T_Cmd_Decode

T_RID_Signature	Return next ONFI signature byte.[1]		
	1. Last ONFI signature byte returned	→	T_Idle_Rd
	2. Else	→	T_RID_Addr_20h
	NOTE: 1. Reading beyond the fourth byte returns indeterminate values.		

7.1.6. Read Parameter Page command states

T_RPP_Execute	The target performs the following actions: 1. tLastCmd set to ECh. 2. Set tbChgCol to TRUE. 3. Set tbChgColEnh to FALSE. 4. Wait for an address cycle. 5. Request all LUNs invalidate page register(s). 6. Target selects LUN to execute parameter page read, sets tLunSelected to the address of this LUN.		
	1. Address cycle of 00h received	→	T_RPP_ReadParams

T_RPP_ReadParams	The target performs the following actions: 1. Request LUN tLunSelected clear SR[6] to zero. 2. R/B_n is cleared to zero. 3. Request LUN tLunSelected make parameter page data available in page register. 4. tReturnState set to T_RPP_ReadParams_Cont.

1. Read of page complete	→	T_RPP_Complete
2. Command cycle 70h (Read Status) received	→	T_RS_Execute
3. Read request received and tbStatusOut set to TRUE	→	T_Idle_Rd_Status

T_RPP_ReadParams_Cont	

1. Read of page complete	→	T_RPP_Complete
2. Command cycle 70h (Read Status) received	→	T_RS_Execute
3. Read request received and tbStatusOut set to TRUE	→	T_Idle_Rd_Status

T_RPP_Complete	Request LUN tLunSelected set SR[6] to one. R/B_n is set to one.

1. Unconditional	→	T_Idle_Rd

7.1.7. Read Unique ID command states

T_RU_Execute	The target performs the following actions: 1. tLastCmd set to EDh. 2. Set tbChgCol to TRUE. 3. Set tbChgColEnh to FALSE. 4. Request all LUNs invalidate page register(s). 5. Wait for an address cycle. 6. Target selects LUN to execute unique ID read, sets tLunSelected to the address of this LUN.

1. Address cycle of 00h received	→	T_RU_ReadUid

T_RU_ReadUid	The target performs the following actions: 1. Request LUN tLunSelected clear SR[6] to zero. 2. R/B_n is cleared to zero. 3. Request LUN tLunSelected make Unique ID data available in page register. 4. tReturnState set to T_RU_ReadUid.

1. LUN tLunSelected indicates data available in page register	→	T_RU_Complete
2. Command cycle 70h (Read Status) received	→	T_RS_Execute
3. Read request received and tbStatusOut set to TRUE	→	T_Idle_Rd_Status

T_RU_Complete	Request LUN tLunSelected set SR[6] to one. R/B_n is set to one.

1. Unconditional	→	T_Idle_Rd

7.1.8. Page Program and Page Cache Program command states

T_PP_Execute	The target performs the following actions: 1. tLastCmd set to 80h. 2. If R/B_n is cleared to zero, then tbStatus78hReq is set to TRUE. 3. If the program page register clear enhancement is not supported or disabled, request all LUNs clear their page register(s).[1]		
	1. Unconditional	→	T_PP_AddrWait
	NOTE: 1. Idle LUNs may choose to not clear their page register if the Program is not addressed to that LUN.		

T_PP_Copyback	If R/B_n is cleared to zero, then tbStatus78hReq is set to TRUE.		
	1. Unconditional	→	T_PP_AddrWait

T_PP_AddrWait	Wait for an address cycle.		
	1. Address cycle received	→	T_PP_Addr

T_PP_Addr	Store the address cycle received.		
	1. More address cycles required	→	T_PP_AddrWait
	2. All address cycles received	→	T_PP_LUN_Execute

T_PP_LUN_Execute	The target performs the following actions: 1. tLunSelected is set to the LUN indicated by the row address received. 2. If the program page register clear enhancement is enabled, request LUN tLunSelected clear the page register for the plane address specified. 3. Target issues the Program with associated address to the LUN tLunSelected.

1. Unconditional	→	T_PP_LUN_DataWait

T_PP_LUN_DataWait	Wait for data byte/word or command cycle to be received from the host.

1. Data byte/word received from the host	→	T_PP_LUN_DataPass
2. Command cycle of 15h received and tCopyback set to FALSE	→	T_PP_Cmd_Pass
3. Command cycle of 10h or 11h received	→	T_PP_Cmd_Pass
4. Command cycle of 85h received	→	T_PP_ColChg

T_PP_LUN_DataPass	Pass data byte/word received from host to LUN tLunSelected

1. Unconditional	→	T_PP_LUN_DataWait

T_PP_Cmd_Pass	Pass command received to LUN tLunSelected

1. Command passed was 11h	→	T_PP_MplWait
2. Command passed was 10h or 15h	→	T_Idle

T_PP_MplWait	Wait for next Program to be issued. tReturnState set to T_PP_MplWait.		
	1. Command cycle of 85h received[1]	→	T_PP_AddrWait
	2. Command cycle of 80h received[2] and tCopyback set to FALSE	→	T_PP_AddrWait
	3. Command cycle of 05h received	→	T_CR_Execute
	4. Command cycle of 06h received	→	T_CRE_Execute
	5. Command cycle of 70h received	→	T_RS_Execute
	6. Command cycle of 78h received	→	T_RSE_Execute
	7. Read request received and tbStatusOut set to TRUE	→	T_Idle_Rd_Status
	NOTE: 1. If the 85h is part of a Copyback, Change Row Address, or Small Data Move operation, then the LUN address and plane address shall be the same as the preceding Program operation. If the 85h is part of a Small Data Move operation, then the page address shall also be the same as the preceding Program operation. 2. Address cycles for the Program operation being issued shall have the same LUN address and page address as the preceding Program operation. The plane address shall be different than the one issued in the preceding Program operation.		

T_PP_ColChg	Wait for column address cycle.		
	1. Address cycle received	→	T_PP_ColChg_Addr

T_PP_ColChg_Addr	Store the address cycle received.		
	1. More column address cycles required	→	T_PP_ColChg
	2. All address cycles received	→	T_PP_ColChg_LUN

T_PP_ColChg_LUN	Request that LUN tLunSelected change column address to column address received.		
	1. Unconditional	→	T_PP_ColChg_Wait

T_PP_ColChg_Wait	Wait for an address cycle, data byte/word, or command cycle to be received from the host		
	1. Address cycle received	→	T_PP_RowChg_Addr
	2. Data byte/word received from the host	→	T_PP_LUN_DataPass
	3. Command cycle of 15h received and tCopyback set to FALSE	→	T_PP_Cmd_Pass
	4. Command cycle of 10h or 11h received	→	T_PP_Cmd_Pass
	5. Command cycle of 85h received	→	T_PP_ColChg

T_PP_RowChg	Wait for row address cycle.		
	1. Address cycle received	→	T_PP_RowChg_Addr

T_PP_RowChg_Addr	Store the address cycle received.		
1. More row address cycles required		→	T_PP_RowChg
2. All address cycles received		→	T_PP_RowChg_LUN

T_PP_RowChg_LUN	Request that LUN tLunSelected change row address to row address received.[1]		
1. Unconditional		→	T_PP_LUN_DataWait
NOTE: 1. The LUN address and plane address shall be the same as previously specified for the Program operation executing.			

T_PP_WaitForDataOut	Wait for read request (data or status) or other action. tReturnState set to T_PP_WaitForDataOut.		
1. Read request received and tbStatusOut set to TRUE		→	T_Idle_Rd_Status
2. Read request received and tbStatus78hReq set to FALSE[1]		→	T_Idle_Rd_LunData
3. Command cycle of 70h received		→	T_RS_Execute
4. Command cycle of 78h received		→	T_RSE_Execute
5. Command cycle of 00h received		→	T_RD_Execute
6. Command cycle received		→	T_PP_MplWait
NOTE: 1. When tbStatus78hReq is set to TRUE, a Read Status Enhanced (78h) command followed by a 00h command shall be issued by the host prior to reading data from a particular LUN. (NOTE: Some NAND vendors may require the use of Change Read Column sequence instead of 00h command to output data from the NAND, see vendor datasheet)			

7.1.9. Block Erase command states

T_BE_Execute	The target performs the following actions: 1. tLastCmd set to 60h. 2. If R/B_n is cleared to zero, then tbStatus78hReq is set to TRUE. 3. Wait for a row address cycle.		
1. Address cycle received		→	T_BE_Addr

T_BE_Addr	Store the row address cycle received.		
1. More address cycles required		→	T_BE_Execute
2. All address cycles received		→	T_BE_LUN_Execute

T_BE_LUN_Execute	tLunSelected is set to the LUN indicated by the row address received. Target issues the Erase with associated row address to the LUN tLunSelected.		
	1. Unconditional	→	T_BE_LUN_Confirm

T_BE_LUN_Confirm	Wait for D0h or D1h command cycle.		
	1. Command cycle of D0h or D1h received	→	T_BE_Cmd_Pass

T_BE_Cmd_Pass	Pass command received to LUN tLunSelected		
	1. Command passed was D1h	→	T_BE_MplWait
	2. Command passed was D0h	→	T_Idle

T_BE_MplWait	Wait for next Erase to be issued. tReturnState set to T_BE_MplWait.		
	1. Command cycle of 60h received	→	T_BE_Execute
	2. Command cycle of 70h received	→	T_RS_Execute
	3. Command cycle of 78h received	→	T_RSE_Execute
	4. Read request received and tbStatusOut set to TRUE	→	T_Idle_Rd_Status

7.1.10. Read command states

T_RD_Execute			
1. tbStatusOut set to TRUE		→	T_RD_StatusOff
2. Else		→	T_RD_AddrWait

T_RD_StatusOff	tbStatusOut set to FALSE. tReturnState set to T_RD_StatusOff.		
1. Address cycle received		→	T_RD_Addr
2. Read request received and tLastCmd set to 80h		→	T_PP_WaitForDataOut
3. Read request received and tLastCmd set to EEh		→	T_Idle_Rd_XferHost
4. Read request received		→	T_Idle_Rd_LunData
5. Command cycle of 05h received		→	T_CR_Execute
6. Command cycle of 06h received		→	T_CRE_Execute

T_RD_AddrWait	tLastCmd set to 00h. Set tbChgCol to TRUE. Set tbChgColEnh to TRUE. If R/B_n is cleared to zero, then tbStatus78hReq is set to TRUE. Wait for an address cycle.		
1. Address cycle received		→	T_RD_Addr

T_RD_Addr	Store the address cycle received.		
3. More address cycles required		→	T_RD_AddrWait
4. All address cycles received		→	T_RD_LUN_Execute

T_RD_LUN_Execute	The target performs the following actions: 1. tLunSelected is set to the LUN indicated by the row address received. 2. Issues the Read Page with address to LUN tLunSelected. 3. Requests all idle LUNs not selected to turn off their output buffers.[1]		
1. Unconditional		→	T_RD_LUN_Confirm
NOTE: 1. LUNs not selected will only turn off their output buffers if they are in an Idle state. If other LUNs are active, the host shall issue a Read Status Enhanced (78h) command to ensure all LUNs that are not selected turn off their output buffers prior to issuing the Read (00h) command. (NOTE: Some NAND vendors may require the use of Change Read Column sequence instead of 00h command to output data from the NAND, see vendor datasheet)			

T_RD_LUN_Confirm	Wait for 30h, 31h, 32h, or 35h to be received.		
1. Command cycle of 30h, 31h, 32h, or 35h received		→	T_RD_Cmd_Pass

T_RD_Cmd_Pass	Pass command received to LUN tLunSelected		
1. Command passed was 35h		→	T_RD_Copyback

2. Command passed was 30h, 31h, or 32h	→	T_Idle_Rd

T_RD_Copyback	tCopyback set to TRUE. tReturnState set to T_RD_Copyback.	
1. Command cycle of 00h received	→	T_RD_Execute
2. Command cycle of 05h received	→	T_CR_Execute
3. Command cycle of 06h received	→	T_CRE_Execute
4. Command cycle of 85h received	→	T_PP_Copyback
5. Command cycle of 70h received	→	T_RS_Execute
6. Command cycle of 78h received	→	T_RSE_Execute
7. LUN indicates its SR[6] value transitions	→	T_Idle_RB_Transition
8. Read request received and tbStatusOut set to TRUE	→	T_Idle_Rd_Status
9. Read request received	→	T_Idle_Rd_LunData

7.1.11. Set Features command states

T_SF_Execute	The target performs the following actions: 1. tLastCmd set to EFh. 2. Request all LUNs invalidate page register(s). 3. Wait for an address cycle.		
1. Address cycle received		→	T_SF_Addr

T_SF_Addr	Store the feature address received.		
1. Unconditional		→	T_SF_WaitForParams

T_SF_WaitForParams	Wait for data byte to be received.		
1. Data byte written to target		→	T_SF_StoreParam

T_SF_StoreParam	Store parameter received.		
1. More parameters required		→	T_SF_WaitForParams
2. All parameters received		→	T_SF_Complete

T_SF_Complete	The target performs the following actions: 1. Request LUN tLunSelected clear SR[6] to zero. 2. R/B_n is cleared to zero. 3. Finish Set Features command. 4. tReturnState set to T_SF_Complete.		
1. Set Features command complete		→	T_SF_UpdateStatus
2. Command cycle 70h (Read Status) received		→	T_RS_Execute
3. Read request received and tbStatusOut set to TRUE		→	T_Idle_Rd_Status

T_SF_UpdateStatus	The target performs the following actions: 1. Request LUN tLunSelected set SR[6] to one. 2. R/B_n is set to one.		
1. tbStatusOut is set to FALSE		→	T_Idle
2. tbStatusOut is set to TRUE		→	T_Idle_Rd

7.1.12. Get Features command states

T_GF_Execute	The target performs the following actions: 1. tLastCmd set to EEh. 2. Request all LUNs invalidate page register(s). 3. Set tbChgCol to FALSE. 4. Set tbChgColEnh to FALSE. 5. Wait for an address cycle.		
1. Address cycle received		→	T_GF_Addr

T_GF_Addr	Store the feature address received.		
1. Unconditional		→	T_GF_RetrieveParams

T_GF_RetrieveParams	The target performs the following actions: 1. Request LUN tLunSelected clear SR[6] to zero. 2. R/B_n is cleared to zero. 3. Retrieve parameters. 4. tReturnState set to T_GF_RetrieveParams.		
1. Parameters are ready to be transferred to the host		→	T_GF_Ready
2. Command cycle 70h (Read Status) received		→	T_RS_Execute
3. Read request received and tbStatusOut set to TRUE		→	T_Idle_Rd_Status

T_GF_Ready	Request LUN tLunSelected set SR[6] to one. R/B_n is set to one.		
1. Unconditional		→	T_Idle_Rd

7.1.13. Read Status command states

T_RS_Execute			
1. tbStatus78hReq is set to FALSE[1]		→	T_RS_Perform
NOTE: 1. When tbStatus78hReq is set to TRUE, issuing a Read Status (70h) command is illegal.			

T_RS_Perform	The target performs the following actions: 1. tbStatusOut is set to TRUE. 2. Indicate 70h command received to LUN tLunSelected.		
1. tReturnState set to T_Idle		→	T_Idle_Rd
2. Else		→	tReturnState

7.1.14. Read Status Enhanced command states

T_RSE_Execute[1]	tbStatus78hReq is set to FALSE. tbStatusOut is set to TRUE. Wait for a row address cycle.		
	1. Row address cycle received	→	T_RSE_Addr
	NOTE: 1. The host should not issue Read Status Enhanced following a Target level command (Reset, Read ID, Read Parameter Page, Read Unique ID, Set Features, Get Features). The status value read from the LUN selected with Read Status Enhanced may not correspond with the LUN selected during the Target level command.		

T_RSE_Addr	Store the row address cycle received.	
1. More row address cycles required	→	T_RSE_Execute
2. All row address cycles received	→	T_RSE_Select

T_RSE_Select	The target performs the following actions: 1. Set tLunSelected to LUN selected by row address received. 2. Indicate 78h command and row address received to all LUNs.	
1. tReturnState set to T_Idle	→	T_Idle_Rd
2. Else	→	tReturnState

7.1.15. Volume Select command states

T_VS_Execute	The target performs the following actions: 1. tLastCmd set to E1h. 2. Wait for an address cycle.	
1. Address cycle received	→	T_VS_Complete

T_VS_Complete	Indicate to all LUNs the Volume Address received.	
1. Unconditional	→	T_Idle

7.1.16. ODT Configure command states

T_ODTC_Execute	The target performs the following actions: 1. tLastCmd set to E2h. 2. Wait for an address cycle.		
1. Address cycle received		→	T_ODTC_Addr

T_ODTC_Addr	Store the LUN received; apply subsequent matrix and Rtt settings to the LUN indicated.		
1. Unconditional		→	T_ODTC_WaitForParam

T_ODTC_WaitForParam	Wait for data byte to be received.		
1. Data byte written to Target		→	T_ODTC_StoreParam

T_ODTC_StoreParam	Store matrix (byte 0/1) or Rtt (byte 2/3) parameter received.		
1. More parameters required		→	T_ODTC_WaitForParam
2. All parameters received		→	T_ODTC_Complete

T_ODTC_Complete	Indicate to the LUN specified the ODT Configuration parameters (M0, M1, Rtt1, Rtt2).		
1. Unconditional		→	T_Idle

7.2. LUN behavioral flows

The LUN state machine describes the allowed sequences when operating with the LUN. If none of the arcs are true, then the LUN remains in the current state.

7.2.1. Variables

This section describes variables used within the LUN state machine.

lunStatus	This variable contains the current LUN status register value contents. The power on value for this variable is 00h.
lunFail[]	This array contains the FAIL and FAILC bits for each interleave address. For example, lunFail[3][1] contains the FAILC bit for plane address 3. The power on value for each variable in this array is 00b.
lunLastConfirm	This variable contains the last confirm command cycle (30h, 31h, 32h, 35h, 10h, 15h, 11h, D0h, D1h). The power on value for this variable is FFh.
lunOutputMpl	This variable contains the plane address requested for data output. The power on value for this variable is 0h.
lunReturnState	This variable contains the state to return to after status operations. The power on value for this variable is L_Idle.
lunStatusCmd	This variable contains the last status command received. The power on value for this variable is 70h.
lunStatusMpl	This variable contains the plane address indicated in a previous 78h command. The power on value for this variable is 0h.
lunbInterleave	This variable is set to one when the LUN is performing a multi-plane operation. The power on value for this variable is FALSE.
lunbMplNextCmd	This variable is set to TRUE when the LUN is ready to receive the next multi-plane command.
lunEraseAddr[]	This variable contains the block addresses of erases that have been suspended.

7.2.2. Idle command states

L_Idle[1]	lunReturnState is set to L_Idle.		
	1. Target request received	→	L_Idle_TargetRequest
	NOTE: 1. This state is entered as a result of a power-on event when Vcc reaches Vcc_min.		

L_Idle_TargetRequest	If Target indicates an address, the address is stored by the LUN.		
	1. Target requests LUN perform a Reset	→	L_RST_Execute
	2. Target indicates WP_n value	→	L_WP_Update
	3. Target requests SR register update	→	L_SR_Update
	4. Target requests status or status command received	→	L_Status_Execute
	5. Target indicates plane address for use in data output	→	L_Idle_Mpl_DataOutAddr
	6. Target indicates output buffer should be turned off	→	L_Idle
	7. Target requests page register clear	→	L_Idle_ClearPageReg
	8. Target requests page register invalidate	→	L_Idle_InvalidPageReg
	9. Target indicates Program request for this LUN	→	L_PP_Execute
	10. Target indicates Erase request for this LUN	→	L_BE_Execute
	11. Target indicates Erase Resume request for this LUN	→	L_ER_Execute
	12. Target indicates Read Page request for this LUN	→	L_RD_Addr
	13. Target indicates Read Parameter Page request	→	L_Idle_RdPp
	14. Target indicates Read Unique ID request	→	L_Idle_RdUid
	15. Target indicates Volume Address received	→	L_Idle_VolAddr
	16. Target indicates ODT Configuration settings received	→	L_Idle_ODTConfig

L_WP_Update	Set lunStatus[7] to the WP_n value indicated by the target.		
	1. Unconditional	→	lunReturnState

L_SR_Update	Update lunStatus as indicated by the target.		
	1. Unconditional	→	lunReturnState

L_Idle_Mpl_DataOutAddr	Set lunOutputMpl to plane address indicated by the target.		
	1. Unconditional	→	lunReturnState

L_Idle_ClearPageReg	Set page register to all ones value.		
	1. Unconditional	→	lunReturnState

L_Idle_InvalidPageReg	Invalidate page register.		
	1. Unconditional	→	lunReturnState

L_Idle_RdPp	The LUN performs the following actions: 1. LUN reads parameter page data into the page register. 2. lunReturnState set to L_Idle_RdPp_Cont.		
	1. Parameter page data transferred to page register	→	L_Idle_RdPp_End
	2. Target requests status or status command received	→	L_Status_Execute

L_Idle_RdPp_Cont			
1. Parameter page data transferred to page register		→	L_Idle_RdPp_End
2. Target requests status or status command received		→	L_Status_Execute

L_Idle_RdPp_End	LUN indicates to Target that parameter page data is in page register.		
1. Unconditional		→	L_Idle_Rd

L_Idle_RdUid	The LUN performs the following actions: 1. LUN reads Unique ID data into the page register. 2. lunReturnState set to L_Idle_RdUid.		
1. Unique ID data transferred to page register		→	L_Idle_RdUid_End
2. Target requests status or status command received		→	L_Status_Execute

L_Idle_RdUid_End	LUN indicates to Target that Unique ID data is in page register.		
1. Unconditional		→	L_Idle_Rd

7.2.3. Idle Read states

L_Idle_Rd	lunReturnState is set to L_Idle_Rd.		
1. Background read operation complete		→	L_Idle_Rd_Finish
2. Target requests column address be selected		→	L_Idle_Rd_ColSelect
3. Read request received from Target		→	L_Idle_Rd_Xfer
4. Command cycle 31h (Read Cache Sequential) received		→	L_RD_Cache_Next
5. Command cycle 3Fh (Read Cache End) received and lunLastConfirm is 31h		→	L_RD_Cache_Xfer_End
6. Target request received		→	L_Idle_TargetRequest

L_Idle_Rd_Finish	Set lunStatus[5] to one.		
1. Unconditional		→	L_Idle_Rd

L_Idle_Rd_Xfer	Return to the target the next byte (x8) or word (x16) of data from page register based on Target requested. Increments column address.		
1. lunReturnState set to L_PP_Mpl_Wait		→	L_PP_Mpl_Wait
2. Unconditional		→	L_Idle_Rd

L_Idle_Rd_ColSelect	Select the column in the page register based on the column address received from the target.		
1. lunReturnState set to L_PP_Mpl_Wait		→	L_PP_Mpl_Wait
2. Unconditional		→	L_Idle_Rd

L_Idle_VolAddr			
1. Volume address matches the NAND Target this LUN is part of (LUN remains selected)		→	L_Idle
2. LUN is a terminator for the specified Volume address		→	L_Idle_VolSniff
3. Volume address does not match the NAND Target this LUN is part of		→	L_Idle_VolDeselect
4. Unconditional		→	L_Idle
NOTE: 1. Refer to the ODT Behavioral Flows in Figure 4-17, Figure 4-18 and Figure 4-19 for more detailed requirements.			

L_Idle_VolSniff	The LUN enters the Sniff state.		
1. Unconditional		→	L_Idle

L_Idle_VolDeselect	The LUN is deselected.		
1. Unconditional		→	L_Idle

L_Idle_ODTConfig	The LUN stores/applies the ODT matrix and Rtt settings specified.		
1. Unconditional		→	L_Idle

7.2.4. Status states

L_Status_Execute			
1. Target requests status value		→	L_Status_Value
2. Target indicates 78h was received		→	L_Status_Enhanced
3. Target indicates 70h was received		→	L_Status_Legacy

L_Status_Value			
1. lunbInterleave set to TRUE and lunStatusCmd set to 70h		→	L_Status_Mpl_Comp
2. lunbInterleave set to TRUE and lunStatusCmd set to 78h		→	L_Status_Mpl_Addr
3. lunbInterleave set to FALSE		→	L_Status_Lun

L_Status_Enhanced			
1. LUN in row address indicated matches this LUN		→	L_Status_Record_78h
2. Else		→	L_Status_Output_Off

L_Status_Record_78h	lunStatusCmd is set to 78h and lunStatusMpl is set to plane address indicated by Target. The LUN turns on its output buffer.

1. lunReturnState set to L_Idle and (lunLastConfirm set to 30h, 31h, 32h, or 35h)	→	L_Idle_Rd
2. Else	→	lunReturnState

L_Status_Output_Off	LUN turns off its output buffer.		
1. lunReturnState set to L_Idle_Rd		→	L_Idle
2. Else		→	lunReturnState

L_Status_Legacy	lunStatusCmd is set to 70h.		
1. Unconditional		→	lunReturnState

L_Status_Mpl_Comp	The LUN composes the status value to return as shown: • status[7:2] = lunStatus[7:2] • status[1] = for all x, OR of lunFail[x][1] • status[0] = for all x, OR of lunFail[x][0] Return status to the Target.		
1. Unconditional		→	lunReturnState

L_Status_Mpl_Addr	The LUN composes the status value to return as shown: • status[7:2] = lunStatus[7:2] • status[1:0] = lunFail[lunStatusMpl][1:0] Return status to the Target.		
1. Unconditional		→	lunReturnState

L_Status_Lun	Return lunStatus to the Target.		
1. Unconditional		→	lunReturnState

7.2.5. Reset states

L_RST_Execute[1]	The LUN performs the following actions: 1. lunStatus[6] is cleared to zero. 2. lunStatus[6] value is indicated to the Target. 3. Perform reset of the LUN. 4. lunbInterleave is set to FALSE. 5. lunReturnState is set to L_RST_Execute.		
1. Reset of the LUN is complete		→	L_RST_Complete
2. Target requests status or status command received		→	L_Status_Execute
NOTE: 1. This state is entered as a result of receiving an indication from the Target state machine to perform a Reset in any other state.			

L_RST_Complete	The LUN performs the following actions: 1. lunStatus[1:0] are cleared to 00b. 2. For all plane addresses x, clear lunFail[x][1:0] to 00b. 3. lunStatus[6] is set to one. 4. lunStatus[6] value is indicated to the Target. 5. Indicate to the Target state machine that Reset for this LUN is complete.

1.	Unconditional	→	L_Idle

7.2.6. Block Erase command states

L_BE_Execute	lunbInterleave set to FALSE.

1.	Unconditional	→	L_BE_WaitForCmd

L_BE_WaitForCmd	Wait for a command cycle.

1.	Command cycle D0h received	→	L_BE_Erase
2.	Command cycle D1h received	→	L_BE_Mpl

L_BE_Erase	The LUN performs the following actions: 1. lunStatus[6] is cleared to zero. 2. If lunbInterleave is TRUE, lunStatus[5] is cleared to zero. 3. lunStatus[6] value is indicated to the Target. 4. lunLastConfirm set to D0h. 5. Erase the requested block and any previously requested blocks if lunbInterleave is set to TRUE and concurrent interleaving is supported.

1.	Unconditional	→	L_BE_Erase_Wait

L_BE_Erase_Wait	lunReturnState set to L_BE_Erase_Wait.

1.	Erase of requested block(s) complete and lunbInterleave set to TRUE	→	L_BE_Mpl_Sts
2.	Erase of requested block complete	→	L_BE_Sts
3.	Target requests page register clear	→	L_Idle_ClearPageReg
4.	Target requests status or status command received	→	L_Status_Execute

L_BE_Mpl	The LUN performs the following actions in the order specified: 1. lunbInterleave set to TRUE. 2. lunLastConfirm set to D1h. 3. lunStatus[6:5] is cleared to 00b. lunStatus[6] value is indicated to the Target. 4. LUN begins erasing block specified if overlapped is supported. 5. lunbMplNextCmd is set to FALSE. 6. LUN prepares to receive the next block to erase.

1. Unconditional	→	L_BE_Mpl_Wait

L_BE_Mpl_Wait	lunReturnState set to L_BE_Mpl_Wait.		
	1. An overlapped multi-plane Erase completed	→	L_BE_Mpl_Overlap
	2. Ready to receive the next Erase command and lunbMplNextCmd is set to FALSE	→	L_BE_Mpl_NextCmd
	3. Target indicates Erase request for this LUN and lunbMplNextCmd is set to TRUE	→	L_BE_WaitForCmd
	4. Target requests status or status command received	→	L_Status_Execute

L_BE_Mpl_NextCmd	The LUN performs the following actions in the order specified: 1. lunbMplNextCmd is set to TRUE. 2. If no array operations are in progress, lunStatus[5] is set to one. 3. lunStatus[6] is set to one. lunStatus[6] value is indicated to the Target.		
	1. Unconditional	→	L_BE_Mpl_Wait

L_BE_Mpl_Overlap	The LUN performs the following actions in the order specified for the overlapped multi-plane operation that completed: 1. mplComplete set to plane address of completed operation 2. lunFail[mplComplete][0] is set to program status of operation. If all array operations are complete, lunStatus[5] is set to one.		
	1. Unconditional	→	lunReturnState

L_BE_Sts	The LUN performs the following actions in the order specified: 1. lunStatus[0] is set to erase status. 2. lunStatus[6] is set to one. lunStatus[6] value is indicated to the Target.		
	1. Unconditional	→	L_Idle

L_BE_Mpl_Sts	The LUN performs the following actions in the order specified for each multi-plane operation that completed: 1. mplComplete set to interleave address of completed operation. 2. lunFail[mplComplete][0] is set to erase status value. lunStatus[6:5] is set to 11b and lunStatus[6] value is indicated to the Target.		
	1. Unconditional	→	L_Idle

7.2.7. Read command states

If caching is not supported, then all actions for status bit 5 are ignored.

L_RD_Addr	The LUN performs the following actions in the order specified: 1. Records address received from the target.

	2. If multi-plane addressing is supported, selects the correct page register based on the plane address. 3. Selects the column in the page register based on the column address received.		
1. Unconditional		→	L_RD_WaitForCmd

L_RD_WaitForCmd	lunbInterleave set to FALSE. Wait for a command cycle.		
1. Command cycle 30h or 35h received		→	L_RD_ArrayRead
2. Command cycle 31h received and lunLastConfirm equal to 30h or 31h		→	L_RD_Cache_Xfer
3. Command cycle 32h received		→	L_RD_Mpl_Xfer

L_RD_ArrayRead	The LUN performs the following actions: 1. lunStatus[6:5] is cleared to 00b. 2. lunStatus[6] value is indicated to the target. 3. lunLastConfirm set to last command cycle (30h or 35h). 4. Read the requested page from the array. If concurrent multi-plane operation, read all pages requested from the array. 5. lunReturnState set to L_RD_ArrayRead_Cont.		
1. Read of requested page(s) complete		→	L_RD_Complete
2. Target requests status or status command received		→	L_Status_Execute

L_RD_ArrayRead_Cont			
1. Read of requested page(s) complete		→	L_RD_Complete
2. Target requests status or status command received		→	L_Status_Execute

L_RD_Complete	lunStatus[6:5] is set to 11b. lunStatus[6] value is indicated to the target.		
1. Unconditional		→	L_Idle_Rd

L_RD_Cache_Next	Select the next row address as the sequential increasing row address to the last page read.		
1. Unconditional		→	L_RD_Cache_Xfer

L_RD_Cache_Xfer	The LUN performs the following actions: 1. lunStatus[6:5] is cleared to 00b. lunStatus[6] value is indicated to the Target. 2. lunLastConfirm set to 31h. 3. Begin background read operation for selected address. 4. lunReturnState set to L_RD_Cache_Xfer.		
1. Data available in page register for previous read operation		→	L_RD_Cache_Sts
2. Target requests status or status command received		→	L_Status_Execute

L_RD_Cache_Xfer_End	The LUN performs the following actions: 1. lunStatus[6] is cleared to zero. 2. lunStatus[6] value is indicated to the target. 3. lunLastConfirm set to 3Fh. 4. lunReturnState set to L_RD_Cache_Xfer_End.		
1. Data available in page register for previous read operation		→	L_RD_Cache_Sts_End
2. Target requests status or status command received		→	L_Status_Execute

L_RD_Cache_Sts	lunStatus[6] is set to one. lunStatus[6] value is indicated to the Target.		
1. Unconditional		→	L_Idle_Rd

L_RD_Cache_Sts_End	lunStatus[6:5] is set to 11b. lunStatus[6] value is indicated to the Target.		
1. Unconditional		→	L_Idle_Rd

L_RD_Mpl_Xfer	The LUN performs the following actions: 1. lunStatus[6:5] is cleared to 00b. 2. lunStatus[6] value is indicated to the target. 3. lunLastConfirm set to 32h. 4. lunbMplNextCmd is set to FALSE. 5. LUN begins reading page specified if overlapped interleaving is supported. 6. Prepare to receive the next page to read. 7. lunReturnState set to L_RD_Mpl_Xfer.		
1. Target ready to receive next page to read		→	L_RD_Mpl_Wait
2. Target requests status or status command received		→	L_Status_Execute

L_RD_Mpl_Wait	lunStatus[6] is set to one. lunStatus[6] value is indicated to the Target. lunReturnState set to L_RD_Mpl_Wait.		
1. An overlapped multi-plane Read completed		→	L_RD_Mpl_Overlap
2. Target indicates Read Page request for this LUN		→	L_RD_Addr
3. Target requests status or status command received		→	L_Status_Execute

L_RD_Mpl_Overlap	The LUN performs the following actions in the order specified for the overlapped multi-plane operation that completed: 1. mplComplete set to plane address of completed operation. If all array operations are complete, lunStatus[5] is set to one.		
	1. Unconditional	→	lunReturnState

7.2.8. Page Program and Page Cache Program command states

If caching or overlapped interleaving is not supported, then all actions for status bit 5 are ignored.
If caching is not supported, then all actions for status bit 1 are ignored.

L_PP_Execute	lunbInterleave set to FALSE.		
	1. Unconditional	→	L_PP_Addr

L_PP_Addr	The LUN performs the following actions in the order specified: 1. Records address received from the Target. 2. If multi-plane addressing is supported, selects the correct page register based on the plane address. 3. Selects the column in the page register based on the column address received.		
	1. Unconditional	→	L_PP_WaitForData

L_PP_WaitForData	Wait for data to be received. lunReturnState is set to L_PP_WaitForData.		
	1. Target passes data byte or word to LUN	→	L_PP_AcceptData
	2. Command cycle 10h (program execute) received	→	L_PP_Prog
	3. Command cycle 15h (cache program) received	→	L_PP_Cache
	4. Command cycle 11h (interleave) received	→	L_PP_Mpl
	5. Target requests column address be selected	→	L_PP_ColSelect
	6. Target requests row address be selected	→	L_PP_RowSelect

L_PP_AcceptData	Write the byte (x8) or word (x16) of data into the selected column address in the page register. Increments column address.		
	1. Unconditional	→	L_PP_WaitForData

L_PP_Prog	The LUN performs the following actions in the order specified: 1. lunStatus[6:5] is cleared to 00h. lunStatus[6] value is indicated to the Target. 2. lunLastConfirm set to 10h. 3. If only one page is specified to be programmed, clear lunbInterleave to FALSE. 4. LUN begins programming page specified and any previous pages specified if lunbInterleave is TRUE and concurrent interleaving is supported.

1. Unconditional	→	L_PP_Prog_Wait

L_PP_Prog_Wait	lunReturnState set to L_PP_Prog_Wait.	
1. Write of all requested pages are complete and lunbInterleave is set to TRUE	→	L_PP_Mpl_Sts
2. Write of requested page is complete and lunbInterleave is cleared to FALSE	→	L_PP_Sts
3. Target requests status or status command received	→	L_Status_Execute

L_PP_Cache	The LUN performs the following actions in the order specified: 1. lunStatus[6:5] is cleared to 00b. lunStatus[6] value is indicated to the Target. 2. lunLastConfirm set to 15h. 3. Wait for the page register to become available for data input. 4. Start background program operation.	
1. Unconditional	→	L_PP_Cache_Wait

L_PP_Cache_Wait	lunReturnState is set to L_PP_Cache_Wait.	
1. Page register available for data input	→	L_PP_CacheRdy
2. Target requests status or status command received	→	L_Status_Execute

L_PP_CacheRdy	The LUN performs the following actions: 1. If lunbInterleave is set to FALSE, then lunStatus[1] is set to the value of lunStatus[0]. 2. If lunbInterleave is set to TRUE, then for all multi-plane addresses, x, lunFail[x][1] is set to the value of lunFail[x][0]. 3. lunStatus[6] is set to one. lunStatus[6] value is indicated to the Target.	
1. Unconditional	→	L_PP_CacheRdy_Wait

L_PP_CacheRdy_Wait	lunReturnState set to L_PP_CacheRdy_Wait.	
1. Previous cache operation complete and lunbInterleave set to TRUE	→	L_PP_Mpl_Cache_Sts
2. Previous cache operation complete	→	L_PP_Cache_Sts
3. Target indicates Program request for this LUN	→	L_PP_Addr
4. Target requests page register clear	→	L_Idle_ClearPageReg
5. Target requests status or status command received	→	L_Status_Execute

L_PP_Mpl	The LUN performs the following actions in the order specified: 1. lunbInterleave set to TRUE. 2. lunStatus[6:5] is cleared to 00b. lunStatus[6] value is indicated to the Target. 3. lunLastConfirm set to 11h. 4. lunbMplNextCmd is set to FALSE.

	5. LUN begins programming page specified if overlapped interleaving is supported.		
1. Unconditional		→	L_PP_Mpl_Wait

L_PP_Mpl_Wait	lunReturnState set to L_PP_Mpl_Wait.		
1. An overlapped multi-plane Program completed		→	L_PP_Mpl_Overlap
2. A previous cache Program completed		→	L_PP_Mpl_Cache_Sts
3. LUN is ready to receive the next Program command and lunbMplNextCmd is set to FALSE		→	L_PP_Mpl_NextCmd
4. Target indicates Program request for this LUN and lunbMplNextCmd is set to TRUE		→	L_PP_Addr
5. Target requests column address be selected		→	L_Idle_Rd_ColSelect
6. Target indicates plane address for use in data output		→	L_Idle_Mpl_DataOutAddr
7. Target requests status or status command received		→	L_Status_Execute
8. Read request received from Target		→	L_Idle_Rd_Xfer

L_PP_Mpl_NextCmd	The LUN performs the following actions in the order specified: 1. lunbMplNextCmd is set to TRUE. 2. If no array operations are in progress, lunStatus[5] is set to one. 3. lunStatus[6] is set to one. lunStatus[6] value is indicated to the Target.		
1. Unconditional		→	L_PP_Mpl_Wait

L_PP_Sts	The LUN performs the following actions in the order specified: 1. lunStatus[1] is set to program status of previous operation 2. lunStatus[0] is set to program status of final operation 3. lunStatus[6:5] is set to 11b. 4. lunStatus[6] value is indicated to the Target.		
1. Unconditional		→	L_Idle

L_PP_Cache_Sts	The LUN performs the following actions in the order specified: 1. lunStatus[0] is set to program status. 2. lunStatus[5] is set to one.		
1. Unconditional		→	lunReturnState

L_PP_Mpl_Cache_Sts	The LUN performs the following actions in the order specified for all completed cache operations: 1. mplAddr set to interleave address of cache operation. 2. lunFail[mplAddr][0] is set to program status. If all array operations are complete, lunStatus[5] is set to one.		
1. Unconditional		→	lunReturnState

L_PP_Mpl_Overlap	The LUN performs the following actions in the order specified for the overlapped multi-plane operation that completed:

	1. mplComplete set to interleave address of completed operation 2. lunFail[mplComplete][0] is set to program status of operation. If all array operations are complete, lunStatus[5] is set to one.

1. Unconditional	→	lunReturnState

L_PP_Mpl_Sts	The LUN performs the following actions in the order specified for each multi-plane operation that completed: 1. mplComplete set to plane address of completed operation 2. lunFail[mplComplete][1] is set to program status of previous operation. 3. lunFail[mplComplete][0] is set to program status of final operation. lunStatus[6:5] is set to 11b and lunStatus[6] value is indicated to the Target.

1. Unconditional	→	L_Idle

L_PP_ColSelect	Select the column in the page register based on the column address received that the target requested.

1. Unconditional	→	L_PP_WaitForData

L_PP_RowSelect	Select the block and page to program based on the row address received from the target.

1. Unconditional	→	L_PP_WaitForData

A. SAMPLE CODE FOR CRC-16 (INFORMATIVE)

This section provides an informative implementation of the CRC-16 polynomial. The example is intended as an aid in verifying an implementation of the algorithm.

```
int main(int argc, char* argv[])
{
      // Bit by bit algorithm without augmented zero bytes
  const unsigned long crcinit = 0x4F4E; // Initial CRC value in the shift register
  const int order = 16;          // Order of the CRC-16
  const unsigned long polynom = 0x8005; // Polynomial
  unsigned long i, j, c, bit;
  unsigned long crc = crcinit;        // Initialize the shift register with 0x4F4E
  unsigned long data_in;
  int dataByteCount = 0;
  unsigned long crcmask, crchighbit;
  crcmask = ((((unsigned long)1<<(order-1))-1)<<1)|1;
  crchighbit = (unsigned long)1<<(order-1);

  // Input byte stream, one byte at a time, bits processed from MSB to LSB
  printf("Input byte value in hex(eg. 0x30):");
  printf("\n");
```

```
      while(scanf("%x", &data_in) == 1)
  {
    c = (unsigned long)data_in;
    dataByteCount++;
    for (j=0x80; j; j>>=1) {
      bit = crc & crchighbit;
      crc<<= 1;
      if (c & j) bit^= crchighbit;
      if (bit) crc^= polynom;
    }
    crc&= crcmask;
    printf("CRC-16 value: 0x%x\n", crc);
  }
  printf("Final CRC-16 value: 0x%x, total data bytes: %d\n", crc, dataByteCount);

      return 0;
}
```

B. SPARE SIZE RECOMMENDATIONS (INFORMATIVE)

This appendix describes recommendations for the spare bytes per page based on the ECC requirements reported in the parameter page. Table 7-1 lists recommendations for 2KB, 4KB, and 8KB page size devices.

Page Size	Number of bits ECC correctability	Spare Bytes Per Page Recommendation
2048 bytes	≤ 8 bits	64 bytes
2048 bytes	> 8 bits	112 bytes
4096 bytes	≤ 8 bits	128 bytes
4096 bytes	> 8 bits	218 or 224 bytes
8192 bytes	≤ 8 bits	256 bytes
8192 bytes[2]	> 8 bits	448 bytes

NOTE:

- The number of bits ECC correctability is based on a 512 byte codeword size.
- If more correction is required than spare area size allows for with a 512 byte codeword size, it is recommended that the host use a larger ECC codeword size (e.g. 1KB, 2KB, etc). The device manufacturer may provide guidance on the ECC codeword size to use in the extended parameter page.

Table 7-1 Spare Area Size Recommendations for raw NAND

The host transfers bytes from the page register in discrete units that include data, metadata, and the ECC check bytes. This discrete unit is recommended to be an even number of bytes for devices that support the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface.

As an example, assume the page size is 8192 bytes and the ECC codeword size used is 1KB. Then 1024 bytes of data will be transferred in each discrete unit, resulting in eight discrete units of data being transferred for this page. The spare bytes for this page should be allocated to allow enough storage for the metadata and check bytes, and should also be an even number when divided by eight (i.e. the number of discrete units contained in that page).

C. DEVICE SELF-INITIALIZATION WITH PSL (INFORMATIVE)

Some devices store configuration information for the Flash array within the Flash array itself. The device loads this information either at power-on or during the first Reset after power-on.

Vendors may choose to support PSL as one of the vendor specific pins. If PSL is supported, then it shall have the following behavior:

- PSL = 0 V: Configuration information is loaded at power-on. The IST current may be up to 15 mA and the time for R/B_n to become one is up to 5 ms.
- PSL = Vcc or not connected: Configuration information if supported is loaded during the first Reset after power-on. There is no change to the IST current requirement. This corresponds to the normally expected ONFI device operation.

If PSL is not supported by the device, then the IST requirement shall be met.

Refer to the device vendor’s datasheet to determine if self-initialization at power-on is supported.

D. ICC MEASUREMENT METHODOLOGY

This section defines the technique used to measure the ICC parameters defined in section 2.13.

The common testing conditions that shall be used to measure the DC and Operating Conditions are defined in Table 7-2. The testing conditions that shall be used to measure the DC and Operating Conditions that are data interface specific are defined in Table 7-3.

Parameter	Testing Condition
General conditions	1. Vcc = Vcc(min) to Vcc(max) 2. VccQ = VccQ(min) to VccQ(max) 3. CE_n = 0 V 4. WP_n = VccQ 5. IOUT = 0 mA 6. Measured across operating temperature range 7. N data input or data output cycles, where N is the number of bytes or words in the page 8. No multi-plane operations. 9. Sample a sufficient number of times to remove measurement variability. 10. Sample an equal ratio of page types that exist in a block. A page type is a group of page addresses and is commonly referred to as upper or lower page (or middle page for 3 bits per cell devices). 11. Choose the first good even/odd block pair beginning at blocks 2-3
Array preconditioning for ICC1, ICC2, and ICC3	The array is preconditioned with vendor required random data pattern.
Fixed wait time (no R/B_n polling)	ICC1: tR = tR(max) ICC2: tPROG = tPROG(max) ICC3: tBERS = tBERS(max)

Table 7-2 Common Testing Conditions for ICC

Parameter	SDR	NV-DDR	NV-DDR2/NV-DDR3
AC Timing Parameters	tWC = tWC(min) tRC = tRC(min) tADL = ~tADL(min) tCCS = ~tCCS(min) tRHW = ~tRHW(min)	tCK = tCK(avg) tADL =~tADL(min) tCCS = ~tCCS(min) tRHW = ~tRHW(min)	tWC = tWC(min) tRC = tRC(avg) tDSC = tDSC(avg) tADL = ~tADL(min) tCCS = ~tCCS(min)
Bus idle data pattern	IO[7:0] = FFh IO[15:0] = FFFFh	DQ[7:0] = FFh	DQ[7:0] = FFh
Repeated data pattern (Used for ICC4R, ICCQ4R, ICCQ4W and ICC4W)	IO[7:0] = A5h, AAh, 5Ah, 55h IO[15:0] = A5A5h, AAAAh, 5A5Ah, 5555h	DQ[7:0] = A5h, AAh, 5Ah, 55h	DQ[7:0] = A5h, AAh, 5Ah, 55h
NOTES: 1. The value of tCK(avg), tRC(avg), and tDSC(avg) used should be the minimum value of the timing modes supported for the device. The NV-DDR, NV-DDR2, and NV-DDR3 timing modes supported by the device are indicated in the parameter page. **2.** ICCQ4R testing is performed with default drive strength setting.			

Table 7-3 Data Interface Specific Testing Conditions for ICC

The following figures detail the testing procedure for ICC1, ICC2, ICC3, ICC4R, ICC4W, and ICC5.

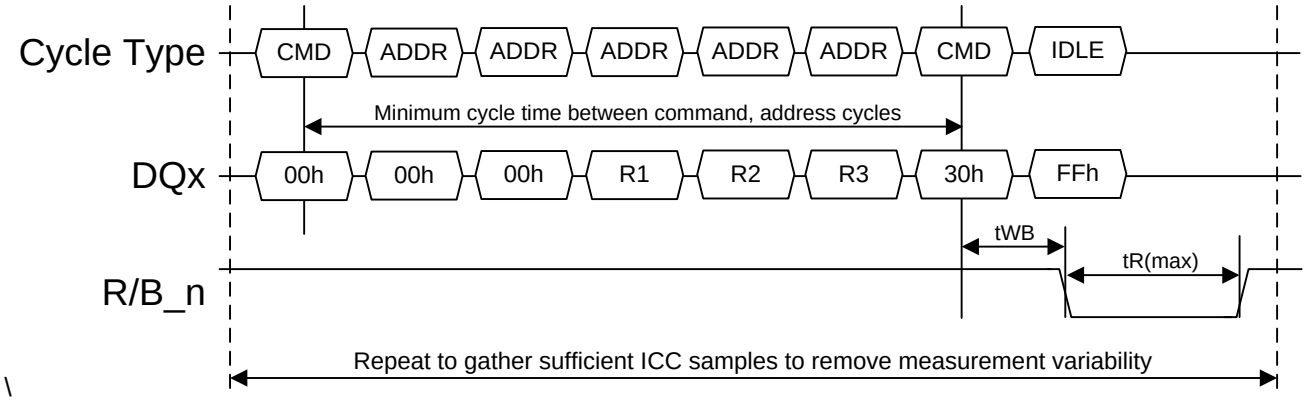


Figure 7-1 ICC1 measurement procedure

To calculate the active current for ICC1, the following equations may be used.

$$Icc1(measured) = \frac{tR(typ)}{tR(\max)} Icc1(active) + \frac{tR(max) - tR(typ)}{tR(max)} Icc5$$

$$Icc1(active) = \frac{Icc1(measured) \times tR(max)}{tR(typ)} - \frac{Icc5 \times tR(max)}{tR(typ)} + Icc5$$

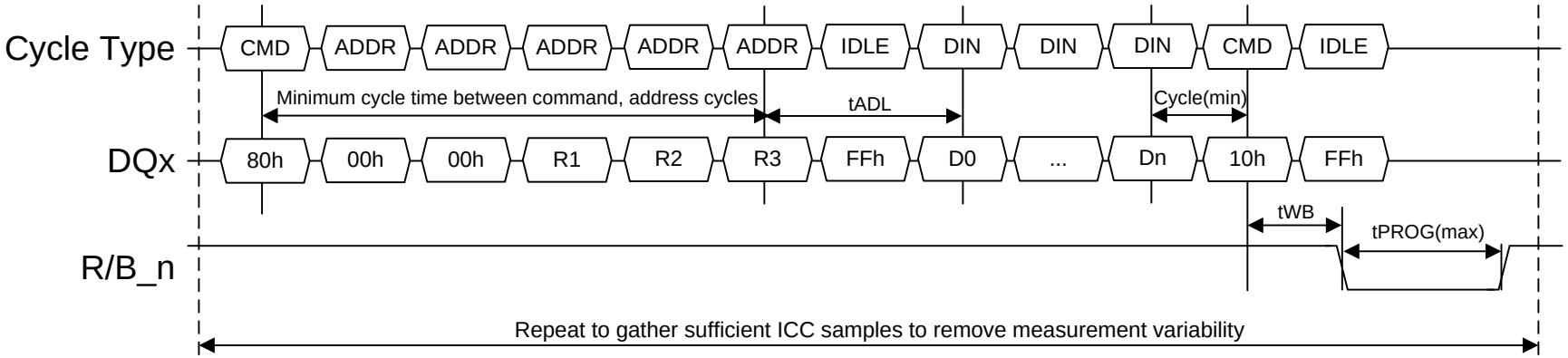


Figure 7-2 ICC2 measurement procedure

To calculate the active current for ICC2, the following equations may be used.

$$Icc2(measured) = \frac{tIO}{tIO + tPROG(max)} Icc4w + \frac{tPROG(typ)}{tIO + tPROG(max)} Icc2(active) + \frac{tPROG(max) - tPROG(typ)}{tIO + tPROG(max)} Icc5$$

$$Icc2(active) = \frac{Icc2(measured) \times (tIO + tPROG(max)]}{tPROG(typ)} - \frac{tIO \times Icc4w}{tPROG(typ)} - \frac{Icc5 \times tPROG(max)}{tPROG(typ)} + Icc5$$

For the SDR interface, the tIO value is calculated as:

$$tIO = NAND\ Page\ Size(bytes\ (x8) or\ words\ (x16)) \times tWC(min)$$

For the NV-DDR data interface, the tIO value is calculated as:

$$tIO = NAND\ Page\ Size(bytes) \times \frac{1}{2} tCK(avg)$$

For the NV-DDR2 and NV-DDR3 data interfaces, the tIO value is calculated as:

tIO= NAND Page Size(bytes) x (1/2 tDSC(avg))

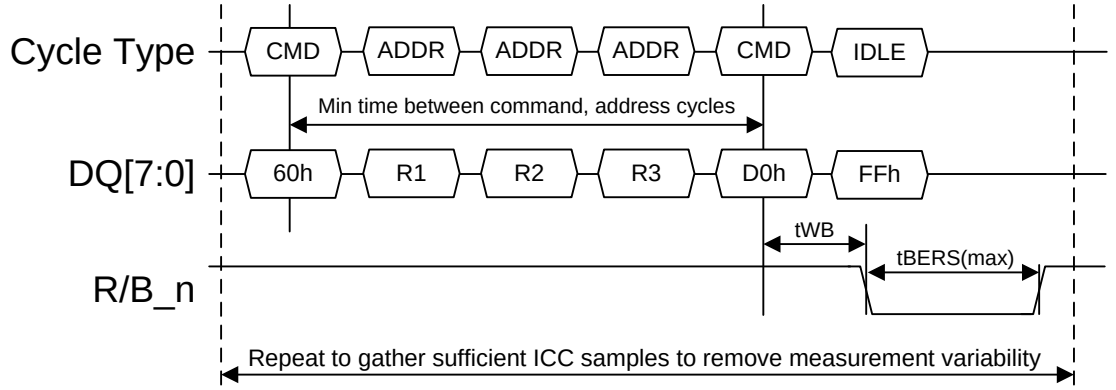


Figure 7-3 ICC3 measurement procedure

To calculate the active current for ICC3, the following equations may be used.

$$Icc3(measured) = \frac{tBERS(typ)}{tBERS(max)} Icc3(active) + \frac{tBERS(max) - tBERS(typ)}{tBERS(max)} Icc5$$

$$Icc3(active) = \frac{Icc3(measured) \times tBERS(max)}{tBERS(typ)} - \frac{Icc5 \times tBERS(max)}{tBERS(typ)} + Icc5$$

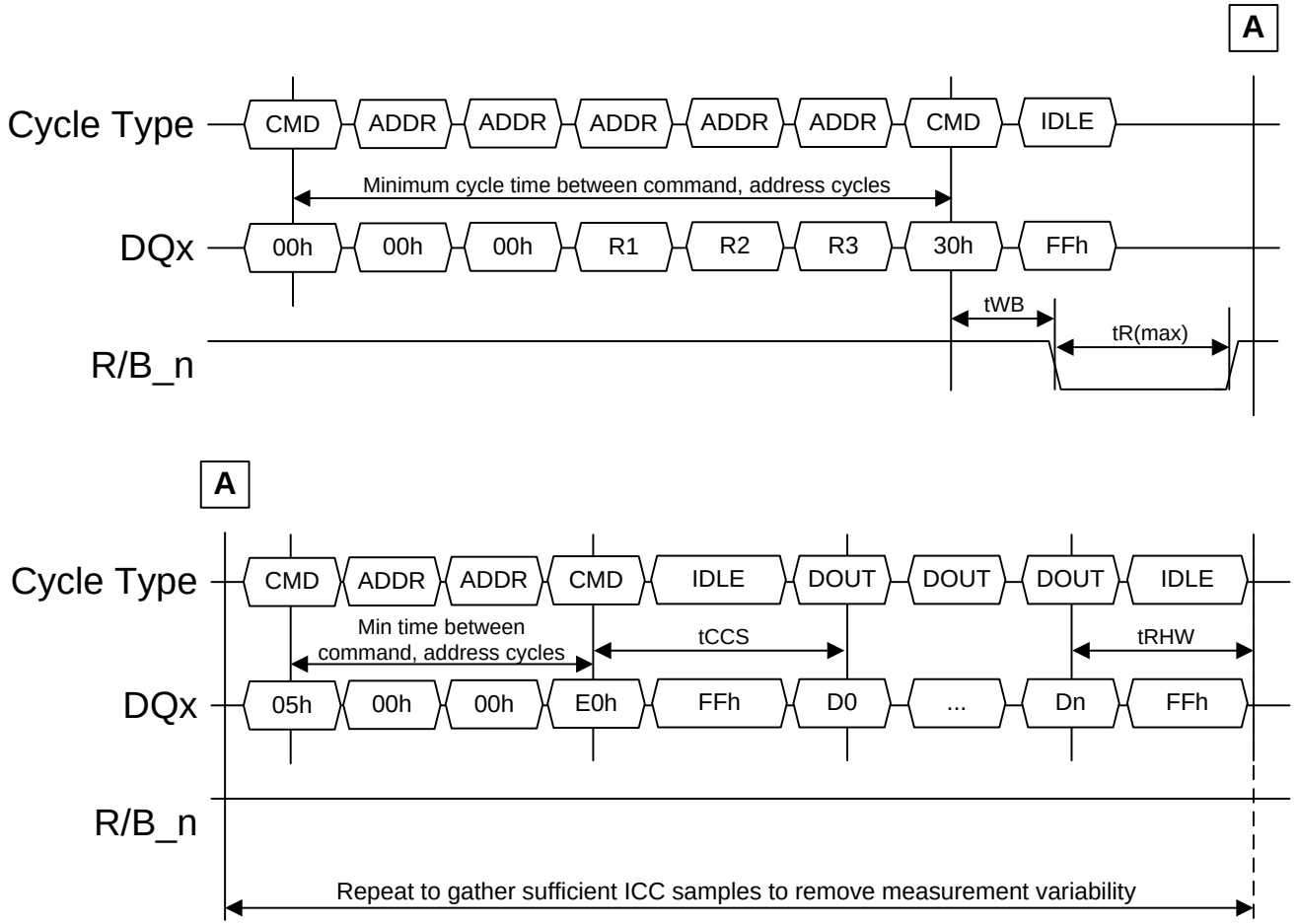


Figure 7-4 ICC4R and ICCQ4R measurement procedure

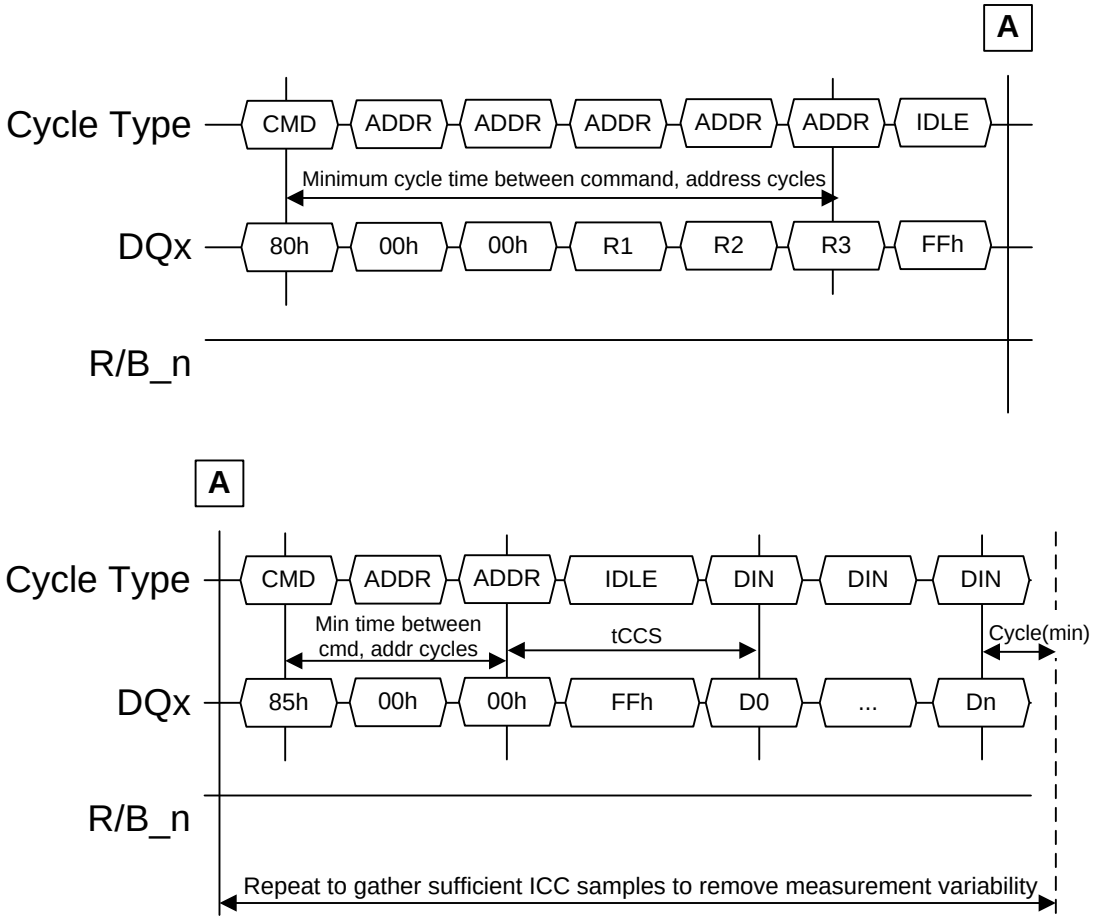


Figure 7-5 ICC4W measurement procedure

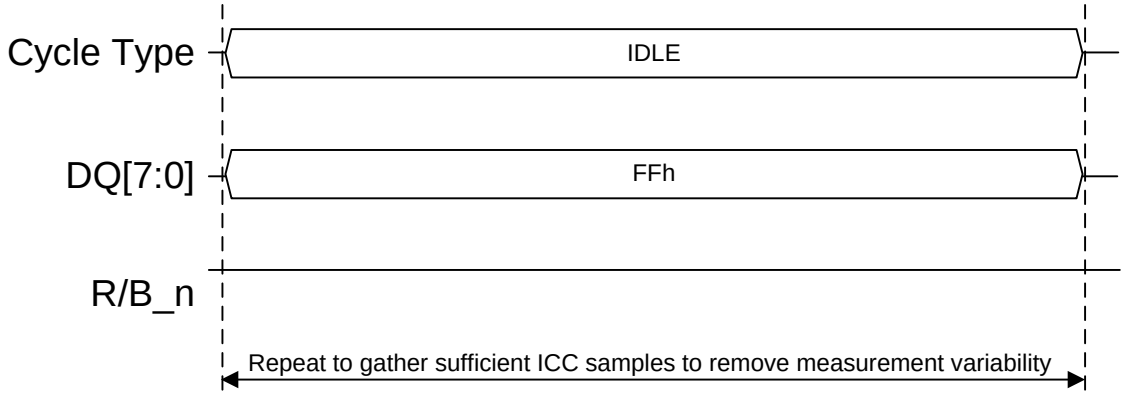


Figure 7-6 ICC5 measurement procedure

E. MEASURING TIMING PARAMETERS TO/FROM TRI-STATE

There are several timing parameters that are measured to or from when:

- The device is no longer driving the NAND bus or a tri-state (hi-Z) condition
- The device begins driving from a tri-state (hi-Z) condition

These timing parameters include: tDQSD, tDQSHZ, tCHZ, tRHZ, and tIR. See section 4.18.

This appendix defines a two point method for measuring timing parameters that involve a tri-state condition. Figure 7-7 defines a method to calculate the point when the device is no longer driving the NAND bus or begins driving by measuring the signal at two different voltages. The voltage measurement points are acceptable across a wide range (x = 20 mV up to x < 1/4 of VccQ). The figure uses tDQSHZ and tDQSD as examples. However, the method should be used for any timing parameter (SDR, NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4) that specifies that the device output is no longer driving the NAND bus or specifies that the device begins driving the NAND bus from a tri-state condition.

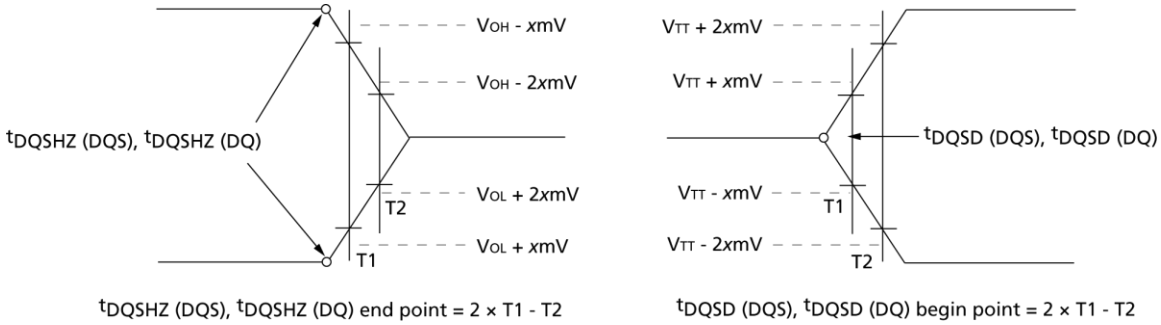


Figure 7-7 Two point method for measuring timing parameters with tri-state condition